2N6851 File Number **2218**

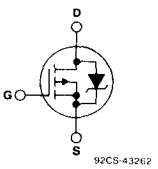
Avalanche-Energy-Rated P-Channel Power MOSFETs

-4.0A, and -200V
r_{DS} (on) = 0.80Ω

Features:

- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

TERMINAL DIAGRAM

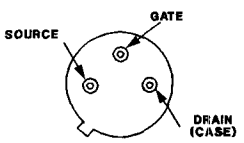


P-CHANNEL ENHANCEMENT MODE

The 2N6851 is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. This is a p-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The 2N6851 is supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

TERMINAL DESIGNATION



JEDEC TO-205AF

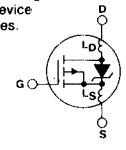
Absolute Maximum Ratings

Parameter		2N6851	Units
V_{DS}	Drain-Source Voltage	-200*	V
V_{DG}	Drain-Gate Voltage (R_{GS} = 20kΩ)	-200*	V
I_D @ T_C = 25°C	Continuous Drain Current	-4.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	-2.4*	A
I_{DM}	Pulsed Drain Current ②	-20*	A
V_{GS}	Gate-Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	25* (See Fig. 14)	W
	Linear Derating Factor	0.2* (See Fig. 14)	W/°C
E_{AS}	Single Pulse Avalanche Energy ③	500	mJ
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	−200*	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	−2.0*	—	−4.0*	V	V_{DS} = V_{GS}, I_D = −0.25mA
I_{GSS}	Gate-Source Leakage Forward	—	—	−100	nA	V_{GS} = −20V
I_{GSS}	Gate-Source Leakage Reverse	—	—	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	−0.25*	μA	V_{DS} = Max. Rating, V_{GS} = 0V
		—	—	−1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Drain Voltage ①	—	—	−3.3	V	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ max., V_{GS} = −10V, I_D = −4.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	—	—	0.80*	Ω	V_{GS} = −10V, I_D = −2.4A
g_{fs}	Forward Transconductance ①	2.2	3.5	−6.6	S(℧)	V_{DS} = −5V × $R_{DS(on)max.}$, I_D = −2.4A
C_{iss}	Input Capacitance	400	550	—	pF	V_{GS} = 0V, V_{DS} = −25V, f = 1.0 MHz
C_{oss}*	Output Capacitance	50	170	—	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	40	50	—	pF	
$t_{d(on)}$	Turn-On Delay Time	—	30	50	ns	V_{DD} = −95V, I_D = −2.4A, Z_o = 50Ω
t_r	Rise Time	—	50	100	ns	See Fig. 17
$t_{d(off)}$	Turn-Off Delay Time	—	50	80	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	—	40	80	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	—	31	45	nC	V_{GS} = −15V, I_D = −8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	—	18	23	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	—	13	22	nC	
L_D	Internal Drain Inductance	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	—	15	—	nH	Measured from the source lead, 5 mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

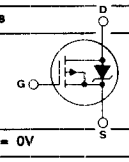


Thermal Resistance

$R\theta_{JC}$	Junction-to-Case	—	—	5.0*	°C/W	
$R\theta_{JA}$	Junction-to-Ambient	—	—	175	°C/W	Typical socket mount

Source-Drain Diode Ratings and Characteristics

Parameter		Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	−4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
I_{SM}	Pulse Source Current (Body Diode) ②	—	—	−20	A	
V_{SD}	Diode Forward Voltage ①	—	—	-1.5	V	T_C = 25°C, I_S = −4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	—	—	400	ns	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
Q_{RR}	Reverse Recovered Charge	—	2.6	—	μC	T_J = 25°C, I_F = −4.0A, dI_F/dt = −100 A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



*JEDEC Registered Value

① Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ V_{DD} = 50V, starting T_J = 25°C, L = 46.9 mH, R_G = 25Ω, Peak I_L = 4.0A. (See Fig. 15 and 16)

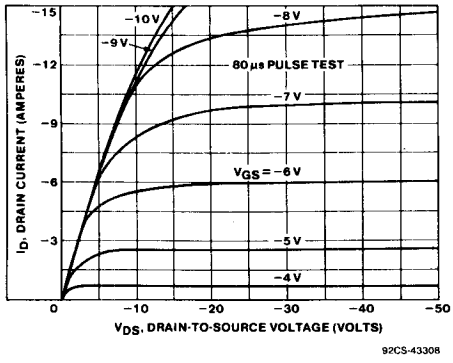


Fig. 1 - Typical Output Characteristics

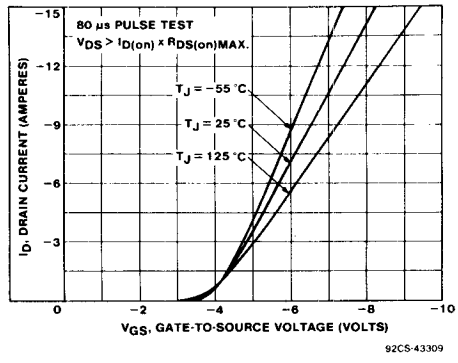


Fig. 2 - Typical Transfer Characteristics

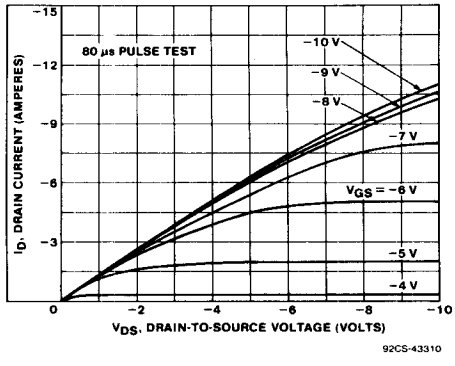


Fig. 3 - Typical Saturation Characteristics

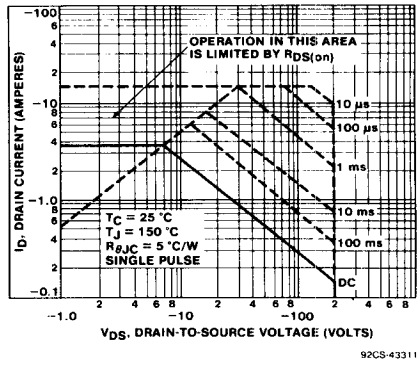


Fig. 4 - Maximum Safe Operating Area

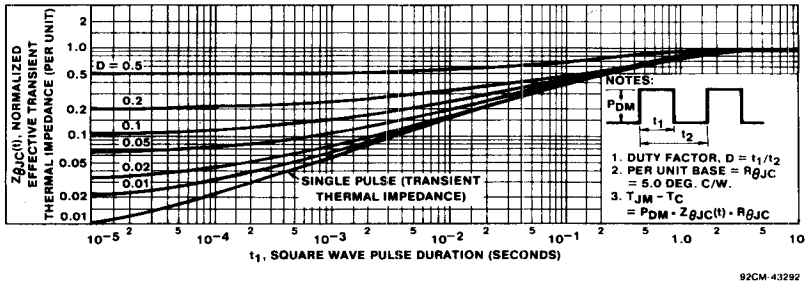


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

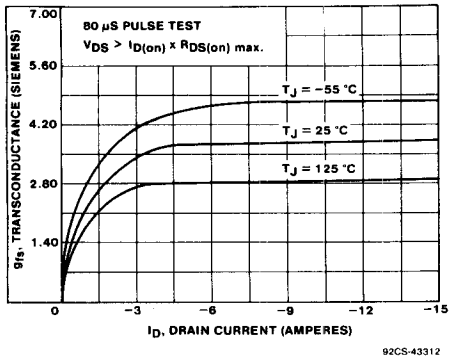


Fig. 6 - Typical Transconductance Vs. Drain Current

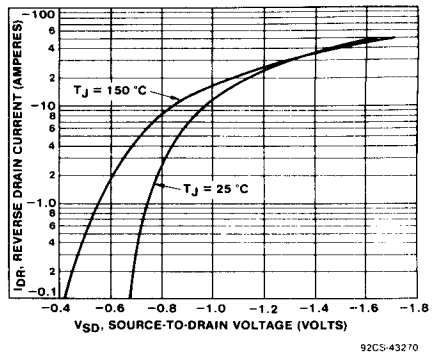


Fig. 7 - Typical Source-Drain Diode Forward Voltage

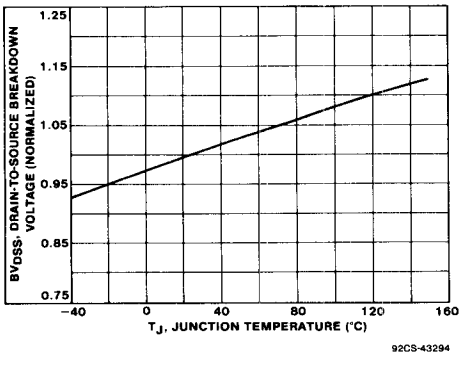


Fig. 8 - Breakdown Voltage Vs. Temperature

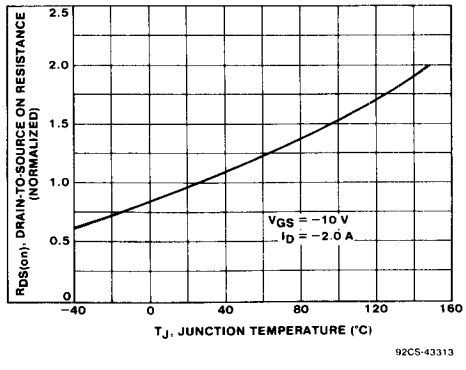


Fig. 9 - Normalized On-Resistance Vs. Temperature

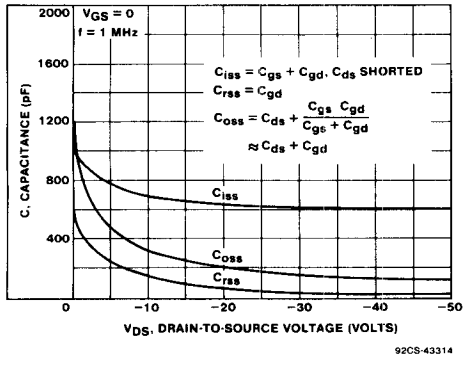


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

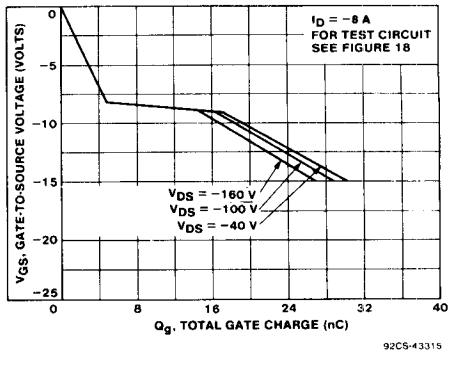


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

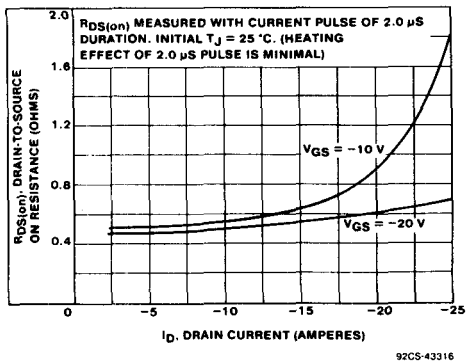


Fig. 12 - Typical On-Resistance Vs. Drain Current

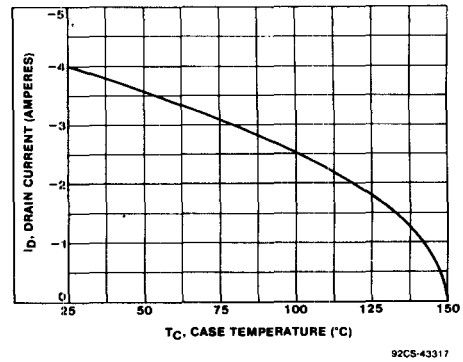


Fig. 13 - Maximum Drain Current Vs. Case Temperature

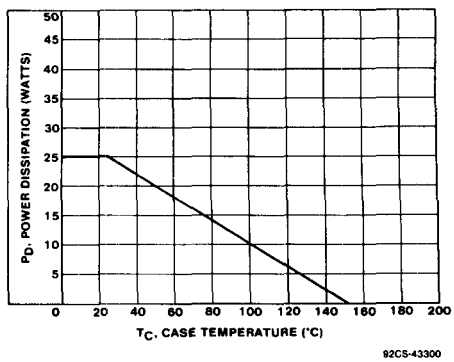


Fig. 14 - Power Vs. Temperature Derating Curve

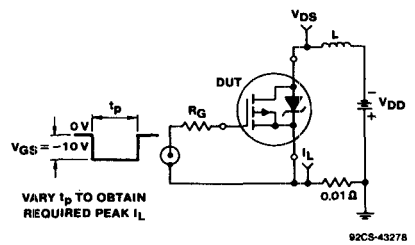


Fig. 15 - Unclamped Inductive Test Circuit

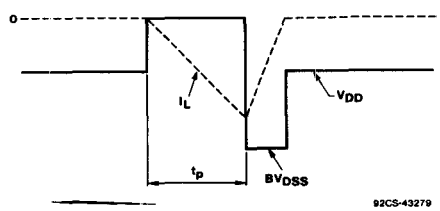


Fig. 16 - Unclamped Inductive Waveforms

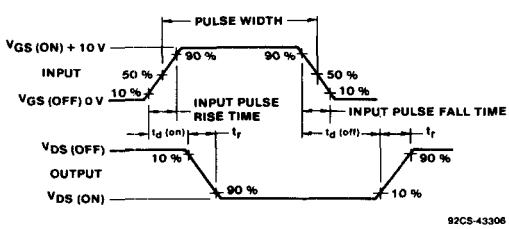


Fig. 17 - Switching Time Test Circuit

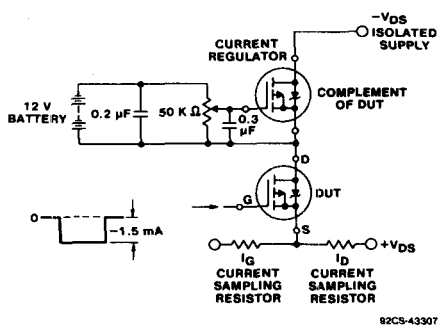


Fig. 18 - Gate Charge Test Circuit

JAN, JANTX, and JANTXV

JAN, JANTX, and JANTXV Solid-State Power Devices

The major military specification used for the procurement of standard solid-state devices by the military is MIL-S-19500, which covers the devices such as discrete transistors, thyristors, and diodes.

MIL-S-19500 is the specification for the familiar "JAN" type solid state devices. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center (DESC).

Levels of reliability are defined by MIL-S-19500. JAN types receive Group A, Group B, and Group C lot sampling only, and are the least expensive. JANTX types receive 100 percent process conditioning, and power conditioning, and are subjected to lot rejection based on delta parameter criteria in addition to Group A, Group B, and Group C lot sampling. JANTXV types are subjected to 100 percent (JTXV) internal visual inspection in addition to all of the JANTX tests in accordance with MIL-STD-750 test methods and MIL-S-19500.

DESC publishes "QPL-19500", a Qualified Products List of all types and suppliers approved to produce and brand devices in accordance with MIL-S-19500.

The following tables list approved "QPL" types and types that are process of testing preliminary to QPL approval by DESC, respectively.

Custom high-reliability selections of Harris Power MOSFETs can also be supplied with similar process and power conditioning tests and delta criteria.

QPL Approved Types

Harris is presently qualified on the following devices. Prices and delivery quotations may be obtained from your local sales representative.

JAN and JANTX Power MOSFETs

N-Channel Types	MIL-S-19500/	Package	Channel	P_T (W)	I_D (A)	BV_{DSS} (V)	r_{DS} (on) Ω
2N6756	542	TO-204AA	N	75	14	100	0.18
2N6758	542	TO-204AA	N	75	9	200	0.4
2N6760	542	TO-204AA	N	75	5.5	400	1
2N6762	542	TO-204AA	N	75	4.5	500	1.5
2N6764	543	TO-204AE	N	150	38	100	0.055
2N6766	543	TO-204AE	N	150	30	200	0.085
2N6768	543	TO-204AA	N	150	14	400	0.3
2N6770	543	TO-204AA	N	150	12	500	0.4
2N6782	556	TO-205AF	N	15	3.5	100	0.6
2N6784	556	TO-205AF	N	15	2.25	200	1.5
2N6788	555	TO-205AF	N	20	6	100	0.3
2N6790	555	TO-205AF	N	20	3.5	200	0.8
2N6792	555	TO-205AF	N	20	2	400	1.8
2N6794	555	TO-205AF	N	20	1.5	500	3
2N6796	557	TO-205AF	N	25	8	100	0.18
2N6798	557	TO-205AF	N	25	5.5	100	0.4
2N6800	557	TO-205AF	N	25	3	400	1
2N6802	557	TO-205AF	N	25	2.5	500	1.5
P-Channel Types	**MIL-S-19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**r_{DS} (on) Ω**
2N6895	565	TO-205AF	P	8.33	-1.5	-100	3.65
2N6896	565	TO-204AA	P	60	-6	-100	0.6
2N6897	565	TO-204AA	P	100	-12	-100	0.3
2N6898	565	TO-204AA	P	150	-25	-100	0.2
2N6849	564	TO-205AF	P	25	-6.5	-100	0.3
2N6851	564	TO-205AF	P	25	-4.0	-200	0.8
N-Channel Logic-Level Types	**MIL-S-19500/**	**Package**	**Channel**	**P_T (W)**	**I_D (A)**	**BV_{DSS} (V)**	**r_{DS} (on) Ω**
2N6901	566	TO-205AF	N	8.33	1.5	100	1.4
2N6902	566	TO-204AA	N	75	12	100	0.2
2N6903	566	TO-205AF	N	8.33	1.5	200	3.65
2N6904	566	TO-204AA	N	75	8	200	0.65