

ISL9211B

Charging System Safety Circuit

FN7861
Rev 1.00
November 4, 2014

The ISL9211B is an integrated circuit (IC) optimized to provide a redundant safety protection to a Li-ion battery charging system. The IC monitors input voltage, battery voltage, and charge current. When any of these parameters exceeds its limit, the IC turns off an internal N-channel MOSFET to remove power from the charging system to the battery. The IC also monitors its own internal temperature and turns off the N-channel MOSFET when the temperature exceeds +150 °C. Together with the battery charger IC and the protection module in a battery pack, the charging system using the ISL9211B has triple-level protection and is two-fault tolerant.

The IC is designed to turn on the internal NFET slowly, to avoid in-rush current at power-up. It turns off the NFET quickly when the input is overvoltage, to remove power before damage occurs. The ISL9211B has a logic flag output to indicate a fault condition. The enable input allows the system to cut off the input power, if needed.

Related Literature

- Technical Brief [TB363](#) "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Technical Brief [TB379](#) "Thermal Characterization of Packaged Semiconductor Devices"
- Technical Brief [TB389](#) "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"

Features

- 24V Max Input Voltage
- Supports Up To 2.0A Input Current
- Fully Integrated Protection Circuit for Three Protected Variables
- High Accuracy Protection Thresholds
- User Programmable Overcurrent Protection Threshold
- Responds to Input Overvoltage in Less Than 1μs
- High Immunity of False Triggering Under Transients
- Fault Indication for Various Fault Occurrence
- Easy to Use
- Pb-Free (RoHS Compliant)

Applications

- Cell Phones
- Digital Still Cameras
- PDAs and Smart Phones
- Portable Instruments
- Desktop Chargers

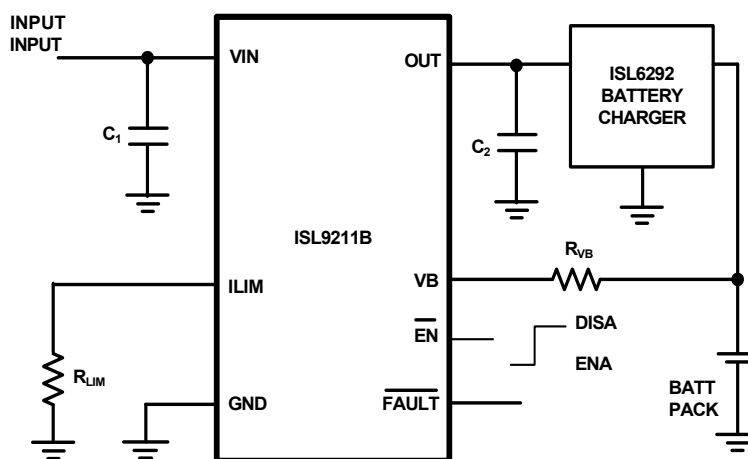
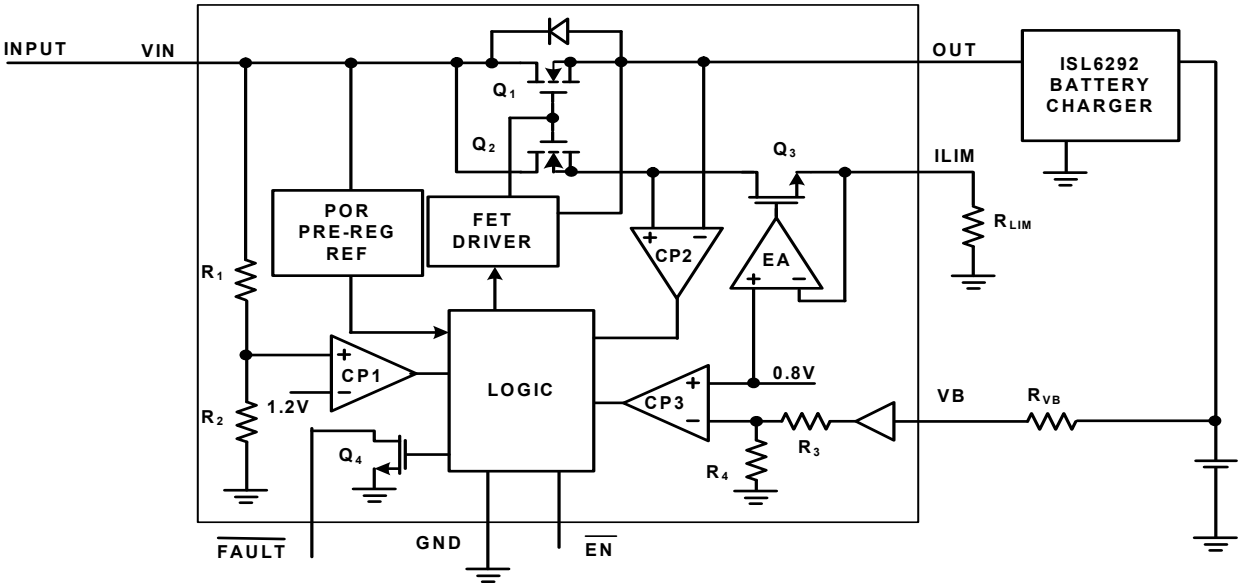
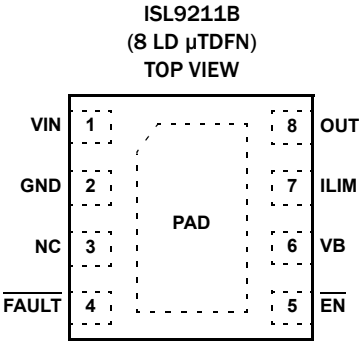


FIGURE 1. TYPICAL APPLICATION CIRCUIT

Block Diagram



Pin Configuration



Pin Descriptions

SYMBOL	PIN NUMBER	DESCRIPTION
VIN	1	The input power source. VIN can withstand 24V input.
GND	2	System ground reference.
NC	3	No connection, and must be left floating.
$\overline{\text{FAULT}}$	4	$\overline{\text{FAULT}}$ is an open-drain logic output that turns LOW when any protection event occurs.
$\overline{\text{EN}}$	5	IC enable pin. Pull this pin to LO to enable the device and pull it to HI to disable.
VB	6	Battery voltage monitoring input. This pin is connected to the battery pack positive terminal via an isolation resistor.
ILIM	7	Overcurrent protection threshold setting pin. Connect a resistor between this pin and GND to set the OCP threshold.
OUT	8	Output pin.
PAD	PAD	Exposed pad. Connect to system ground.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ISL9211BIRU58XZ-T	58X	-40 to +85	8 Ld μ TDFN	L8.2x2B

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL9211B](#). For more information on MSL please see Tech Brief [TB363](#).

Absolute Maximum Ratings

Supply Voltage (V_{IN})	-0.3V to 26V
Output and VB Pin (OUT, VB) (Note 4)	-0.3V to 8V
Other Pins (ILIM, FAULT, EN)	-0.3V to 5.5V
ESD Rating	
Human Body Model (Tested per JESD22-A114F)	3kV
Machine Model (Tested per JESD22-A115-A)	200V
Latch Up (Tested per JESD78B; Class II, Level A)	100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld 2x2 μ TDFN (Notes 5, 6)	98	37
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

Recommended Operating Conditions

Ambient Temperature Range	-40°C to +85°C
Supply Voltage, V_{IN}	4.3V to 24V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- The maximum voltage rating for the VB pin under continuous operating conditions is 5.5V. All other pins are allowed to operate continuously at the absolute maximum ratings.
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).
- For θ_{JC} , the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER-ON RESET						
V _{IN} Threshold	V _{POR}	Rising	-	-	2.47	V
		Falling	2.20	-	-	V
V _{IN} Bias Current	I _{VIN}	R _{LIM} = 24.9k, $\overline{EN}$ = L	-	-	1000	μA
		$\overline{EN}$ = H	-	80	-	μA
PROTECTIONS						
Input OVP Protection	V _{OVP}		5.6	5.8	6.0	V
Input OVP Hysteresis			-	100	-	mV
Input OVP Falling Threshold			5.55	-	-	V
Input OVP Response Time (Note 7)			-	-	1	μs
Overcurrent Protection	I _{OCP}	V _{VB} = 3V, R _{LIM} = 24.9kΩ	0.93	1.0	1.07	A
Maximum Output Current	I _{MAX}	R _{LIM} = 9.53kΩ	-	2.0	-	A
Overcurrent Protection Blanking Time	BT _{OCP}		-	2.0	-	μs
Battery Overvoltage Protection Threshold	V _{BOVP}		4.25	4.34	4.40	V
Battery OVP Threshold Hysteresis			-	30	-	mV
Battery OVP Blanking Time	BT _{BOVP}		-	180	-	μs
VB Pin Leakage Current		V _{VB} = 4.34V	-	-	20	nA
Over-Temperature Protection Rising Threshold			-	150	-	°C
Over-Temperature Protection Falling Threshold			-	110	-	°C
LOGIC						
$\overline{EN}$ Input Logic HIGH			1.5	-	-	V
$\overline{EN}$ Input Logic LOW			-	-	0.4	V
$\overline{EN}$ Internal Pull-down Resistor			-	200	-	kΩ
$\overline{FAULT}$ Output Logic Low		Sink 5mA current	-	0.4	0.8	V

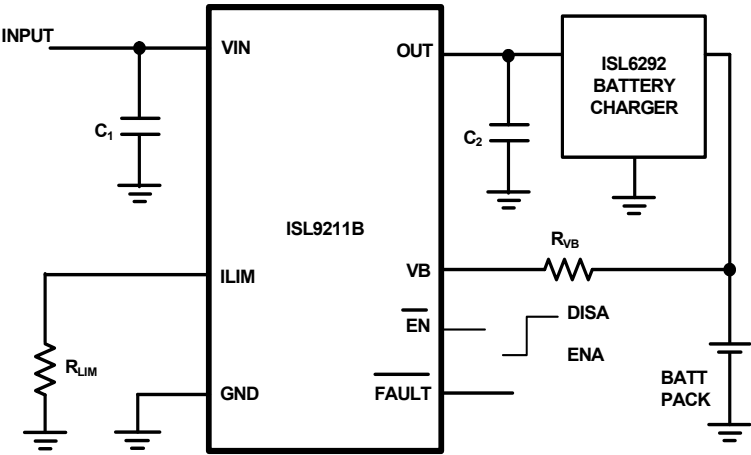
Electrical Specifications **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
FAULT Output Logic High Leakage Current		Pin Voltage = 4.2V	-	-	1.5	μA
POWER MOSFET						
On-Resistance (Note 7)	r_{DS(ON)}	Measured at 200mA	-	170	280	mΩ

NOTES:

- 7. Limits should be considered typical and are not production tested.
- 8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Application



PART	DESCRIPTION
R _{LIM}	24.9kΩ
R _{VB}	200kΩ to 1MΩ
C ₁ , C ₂	1μF/25V X5R ceramic capacitor

Typical Operating Performance Test conditions for typical operating performance are: $V_{IN} = 5V$, $T_A = +25^\circ C$, $R_{LIM} = 24.9k\Omega$, $R_{VB} = 200k\Omega$, unless otherwise noted.

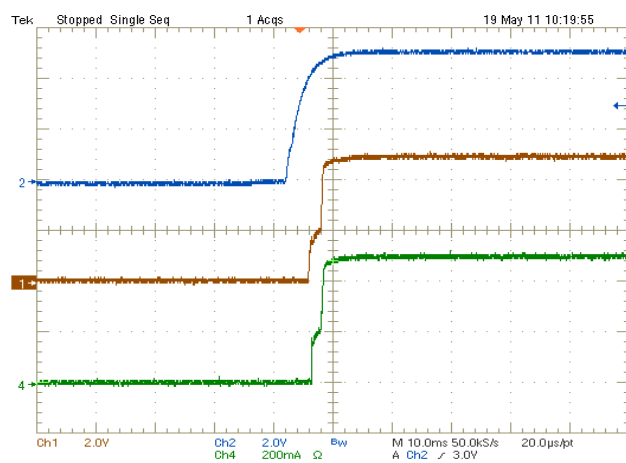


FIGURE 2. POWER UP WITH 500mA LOAD (CH1 = V_{OUT} , CH2 = V_{IN} , CH4 = I_{OUT})

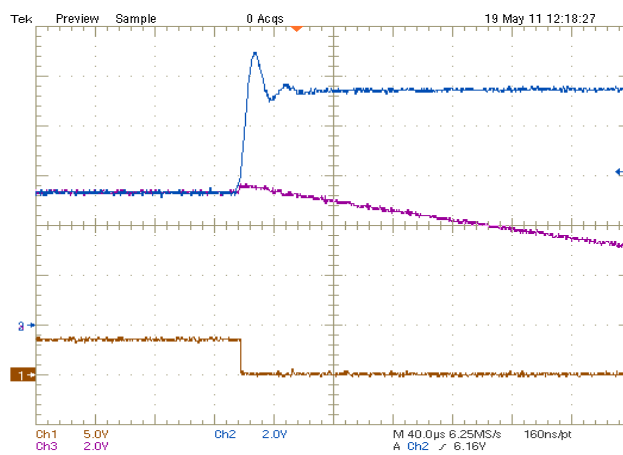


FIGURE 3. INPUT OVERVOLTAGE PROTECTION - V_{IN} STEPPING FROM 5.5V TO 9.5V (CH1 = V_{FAULT} , CH2 = V_{IN} , CH3 = V_{OUT})

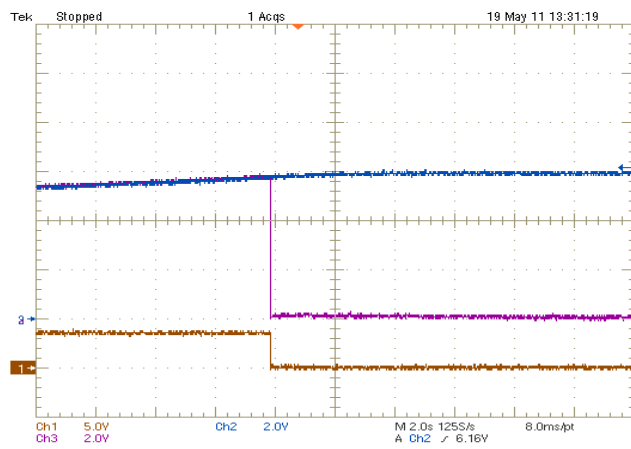


FIGURE 4. INPUT OVERVOLTAGE PROTECTION - V_{IN} SLOWLY RAMPING UP TO OVP THRESHOLD (CH1 = V_{FAULT} , CH2 = V_{IN} , CH3 = V_{OUT})

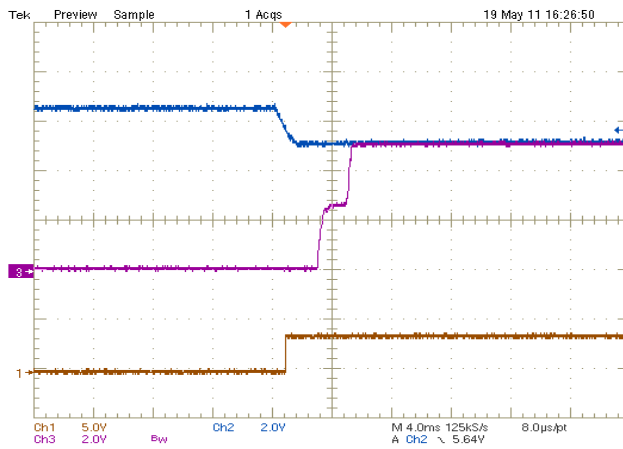


FIGURE 5. LINE TRANSIENT - V_{IN} STEPPING FROM 6.5V TO 5.5V (CH1 = V_{FAULT} , CH2 = V_{IN} , CH3 = V_{OUT})

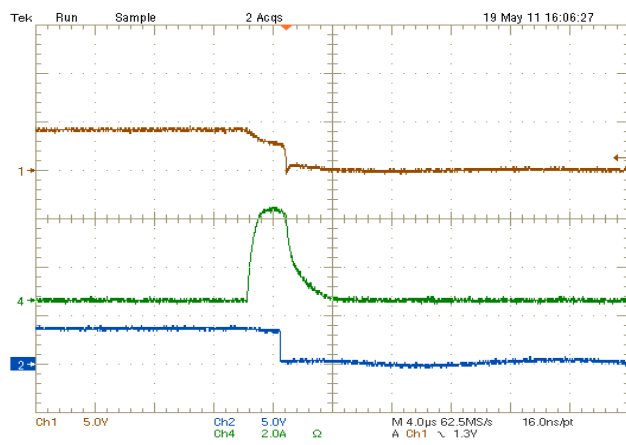


FIGURE 6. SHORT CIRCUIT TEST (CH1 = V_{OUT} , CH2 = V_{FAULT} , CH3 = V_{IN} , CH4 = I_{OUT})

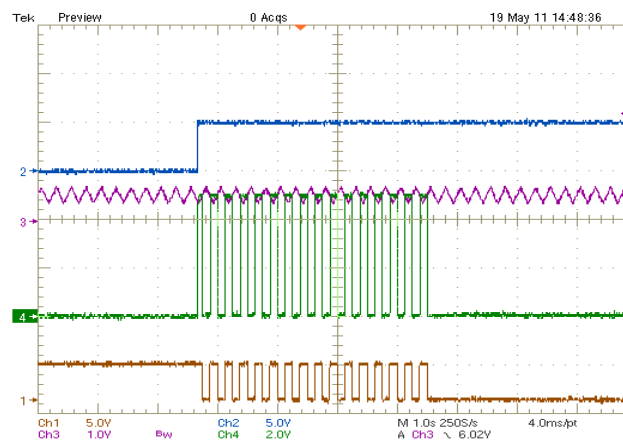


FIGURE 7. BATTERY OVERVOLTAGE PROTECTION - V_B VARYING BETWEEN 4.3V TO 4.5V. THE IC LATCHED OFF AFTER 16 COUNTS PROTECTION (CH1 = V_{FAULT} , CH2 = V_{IN} , CH3 = V_B , CH4 = V_{OUT})

Typical Operating Performance Test conditions for typical operating performance are: $V_{IN} = 5V$, $T_A = +25^\circ C$, $R_{LIM} = 24.9k\Omega$, $R_{VB} = 200k\Omega$, unless otherwise noted. (Continued)

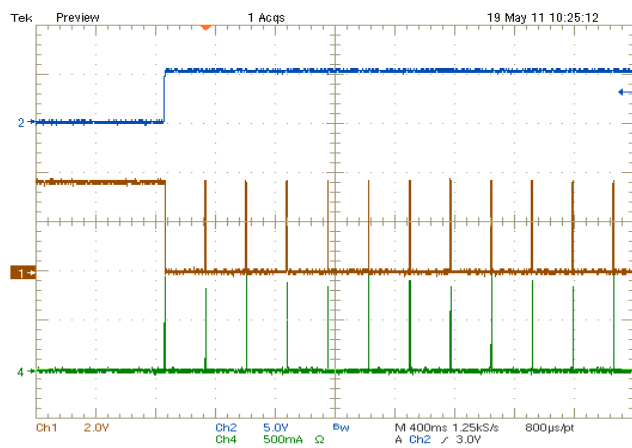


FIGURE 8. POWER UP WITH OUTPUT SHORTED (CH1 = V_{FAULT} , CH2 = V_{IN} , CH4 = I_{OUT})

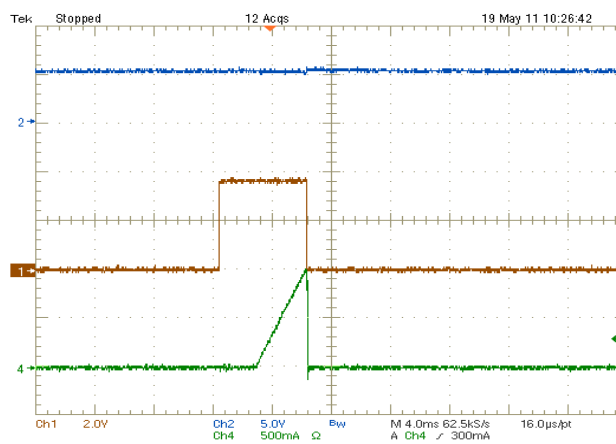


FIGURE 9. ZOOMED-IN VIEW OF FIGURE 8

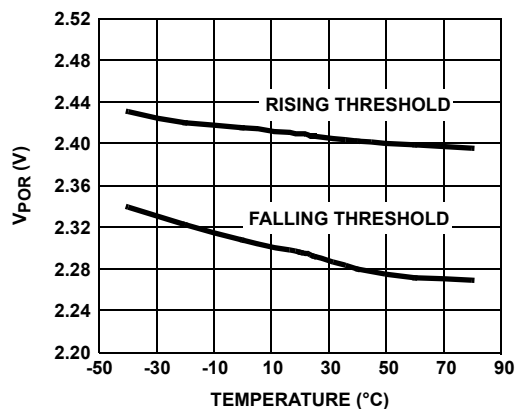


FIGURE 10. V_{POR} vs TEMPERATURE

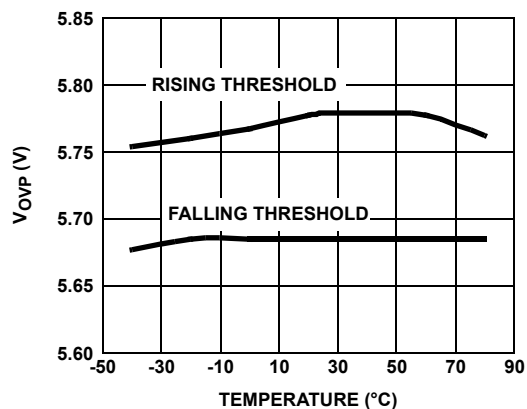


FIGURE 11. INPUT OVERVOLTAGE PROTECTION vs TEMPERATURE

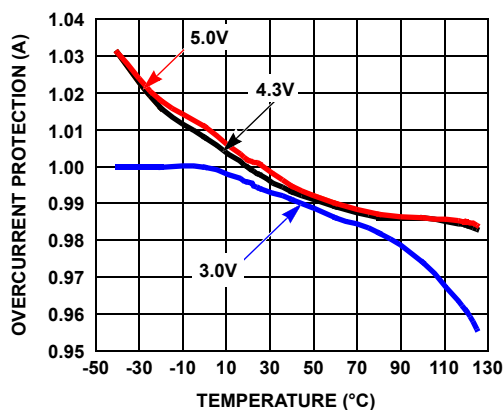


FIGURE 12. OVERCURRENT PROTECTION vs TEMPERATURE AT VARIOUS INPUT VOLTAGES

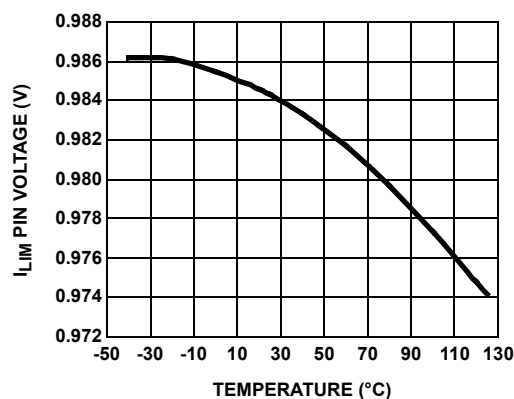


FIGURE 13. I_{LIM} PIN VOLTAGE vs TEMPERATURE

Typical Operating Performance

Test conditions for typical operating performance are: $V_{IN} = 5V$, $T_A = +25^\circ C$, $R_{LIM} = 24.9k\Omega$, $R_{VB} = 200k\Omega$, unless otherwise noted. (Continued)

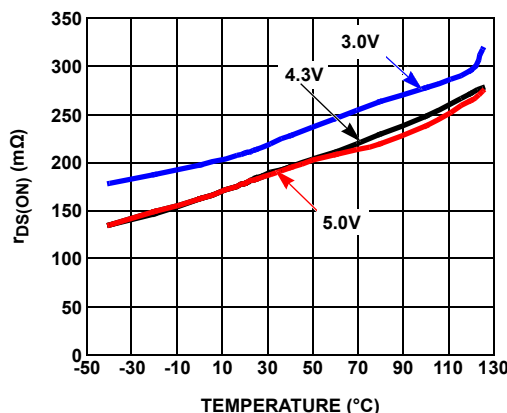


FIGURE 14. ON-RESISTANCE vs TEMPERATURE AT DIFFERENT INPUT VOLTAGES

Theory of Operation

The ISL9211B is an integrated circuit (IC) optimized to provide redundant safety protection to a Li-ion battery against charging system failures. The IC monitors input voltage, battery voltage, and charge current. When any of these parameters exceeds its limit, the IC turns off an internal N-channel MOSFET to remove power from the charging system. The IC also monitors its own internal temperature and turns off the N-channel MOSFET when temperature exceeds $+150^\circ C$. Together with the battery charger IC and the protection module in a battery pack, the charging system has triple-level protection against overcharging the Li-ion battery and is two-fault tolerant. The ISL9211B protects up to 26V input voltage.

Power-Up

The ISL9211B has a power-on reset (POR) threshold of 2.47V (max). Before the input voltage reaches the POR threshold, the internal power NFET is off. Approximately 10ms after the input voltage exceeds the POR threshold, the IC resets itself and begins soft-start. The 10ms delay allows any transients at the input during a hot insertion of the power supply to settle down before the IC starts to operate. The soft-start slowly turns on the power NFET to reduce the inrush current as well as the input voltage drop during the transition. Figure 2 shows the power-up sequence.

Input Overvoltage Protection (OVP)

The input voltage is monitored by the comparator, CP1, as shown in the "Block Diagram" on page 2. CP1 has an accurate reference of 1.2V from the bandgap reference. The OVP threshold is set by the resistive divider consisting of R_1 and R_2 . When the input voltage exceeds the threshold, CP1 outputs a logic signal to turn off the power NFET within $1\mu s$ (see Figure 3). This prevents high input voltage from damaging the electronics in a handheld system. Hysteresis for the input OVP threshold is given in the "Electrical Specifications" table on page 4. When the input overvoltage condition is removed, the ISL9211B re-enables the output by running through soft-start, as shown in Figure 5. Because of the 10ms delay before soft-start, the output is never

enabled if the input rises above the OVP threshold quickly, as shown in Figure 6.

Battery Overvoltage Protection

Battery voltage OVP is realized with the VB pin. The comparator, CP3, shown in the "Block Diagram" on page 2, monitors the VB pin and issues an overvoltage signal when battery voltage exceeds the 4.34V battery OVP threshold. The threshold has 30mV built-in hysteresis. The comparator, CP3, has a built-in 180 μs blanking time to prevent any transient voltage from triggering OVP. If the OVP situation still exists after the blanking time, the power NFET is turned off. The control logic contains a 4-bit binary counter so that, if the battery overvoltage event occurs 16 times, the power NFET is turned off permanently, as shown in Figure 7. Recycling the input power resets the counter and restarts the ISL9211B.

The resistor, R_{VB} , between the VB pin and the battery, as shown in "TYPICAL APPLICATION CIRCUIT" on page 1, is an important component. This resistor provides a current limit in case the VB pin is shorted to the input voltage under a failure mode. VB pin leakage current under normal operation is negligible, which allows a resistance of 200k Ω to 1M Ω to be used.

Overcurrent Protection (OCP)

To prevent charging the battery with excessive current, the current in the power NFET is limited. Current is sensed using the voltage drop across the power FET after it is turned on. The reference for the OCP is generated using a sensing FET, Q_2 (mirror to Q_1), as shown in the "Block Diagram" on page 2. The current in the sensing FET is forced to match the value programmed by the I_{LIM} pin. The OCP threshold can be set with the resistor, R_{LIM} , as shown in Table 1.

The size of the power FET, Q_1 , is 31,250 times the size of the sensing FET. Therefore, when the current in the power FET is 31,250 times the current in the sensing FET, the drain voltage of the power FET falls below that of the sensing FET. The comparator, CP2, then outputs a signal to turn off the power FET. When an OCP condition is encountered, the power FET is turned off immediately and then attempts to restart. If the condition

persists, the FET shuts off again. This hiccup mode continues until the OCP condition is cleared. Figures 8 and 9 show the waveforms during power-up when the output is shorted to ground.

TABLE 1. CURRENT LIMIT RESISTOR SETTINGS

R_{LIM} (k Ω)	OCP (mA)	R_{LIM} (k Ω)	OCP (mA)
82.5	300	21	1200
61.9	400	19.1	1300
49.9	500	16.5	1400
41.2	600	15.4	1500
35.7	700	14	1600
31.6	800	12.4	1700
28	900	11.3	1800
24.9	1000	10.5	1900
22.6	1100	9.53	2000

Internal Over-Temperature Protection

The ISL9211B monitors its own internal temperature to prevent thermal failures. When the internal temperature reaches +150°C, the IC turns off the N-channel power MOSFET. The IC does not resume operation until the internal temperature drops below +110°C.

Fault Indication Output

The **FAULT** pin is an open-drain output that indicates a LOW signal when any of the three fault events occurs. This provides a signal to the microprocessor to take further action to enhance the safety of the charging system.

Applications Information

The ISL9211B is designed to meet the “Lithium-Safe” criteria when operating together with a qualified Li-ion battery charger. The “Lithium-Safe” criteria require the charger output to fall within the green region shown in Figure 15 under normal operating conditions and *not* to fall within the red region when there is a single fault in the charging system. Taking into account the safety circuit in a Li-ion battery pack, the charging system is allowed to have two faults without creating hazardous conditions for the battery cell. The output of a Li-ion charger such as the ISL6292C has a typical I-V curve (shown by the blue lines in Figure 15) under normal operation (shown by the green region). The function of the ISL9211B is to add a redundant protection layer such that, under any single fault condition, the charging system output does not exceed the I-V limits (shown by the red lines). As Figure 15 shows, a charging system that includes the ISL9211B and the ISL6292C chip set can easily meet the “Lithium-Safe” test criteria.

The ISL9211B is a simple device that requires only three external components, in addition to the ISL6292 charger circuit, to meet the “Lithium-Safe” criteria (see “TYPICAL APPLICATION CIRCUIT”

on page 1. The selection of the current limit resistor, R_{LIM} , is given in “Overcurrent Protection (OCP)” on page 8.

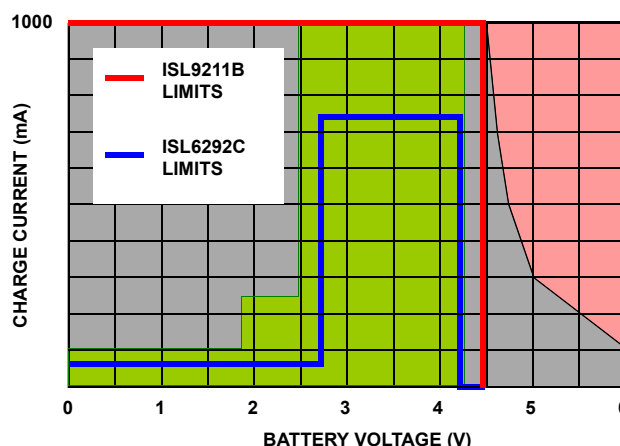


FIGURE 15. LITHIUM-SAFE OPERATING REGIONS

R_{VB} Selection

R_{VB} prevents a large current from the VB pin to the battery terminal, in case the ISL9211B fails. The recommended value is between 200k Ω and 1M Ω . With 200k Ω resistance, the worst-case current flowing from the VB pin to the charger output is shown in Equation 1, assuming VB pin voltage is 24V under failure mode and battery voltage is 4.2V.

$$(24V - 4.2V) / (200k\Omega) = 99\mu A \quad (EQ. 1)$$

Such a small current can easily be absorbed by the bias current of other components in a handheld system. Increasing the R_{VB} value reduces the worst-case current but at the same time increases the error for the 4.34V battery OVP threshold.

The battery OVP threshold error is the original accuracy at the VB pin given in the “Electrical Specifications” table on page 4, plus the voltage built across R_{VB} by the VB pin leakage current. The VB pin leakage current is less than 20nA, as given in the “Electrical Specifications” table on page 4. With a 200k Ω resistor, the worst-case additional error is 4mV; with a 1M Ω resistor, the worst-case additional error is 20mV.

Capacitor Selection

The input capacitor (C_1 in the “TYPICAL APPLICATION CIRCUIT” on page 1) is for decoupling. A higher value reduces the voltage drop or the over-shoot during transients.

Two scenarios can cause input voltage over-shoot. The first one is when the AC adapter is inserted live (hot insertion). The second one is when the current in the power NFET of the ISL9211B has a step-down change. Figure 16 shows an equivalent circuit for the ISL9211B input. The cable between the AC/DC converter output and the handheld system input has a parasitic inductor. The parasitic resistor is the sum of various components, such as the cable, the adapter output capacitor ESR, the connector contact resistance, and so on.

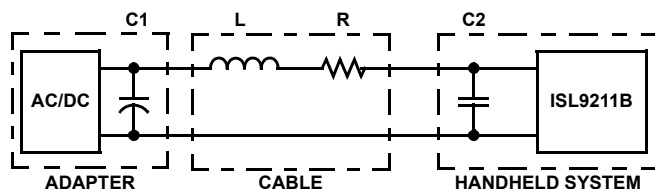


FIGURE 16. EQUIVALENT CIRCUIT FOR ISL9211B INPUT

During the load current step-down transient, the energy stored in the parasitic inductor is used to charge the input decoupling capacitor, C_2 . The ISL9211B is designed to turn off the power NFET slowly during an OCP and battery OVP event. Because of this design, the input over-shoot during these events is not significant. During an input OVP, however, the NFET is turned in less than $1\mu\text{s}$ and can lead to significant over-shoot. Higher capacitance reduces the over-shoot.

Over-shoot caused by a hot insertion is not very dependent on the decoupling capacitance value, especially when ceramic type capacitors are used for decoupling. In theory, over-shoot can rise up to twice the DC output voltage of the AC adapter. Actual peak voltage is dependent on the damping factor that is mainly determined by parasitic resistance (R in Figure 16).

The recommended input decoupling capacitor is a 25V, X5R dielectric ceramic capacitor with a value between $0.1\mu\text{F}$ and $1\mu\text{F}$.

The output of the ISL9211B and the input of the charging circuit typically share one decoupling capacitor. Selection of that capacitor is determined mainly by the requirements of the charging circuit. When using the ISL6292 family of chargers, a $1\mu\text{F}$, 6.3V, X5R capacitor is recommended.

Layout Recommendation

The ISL9211B uses a thermally enhanced TDFN package with an exposed thermal pad at the bottom of the package. The layout should include as much copper as possible beneath the exposed pad on the component layer to improve thermal performance. The exposed pad under the package should be connected to the ground plane electrically as well as thermally. The vias should be about 0.3mm to 0.33mm in diameter. Use as many vias as will fit in the thermal pad area.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
November 4, 2014	FN7861.1	Updated Note 2 for the Ordering Information on page 3.
July 8, 2011	FN7861.0	Initial release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL9211B](http://www.intersil.com/ISL9211B)

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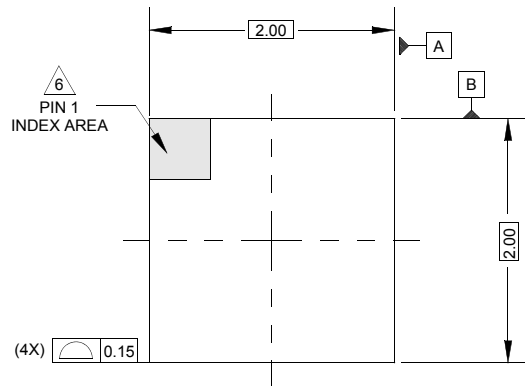
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Package Outline Drawing

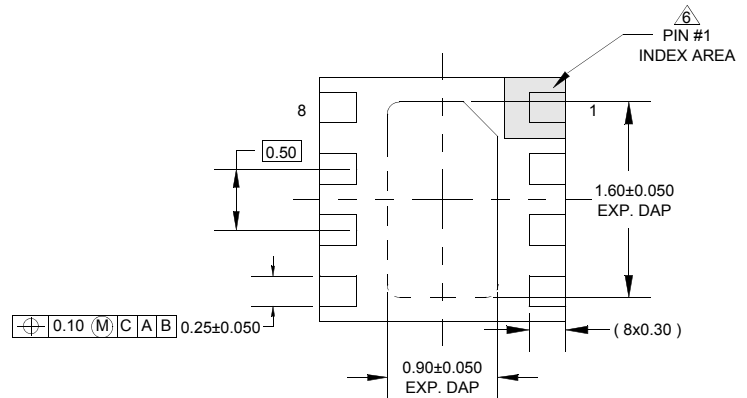
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8 LEAD MICRO THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (μ TDFN) WITH E-PAD

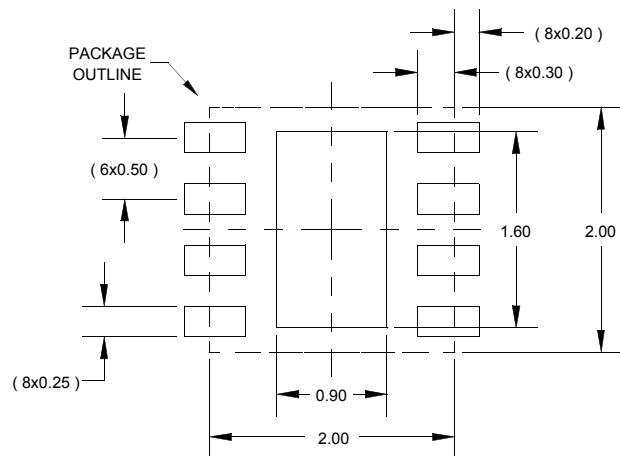
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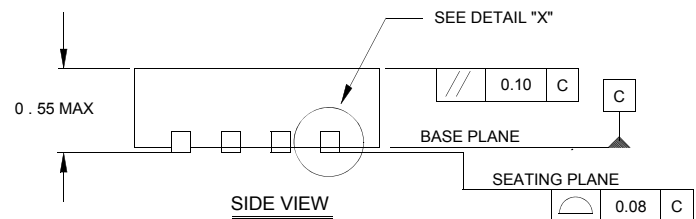
TOP VIEW



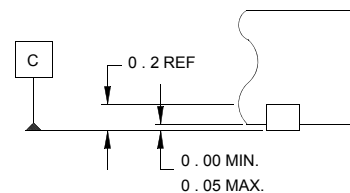
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.