

## FEATURES

- <1 pC charge injection over full signal range
- 1.5 pF off capacitance
- 33 V supply range
- 120  $\Omega$  on resistance
- Fully specified at  $\pm 15$  V/+12 V
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 28-lead TSSOP and 32-lead, 5 mm  $\times$  5 mm LFCSP

## APPLICATIONS

- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Communication systems

## GENERAL DESCRIPTION

The **ADG1206** and **ADG1207** are monolithic *i*CMOS<sup>®</sup> analog multiplexers comprising sixteen single channels and eight differential channels, respectively. The **ADG1206** switches one of sixteen inputs to a common output, as determined by the 4-bit binary address lines A0, A1, A2, and A3. The **ADG1207** switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines A0, A1, and A2. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off. When on, each channel conducts equally well in both directions and has an input signal range that extends to the supplies.

The industrial CMOS (*i*CMOS) modular manufacturing process combines high voltage, complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage devices has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

## FUNCTIONAL BLOCK DIAGRAMS

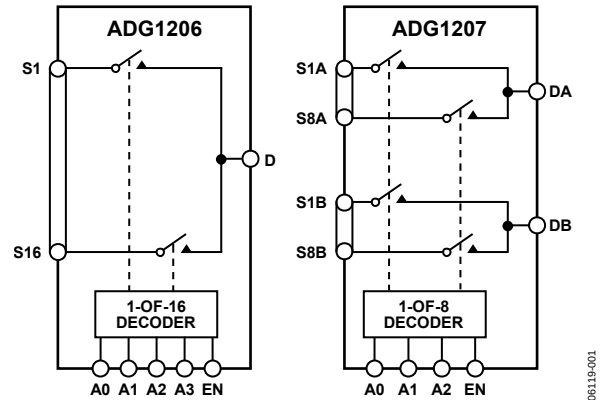


Figure 1.

The ultralow capacitance and exceptionally low charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Figure 2 shows that there is minimum charge injection over the entire signal range of the device. *i*CMOS construction also ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

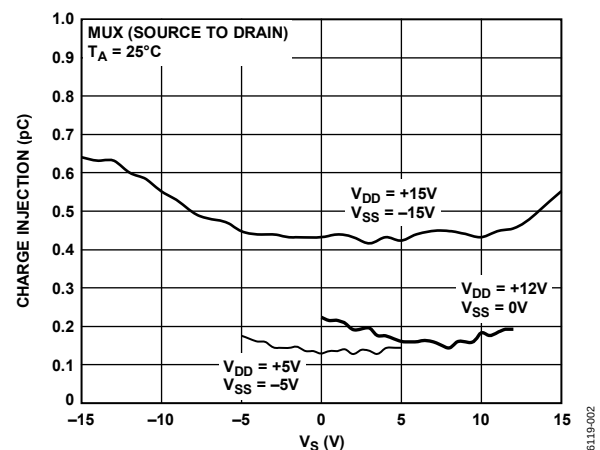


Figure 2. Source-to-Drain Charge Injection vs. Source Voltage

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## REVISION HISTORY

### 6/2016—Rev. B to Rev. C

|                                                   |   |
|---------------------------------------------------|---|
| Changes to Analog Inputs Parameter, Table 3 ..... | 7 |
| Added Digital Inputs Parameter, Table 3 .....     | 7 |

### 4/2016—Rev. A to Rev. B

|                                                  |            |
|--------------------------------------------------|------------|
| Changed CP-32-2 to CP-32-7 .....                 | Throughout |
| Changes to Figure 3, Figure 4, and Table 4 ..... | 8          |
| Changes to Figure 5, Figure 6, and Table 6 ..... | 10         |
| Updated Outline Dimensions .....                 | 20         |
| Changes to Ordering Guide .....                  | 20         |

### 3/2009—Rev. 0 to Rev. A

|                                             |    |
|---------------------------------------------|----|
| Change to $I_{DD}$ Parameter, Table 1 ..... | 4  |
| Change to $I_{DD}$ Parameter, Table 2 ..... | 6  |
| Updated Outline Dimensions .....            | 19 |
| Changes to Ordering Guide .....             | 19 |

### 7/2006—Revision 0: Initial Version

## SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V, unless otherwise noted.<sup>1</sup>

Table 1.

| Parameter                                             | +25°C       | –40°C to<br>+85°C | –40°C to<br>+125°C   | Unit              | Test Conditions/Comments                                                                            |
|-------------------------------------------------------|-------------|-------------------|----------------------|-------------------|-----------------------------------------------------------------------------------------------------|
| ANALOG SWITCH                                         |             |                   |                      |                   |                                                                                                     |
| Analog Signal Range                                   |             |                   | $V_{SS}$ to $V_{DD}$ | V                 |                                                                                                     |
| On Resistance, $R_{ON}$                               | 120         |                   |                      | $\Omega$ typ      | $V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 28                                      |
|                                                       | 200         | 240               | 270                  | $\Omega$ max      | $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$                                               |
| On-Resistance Match Between Channels, $\Delta R_{ON}$ | 3.5         |                   |                      | $\Omega$ typ      | $V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$                                                      |
|                                                       | 6           | 10                | 12                   | $\Omega$ max      |                                                                                                     |
| On-Resistance Flatness, $R_{FLAT}$ (On)               | 20          |                   |                      | $\Omega$ typ      | $V_S = -5\text{ V}, 0\text{ V}, +5\text{ V}$ ; $I_S = -1\text{ mA}$                                 |
|                                                       | 64          | 76                | 83                   | $\Omega$ max      |                                                                                                     |
| LEAKAGE CURRENTS                                      |             |                   |                      |                   |                                                                                                     |
| Source Off Leakage, $I_S$ (Off)                       | $\pm 0.03$  |                   |                      | nA typ            | $V_D = \pm 10\text{ V}$ , $V_S = \mp 10\text{ V}$ ; see Figure 29                                   |
|                                                       | $\pm 0.2$   | $\pm 0.6$         | $\pm 1$              | nA max            |                                                                                                     |
| Drain Off Leakage, $I_D$ (Off)                        | $\pm 0.05$  |                   |                      | nA typ            | $V_S = 1\text{ V}, 10\text{ V}$ ; $V_D = 10\text{ V}, 1\text{ V}$ ; see Figure 29                   |
|                                                       | $\pm 0.2$   | $\pm 0.6$         | $\pm 2$              | nA max            |                                                                                                     |
| Channel On Leakage, $I_D, I_S$ (On)                   | $\pm 0.08$  |                   |                      | nA typ            | $V_S = V_D = \pm 10\text{ V}$ ; see Figure 30                                                       |
|                                                       | $\pm 0.2$   | $\pm 0.6$         | $\pm 2$              | nA max            |                                                                                                     |
| DIGITAL INPUTS                                        |             |                   |                      |                   |                                                                                                     |
| Input High Voltage, $V_{INH}$                         |             |                   | 2.0                  | V min             |                                                                                                     |
| Input Low Voltage, $V_{INL}$                          |             |                   | 0.8                  | V max             |                                                                                                     |
| Input Current, $I_{INL}$ or $I_{INH}$                 | $\pm 0.005$ |                   |                      | $\mu\text{A}$ typ | $V_{IN} = V_{INL}$ or $V_{INH}$                                                                     |
|                                                       |             |                   | $\pm 0.1$            | $\mu\text{A}$ max |                                                                                                     |
| Digital Input Capacitance, $C_{IN}$                   | 2           |                   |                      | pF typ            |                                                                                                     |
| DYNAMIC CHARACTERISTICS <sup>2</sup>                  |             |                   |                      |                   |                                                                                                     |
| Transition Time, $t_{TRANSITION}$                     | 80          |                   |                      | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                                          |
|                                                       | 130         | 165               | 185                  | ns max            | $V_S = 10\text{ V}$ ; see Figure 31                                                                 |
| $t_{ON}$ (EN)                                         | 75          |                   |                      | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                                          |
|                                                       | 95          | 105               | 115                  | ns max            | $V_S = 10\text{ V}$ ; see Figure 33                                                                 |
| $t_{OFF}$ (EN)                                        | 85          |                   |                      | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                                          |
|                                                       | 100         | 125               | 140                  | ns max            | $V_S = 10\text{ V}$ ; see Figure 33                                                                 |
| Break-Before-Make Time Delay, $t_{BBM}$               | 20          |                   |                      | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                                          |
|                                                       |             |                   | 10                   | ns min            | $V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 32                                                     |
| Charge Injection                                      | 0.5         |                   |                      | pC typ            | $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 34                        |
| Off Isolation                                         | –85         |                   |                      | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 35                       |
| Channel-to-Channel Crosstalk                          | –85         |                   |                      | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 37                       |
| Total Harmonic Distortion Plus Noise                  | 0.15        |                   |                      | % typ             | $R_L = 10\text{ k}\Omega$ , $5\text{ V rms}$ , $f = 20\text{ Hz to } 20\text{ kHz}$ ; see Figure 38 |
| –3 dB Bandwidth, <a href="#">ADG1206</a>              | 280         |                   |                      | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 36                                            |
| –3 dB Bandwidth, <a href="#">ADG1207</a>              | 490         |                   |                      | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 36                                            |
| $C_S$ (Off)                                           | 1.5         |                   |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                                             |
|                                                       | 2           |                   |                      | pF max            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                                             |
| $C_D$ (Off), <a href="#">ADG1206</a>                  | 11          |                   |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                                             |
|                                                       | 12          |                   |                      | pF max            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                                             |
| $C_D$ (Off), <a href="#">ADG1207</a>                  | 7           |                   |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                                             |
|                                                       | 9           |                   |                      | pF max            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                                             |

| Parameter                                | +25°C | –40°C to<br>+85°C | –40°C to<br>+125°C | Unit                                   | Test Conditions/Comments                             |
|------------------------------------------|-------|-------------------|--------------------|----------------------------------------|------------------------------------------------------|
| $C_D, C_S$ (On), <a href="#">ADG1206</a> | 13    |                   |                    | pF typ                                 | $f = 1 \text{ MHz}, V_S = 0 \text{ V}$               |
|                                          | 15    |                   |                    | pF max                                 | $f = 1 \text{ MHz}, V_S = 0 \text{ V}$               |
| $C_D, C_S$ (On), <a href="#">ADG1207</a> | 8     |                   |                    | pF typ                                 | $f = 1 \text{ MHz}, V_S = 0 \text{ V}$               |
|                                          | 10    |                   |                    | pF max                                 | $f = 1 \text{ MHz}, V_S = 0 \text{ V}$               |
| POWER REQUIREMENTS                       |       |                   |                    |                                        | $V_{DD} = +16.5 \text{ V}, V_{SS} = -16.5 \text{ V}$ |
| $I_{DD}$                                 | 0.002 |                   | 1.0                | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 0 V or $V_{DD}$                     |
| $I_{DD}$                                 | 260   |                   | 475                | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 5 V                                 |
| $I_{SS}$                                 | 0.002 |                   | 1.0                | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 0 V, 5 V, or $V_{DD}$               |
| $V_{DD}/V_{SS}$                          |       |                   | $\pm 5/\pm 16.5$   | V min/max                              | GND = 0V                                             |

<sup>1</sup> Temperature range for Y version is –40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

**SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.<sup>1</sup>

**Table 2.**

| Parameter                                             | +25°C       | −40°C to<br>+85°C | −40°C to<br>+125°C | Unit              | Test Conditions/Comments                                                        |
|-------------------------------------------------------|-------------|-------------------|--------------------|-------------------|---------------------------------------------------------------------------------|
| <b>ANALOG SWITCH</b>                                  |             |                   |                    |                   |                                                                                 |
| Analog Signal Range                                   |             |                   | 0 to $V_{DD}$      | V                 |                                                                                 |
| On Resistance, $R_{ON}$                               | 300         |                   |                    | $\Omega$ typ      | $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 28      |
|                                                       | 475         | 567               | 625                | $\Omega$ max      | $V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$                                |
| On-Resistance Match Between Channels, $\Delta R_{ON}$ | 5           |                   |                    | $\Omega$ typ      | $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -1\text{ mA}$                      |
|                                                       | 16          | 26                | 27                 | $\Omega$ max      |                                                                                 |
| On-Resistance Flatness, $R_{FLAT}$ (On)               | 60          |                   |                    | $\Omega$ typ      | $V_S = 3\text{ V}$ , $6\text{ V}$ , $9\text{ V}$ ; $I_S = -1\text{ mA}$         |
| <b>LEAKAGE CURRENTS</b>                               |             |                   |                    |                   |                                                                                 |
| Source Off Leakage, $I_S$ (Off)                       | $\pm 0.02$  |                   |                    | nA typ            | $V_{DD} = 13.2\text{ V}$                                                        |
|                                                       | $\pm 0.2$   | $\pm 0.6$         | $\pm 1$            | nA max            | $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 29 |
| Drain Off Leakage, $I_D$ (Off)                        | $\pm 0.05$  |                   |                    | nA typ            | $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 29 |
|                                                       | $\pm 0.2$   | $\pm 0.6$         | $\pm 2$            | nA max            |                                                                                 |
| Channel On Leakage, $I_D$ , $I_S$ (On)                | $\pm 0.08$  |                   |                    | nA typ            | $V_S = V_D = 1\text{ V}$ or $10\text{ V}$ ; see Figure 30                       |
|                                                       | $\pm 0.2$   | $\pm 0.6$         | $\pm 2$            | nA max            |                                                                                 |
| <b>DIGITAL INPUTS</b>                                 |             |                   |                    |                   |                                                                                 |
| Input High Voltage, $V_{INH}$                         |             |                   | 2.0                | V min             |                                                                                 |
| Input Low Voltage, $V_{INL}$                          |             |                   | 0.8                | V max             |                                                                                 |
| Input Current, $I_{INL}$ or $I_{INH}$                 | $\pm 0.001$ |                   |                    | $\mu\text{A}$ typ | $V_{IN} = V_{INL}$ or $V_{INH}$                                                 |
|                                                       |             |                   | $\pm 0.1$          | $\mu\text{A}$ max |                                                                                 |
| Digital Input Capacitance, $C_{IN}$                   | 3           |                   |                    | pF typ            |                                                                                 |
| <b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>            |             |                   |                    |                   |                                                                                 |
| Transition Time, $t_{TRANSITION}$                     | 100         |                   |                    | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 140         | 175               | 200                | ns max            | $V_S = 8\text{ V}$ ; see Figure 31                                              |
| $t_{ON}$ (EN)                                         | 80          |                   |                    | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 100         | 120               | 130                | ns max            | $V_S = 8\text{ V}$ ; see Figure 33                                              |
| $t_{OFF}$ (EN)                                        | 90          |                   |                    | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 110         | 130               | 155                | ns max            | $V_S = 8\text{ V}$ ; see Figure 33                                              |
| Break-Before-Make Time Delay, $t_{BBM}$               | 25          |                   |                    | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       |             |                   | 15                 | ns min            | $V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 32                                  |
| Charge Injection                                      | 0.2         |                   |                    | pC typ            | $V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 34    |
| Off Isolation                                         | −85         |                   |                    | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 35   |
| Channel-to-Channel Crosstalk                          | −85         |                   |                    | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 37   |
| −3 dB Bandwidth, <a href="#">ADG1206</a>              | 185         |                   |                    | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 36                        |
| −3 dB Bandwidth, <a href="#">ADG1207</a>              | 300         |                   |                    | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 36                        |
| $C_S$ (Off)                                           | 1.5         |                   |                    | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
|                                                       | 2           |                   |                    | pF max            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| $C_D$ (Off), <a href="#">ADG1206</a>                  | 13          |                   |                    | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
|                                                       | 15          |                   |                    | pF max            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| $C_D$ (Off), <a href="#">ADG1207</a>                  | 9           |                   |                    | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
|                                                       | 11          |                   |                    | pF max            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| $C_D$ , $C_S$ (On), <a href="#">ADG1206</a>           | 15          |                   |                    | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
|                                                       | 17          |                   |                    | pF max            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| $C_D$ , $C_S$ (On), <a href="#">ADG1207</a>           | 10          |                   |                    | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
|                                                       | 12          |                   |                    | pF max            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |

| Parameter          | +25°C | –40°C to<br>+85°C | –40°C to<br>+125°C | Unit                                   | Test Conditions/Comments          |
|--------------------|-------|-------------------|--------------------|----------------------------------------|-----------------------------------|
| POWER REQUIREMENTS |       |                   |                    |                                        | $V_{DD} = 13.2\text{ V}$          |
| $I_{DD}$           | 0.002 |                   | 1.0                | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 0 V or $V_{DD}$  |
| $I_{DD}$           | 260   |                   | 475                | $\mu\text{A typ}$<br>$\mu\text{A max}$ | Digital inputs = 5 V              |
| $V_{DD}$           |       |                   | 5/16.5             | V min/max                              | $V_{SS} = 0\text{ V}$ , GND = 0 V |

<sup>1</sup> Temperature range for Y version is –40°C to +125°C.<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

| Parameter                                                     | Rating                                                                                 |
|---------------------------------------------------------------|----------------------------------------------------------------------------------------|
| $V_{DD}$ to $V_{SS}$                                          | 35 V                                                                                   |
| $V_{DD}$ to GND                                               | −0.3 V to +25 V                                                                        |
| $V_{SS}$ to GND                                               | +0.3 V to −25 V                                                                        |
| Analog Inputs <sup>1</sup>                                    | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$<br>or 30 mA, whichever occurs first |
| Digital Inputs <sup>1</sup>                                   | GND − 0.3 V to $V_{DD} + 0.3\text{ V}$<br>or 30 mA, whichever occurs first             |
| Continuous Current, S or D                                    | 30 mA                                                                                  |
| Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum) | 100 mA                                                                                 |
| Operating Temperature Range                                   |                                                                                        |
| Industrial (Y Version)                                        | −40°C to +125°C                                                                        |
| Storage                                                       | −65°C to +150°C                                                                        |
| Junction Temperature                                          | 150°C                                                                                  |
| Thermal Impedance                                             |                                                                                        |
| 28-Lead TSSOP                                                 |                                                                                        |
| $\theta_{JA}$                                                 | 97.9°C/W                                                                               |
| $\theta_{JC}$                                                 | 14°C/W                                                                                 |
| 32-Lead LFCSP                                                 |                                                                                        |
| $\theta_{JA}$                                                 | 27.27°C/W                                                                              |
| Reflow Soldering Peak Temperature (RoHS Compliant)            | 260(+0/−5)°C                                                                           |

<sup>1</sup> Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

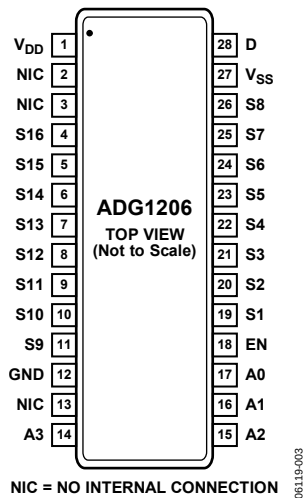


Figure 3. 28-Lead TSSOP Pin Configuration (ADG1206)

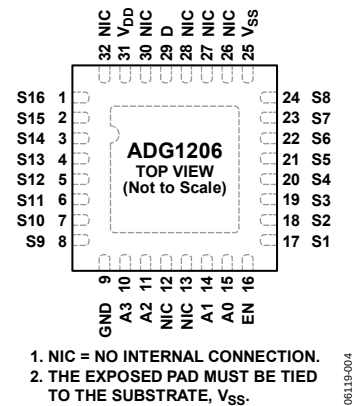


Figure 4. 32-Lead LFCSP Pin Configuration (ADG1206)

Table 4. ADG1206 Pin Function Descriptions

| Pin No.        |                            | Mnemonic | Description                                                                                                                                                                              |
|----------------|----------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSSOP          | LFCSP                      |          |                                                                                                                                                                                          |
| 1              | 31                         | $V_{DD}$ | Most Positive Power Supply Potential.                                                                                                                                                    |
| 2, 3, 13       | 12, 13, 26, 27, 28, 30, 32 | NIC      | No Internal Connection.                                                                                                                                                                  |
| 4              | 1                          | S16      | Source Terminal 16. Can be an input or an output.                                                                                                                                        |
| 5              | 2                          | S15      | Source Terminal 15. Can be an input or an output.                                                                                                                                        |
| 6              | 3                          | S14      | Source Terminal 14. Can be an input or an output.                                                                                                                                        |
| 7              | 4                          | S13      | Source Terminal 13. Can be an input or an output.                                                                                                                                        |
| 8              | 5                          | S12      | Source Terminal 12. Can be an input or an output.                                                                                                                                        |
| 9              | 6                          | S11      | Source Terminal 11. Can be an input or an output.                                                                                                                                        |
| 10             | 7                          | S10      | Source Terminal 10. Can be an input or an output.                                                                                                                                        |
| 11             | 8                          | S9       | Source Terminal 9. Can be an input or an output.                                                                                                                                         |
| 12             | 9                          | GND      | Ground (0 V) Reference.                                                                                                                                                                  |
| 14             | 10                         | A3       | Logic Control Input.                                                                                                                                                                     |
| 15             | 11                         | A2       | Logic Control Input.                                                                                                                                                                     |
| 16             | 14                         | A1       | Logic Control Input.                                                                                                                                                                     |
| 17             | 15                         | A0       | Logic Control Input.                                                                                                                                                                     |
| 18             | 16                         | EN       | Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on. |
| 19             | 17                         | S1       | Source Terminal 1. Can be an input or an output.                                                                                                                                         |
| 20             | 18                         | S2       | Source Terminal 2. Can be an input or an output.                                                                                                                                         |
| 21             | 19                         | S3       | Source Terminal 3. Can be an input or an output.                                                                                                                                         |
| 22             | 20                         | S4       | Source Terminal 4. Can be an input or an output.                                                                                                                                         |
| 23             | 21                         | S5       | Source Terminal 5. Can be an input or an output.                                                                                                                                         |
| 24             | 22                         | S6       | Source Terminal 6. Can be an input or an output.                                                                                                                                         |
| 25             | 23                         | S7       | Source Terminal 7. Can be an input or an output.                                                                                                                                         |
| 26             | 24                         | S8       | Source Terminal 8. Can be an input or an output.                                                                                                                                         |
| 27             | 25                         | $V_{SS}$ | Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.                                                                                |
| 28             | 29                         | D        | Drain Terminal. Can be an input or an output.                                                                                                                                            |
| Not applicable | 0                          | EPAD     | Exposed Pad. The exposed pad must be tied to the substrate, $V_{SS}$ .                                                                                                                   |



Table 5. [ADG1206](#) Truth Table

| A3 | A2 | A1 | A0 | EN | On Switch |
|----|----|----|----|----|-----------|
| X  | X  | X  | X  | 0  | None      |
| 0  | 0  | 0  | 0  | 1  | 1         |
| 0  | 0  | 0  | 1  | 1  | 2         |
| 0  | 0  | 1  | 0  | 1  | 3         |
| 0  | 0  | 1  | 1  | 1  | 4         |
| 0  | 1  | 0  | 0  | 1  | 5         |
| 0  | 1  | 0  | 1  | 1  | 6         |
| 0  | 1  | 1  | 0  | 1  | 7         |
| 0  | 1  | 1  | 1  | 1  | 8         |
| 1  | 0  | 0  | 0  | 1  | 9         |
| 1  | 0  | 0  | 1  | 1  | 10        |
| 1  | 0  | 1  | 0  | 1  | 11        |
| 1  | 0  | 1  | 1  | 1  | 12        |
| 1  | 1  | 0  | 0  | 1  | 13        |
| 1  | 1  | 0  | 1  | 1  | 14        |
| 1  | 1  | 1  | 0  | 1  | 15        |
| 1  | 1  | 1  | 1  | 1  | 16        |

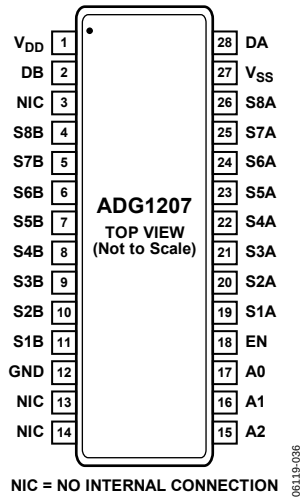


Figure 5. 28-Lead TSSOP Pin Configuration (ADG1207)

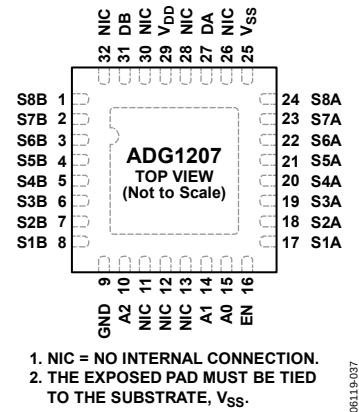


Figure 6. 32-Lead LFCSP Pin Configuration (ADG1207)

Table 6. ADG1207 Pin Function Descriptions

| Pin No.        |                            | Mnemonic | Description                                                                                                                                                                              |
|----------------|----------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TSSOP          | LFCSP                      |          |                                                                                                                                                                                          |
| 1              | 29                         | $V_{DD}$ | Most Positive Power Supply Potential.                                                                                                                                                    |
| 2              | 31                         | DB       | Drain Terminal B. Can be an input or an output.                                                                                                                                          |
| 3, 13, 14      | 11, 12, 13, 26, 28, 30, 32 | NIC      | No Internal Connection.                                                                                                                                                                  |
| 4              | 1                          | S8B      | Source Terminal 8B. Can be an input or an output.                                                                                                                                        |
| 5              | 2                          | S7B      | Source Terminal 7B. Can be an input or an output.                                                                                                                                        |
| 6              | 3                          | S6B      | Source Terminal 6B. Can be an input or an output.                                                                                                                                        |
| 7              | 4                          | S5B      | Source Terminal 5B. Can be an input or an output.                                                                                                                                        |
| 8              | 5                          | S4B      | Source Terminal 4B. Can be an input or an output.                                                                                                                                        |
| 9              | 6                          | S3B      | Source Terminal 3B. Can be an input or an output.                                                                                                                                        |
| 10             | 7                          | S2B      | Source Terminal 2B. Can be an input or an output.                                                                                                                                        |
| 11             | 8                          | S1B      | Source Terminal 1B. Can be an input or an output.                                                                                                                                        |
| 12             | 9                          | GND      | Ground (0 V) Reference.                                                                                                                                                                  |
| 15             | 10                         | A2       | Logic Control Input.                                                                                                                                                                     |
| 16             | 14                         | A1       | Logic Control Input.                                                                                                                                                                     |
| 17             | 15                         | A0       | Logic Control Input.                                                                                                                                                                     |
| 18             | 16                         | EN       | Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on. |
| 19             | 17                         | S1A      | Source Terminal 1A. Can be an input or an output.                                                                                                                                        |
| 20             | 18                         | S2A      | Source Terminal 2A. Can be an input or an output.                                                                                                                                        |
| 21             | 19                         | S3A      | Source Terminal 3A. Can be an input or an output.                                                                                                                                        |
| 22             | 20                         | S4A      | Source Terminal 4A. Can be an input or an output.                                                                                                                                        |
| 23             | 21                         | S5A      | Source Terminal 5A. Can be an input or an output.                                                                                                                                        |
| 24             | 22                         | S6A      | Source Terminal 6A. Can be an input or an output.                                                                                                                                        |
| 25             | 23                         | S7A      | Source Terminal 7A. Can be an input or an output.                                                                                                                                        |
| 26             | 24                         | S8A      | Source Terminal 8A. Can be an input or an output.                                                                                                                                        |
| 27             | 25                         | $V_{SS}$ | Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.                                                                                |
| 28             | 27                         | DA       | Drain Terminal A. Can be an input or an output.                                                                                                                                          |
| Not applicable | 0                          | EPAD     | Exposed Pad. The exposed pad must be tied to the substrate, $V_{SS}$ .                                                                                                                   |

Table 7. [ADG1207](#) Truth Table

| A2 | A1 | A0 | EN | On Switch Pair |
|----|----|----|----|----------------|
| X  | X  | X  | 0  | None           |
| 0  | 0  | 0  | 1  | 1              |
| 0  | 0  | 1  | 1  | 2              |
| 0  | 1  | 0  | 1  | 3              |
| 0  | 1  | 1  | 1  | 4              |
| 1  | 0  | 0  | 1  | 5              |
| 1  | 0  | 1  | 1  | 6              |
| 1  | 1  | 0  | 1  | 7              |
| 1  | 1  | 1  | 1  | 8              |

## TYPICAL PERFORMANCE CHARACTERISTICS

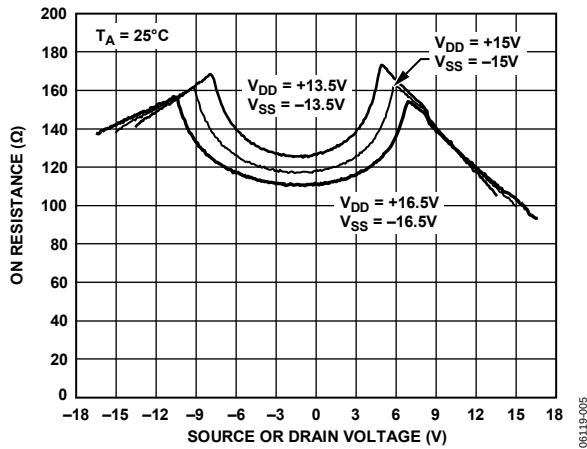
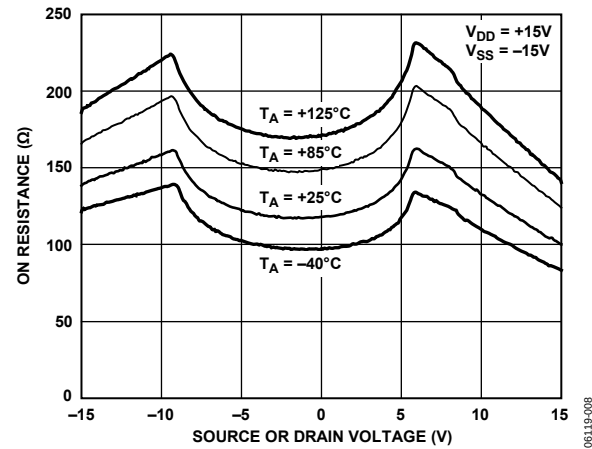
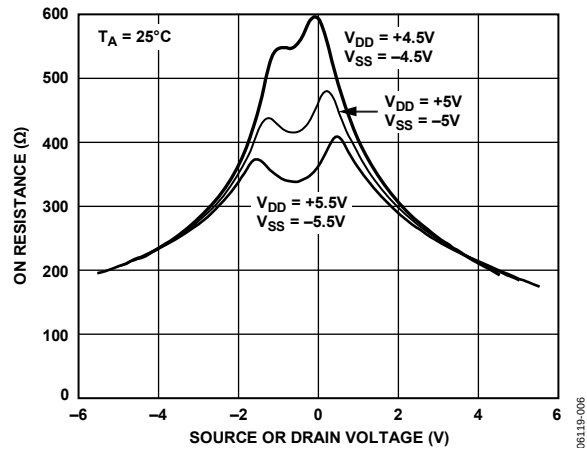
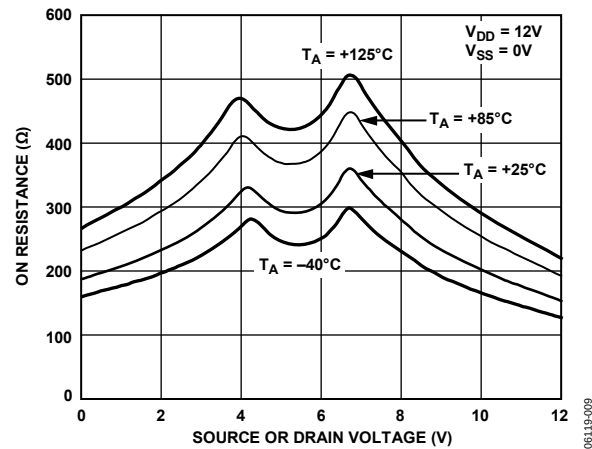
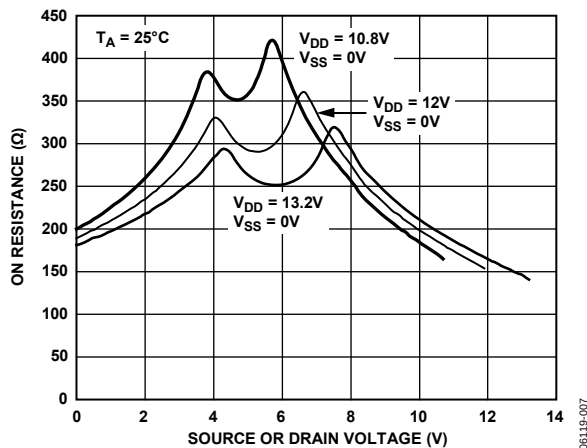
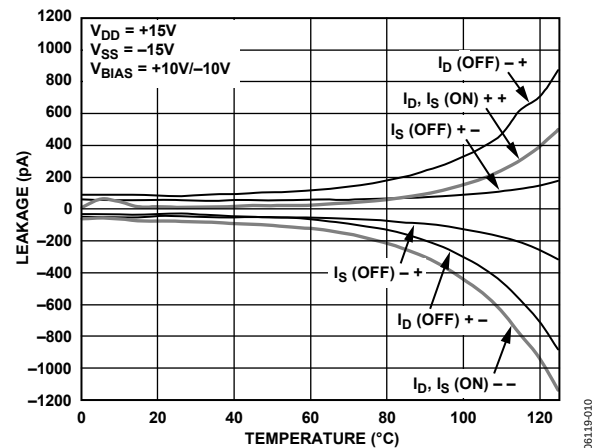
Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual SupplyFigure 10. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Dual SupplyFigure 8. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual SupplyFigure 11. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single SupplyFigure 9. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

Figure 12. ADG1206 Leakage Currents as a Function of Temperature, Dual Supply

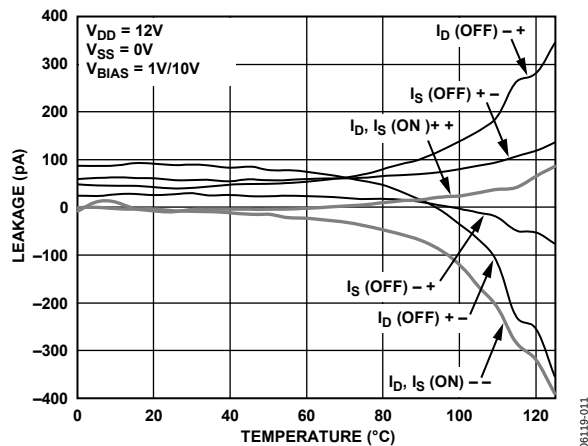


Figure 13. ADG1206 Leakage Currents as a Function of Temperature, Single Supply

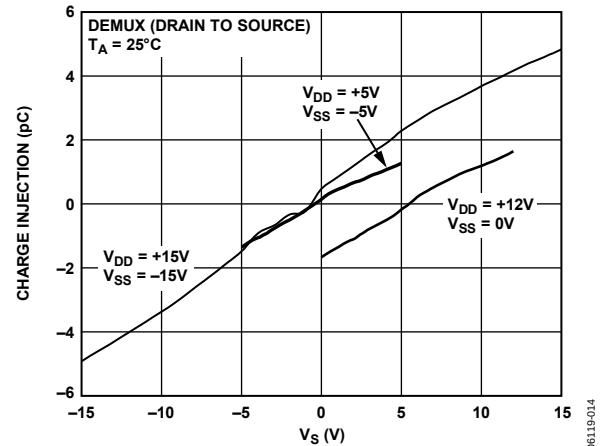


Figure 16. Drain-to-Source Charge Injection vs. Source Voltage

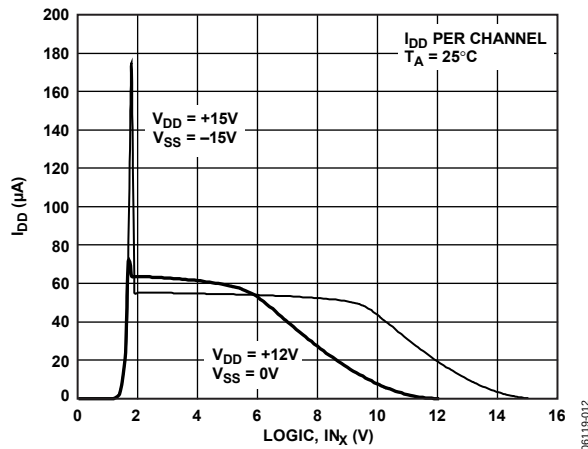


Figure 14.  $I_{DD}$  vs. Logic Level

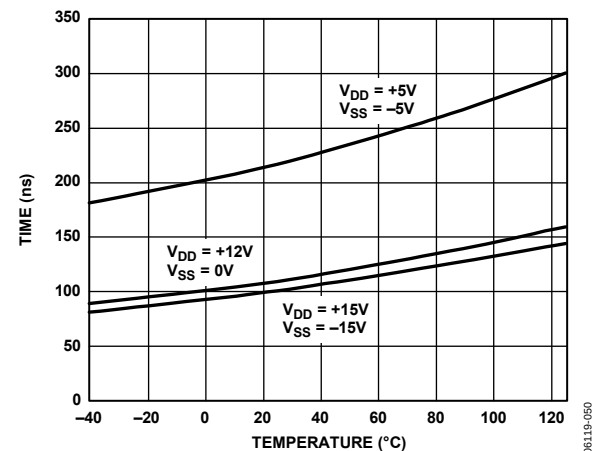


Figure 17. Transition Time vs. Temperature

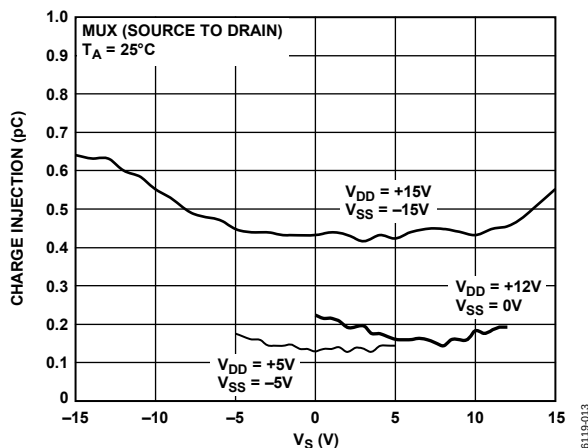


Figure 15. Source-to-Drain Charge Injection vs. Source Voltage

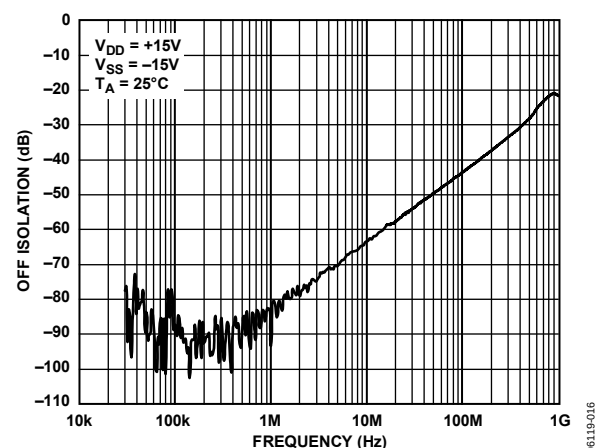


Figure 18. Off Isolation vs. Frequency

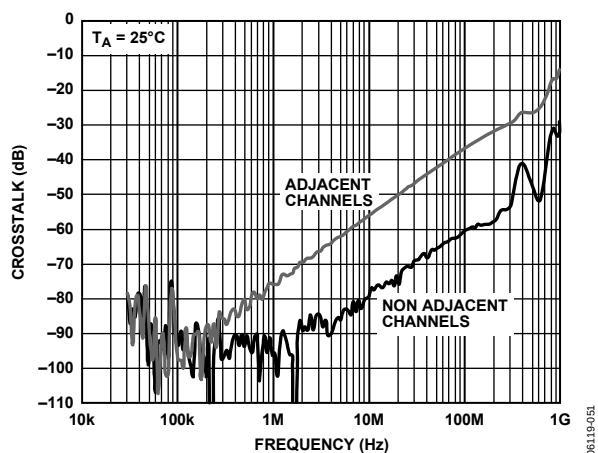


Figure 19. ADG1206 Crosstalk vs. Frequency

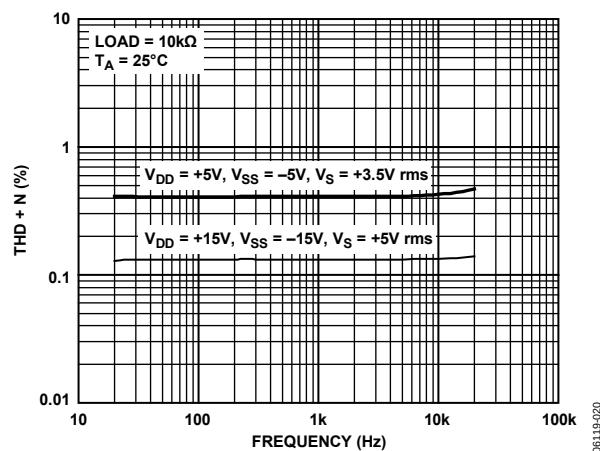


Figure 22. THD + N vs. Frequency

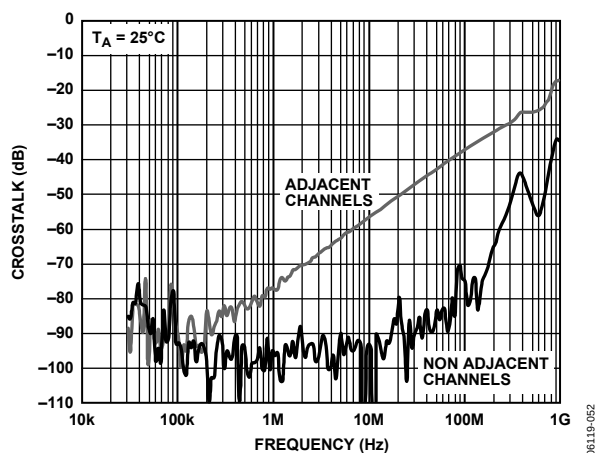


Figure 20. ADG1207 Crosstalk vs. Frequency

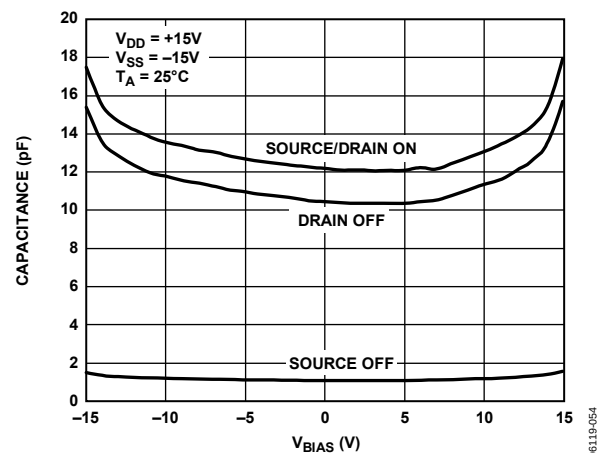


Figure 23. ADG1206 Capacitance vs. Source Voltage,  $\pm 15\text{V}$  Dual Supply

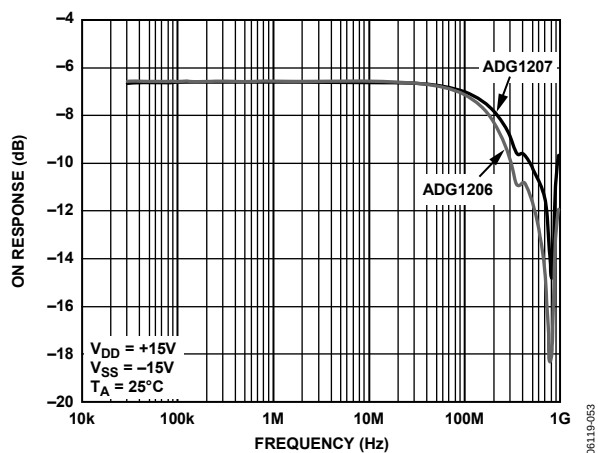


Figure 21. On Response vs. Frequency

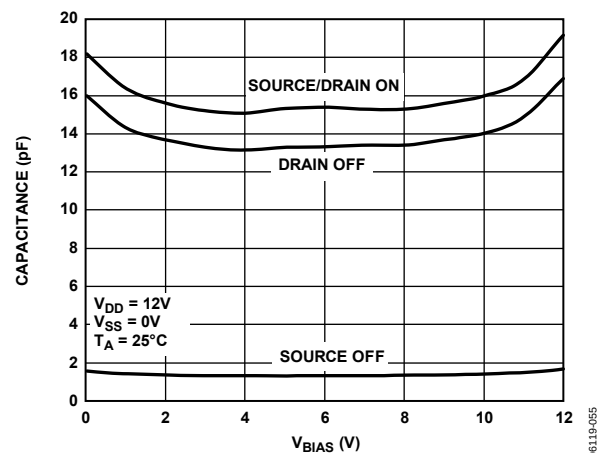


Figure 24. ADG1206 Capacitance vs. Source Voltage, 12 V Single Supply

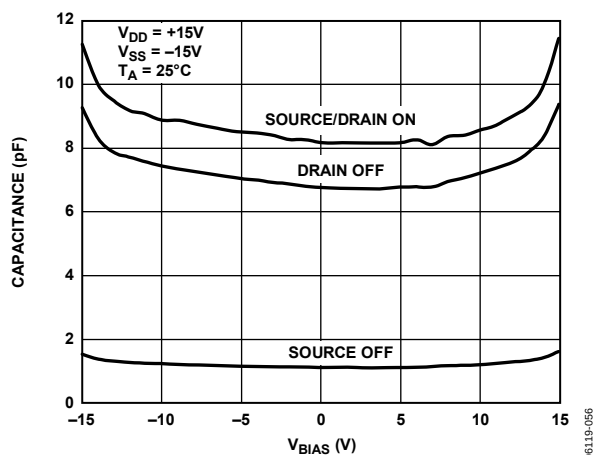
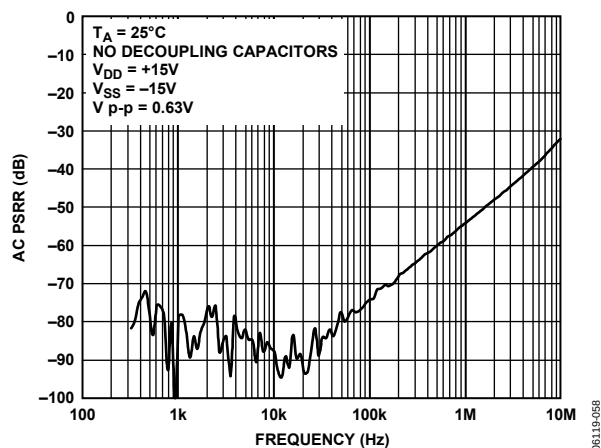
Figure 25. ADG1207 Capacitance vs. Source Voltage,  $\pm 15$  V Dual Supply

Figure 27. ACPSRR vs. Frequency

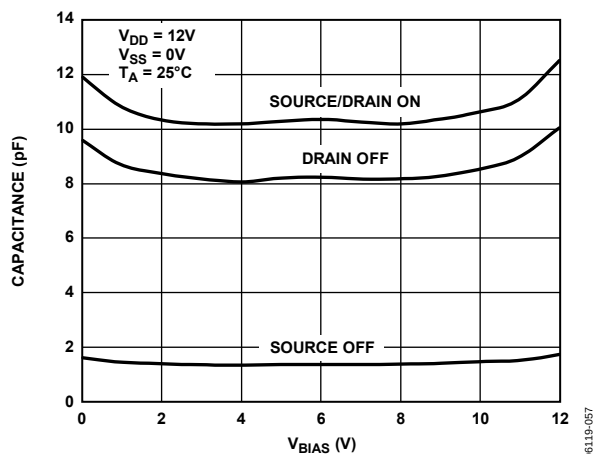


Figure 26. ADG1207 Capacitance vs. Source Voltage, 12 V Single Supply

## TERMINOLOGY

### **R<sub>ON</sub>**

Ohmic resistance between D and S.

### **ΔR<sub>ON</sub>**

Difference between the R<sub>ON</sub> of any two channels.

### **R<sub>FLAT(ON)</sub>**

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

### **I<sub>S</sub> (Off)**

Source leakage current when the switch is off.

### **I<sub>D</sub> (Off)**

Drain leakage current when the switch is off.

### **I<sub>D</sub>, I<sub>S</sub> (On)**

Channel leakage current when the switch is on.

### **V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on Terminals D and S.

### **C<sub>S</sub> (Off)**

Channel input capacitance for the off condition.

### **C<sub>D</sub> (Off)**

Channel output capacitance for the off condition.

### **C<sub>D</sub>, C<sub>S</sub> (On)**

On switch capacitance.

### **C<sub>IN</sub>**

Digital input capacitance.

### **t<sub>ON</sub> (EN)**

Delay time between the 50% and 90% points of the digital input and the switch on condition.

### **t<sub>OFF</sub> (EN)**

Delay time between the 50% and 90% points of the digital input and the switch off condition.

### **t<sub>TRANSITION</sub>**

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

### **T<sub>BBM</sub>**

Off time measured between the 80% points of the switches when switching from one address state to another.

### **V<sub>INL</sub>**

Maximum input voltage for Logic 0.

### **V<sub>INH</sub>**

Minimum input voltage for Logic 1.

### **I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

### **I<sub>DD</sub>**

Positive supply current.

### **I<sub>SS</sub>**

Negative supply current.

### **Off Isolation**

A measure of unwanted signal coupling through an off channel.

### **Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

### **Bandwidth**

The frequency at which the output is attenuated by 3 dB.

### **On Response**

The frequency response of the on switch.

### **Total Harmonic Distortion Plus Noise (THD + N)**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

### **AC Power Supply Rejection Ratio (ACPSRR)**

Measures the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.



## TEST CIRCUITS

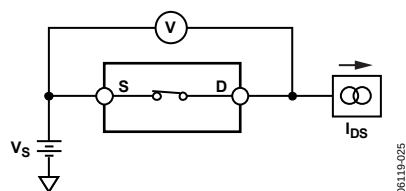


Figure 28. On Resistance

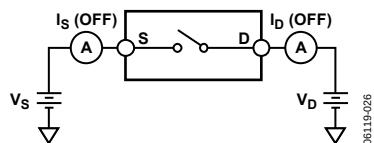


Figure 29. Off Leakage

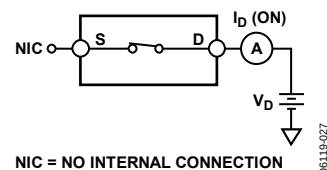
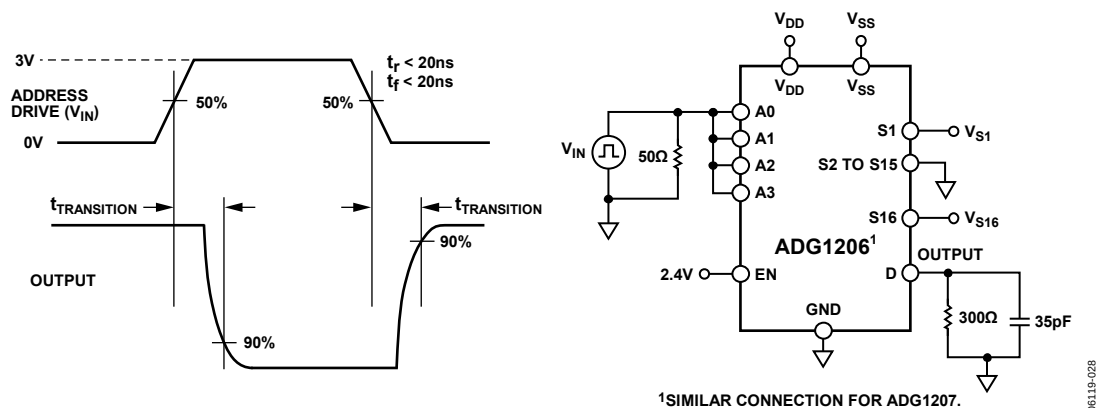
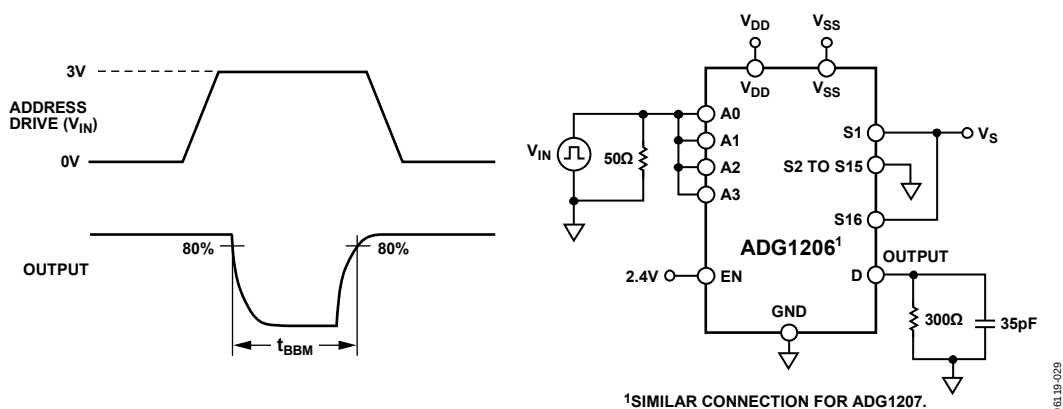
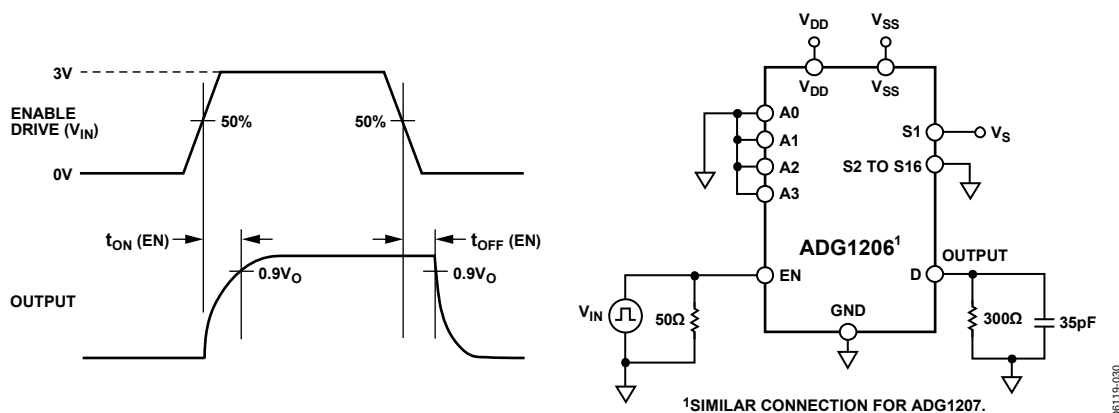
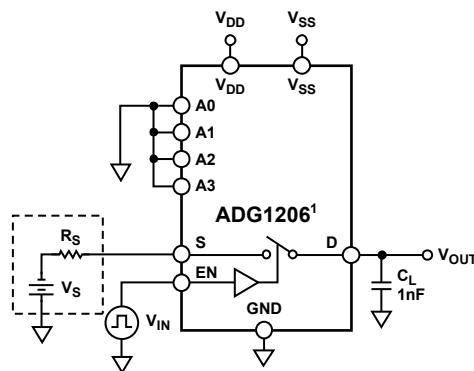
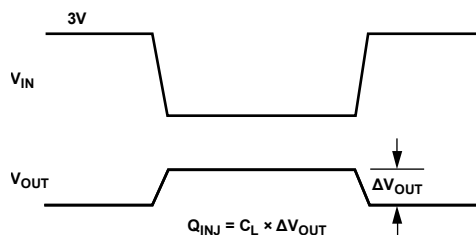


Figure 30. On Leakage

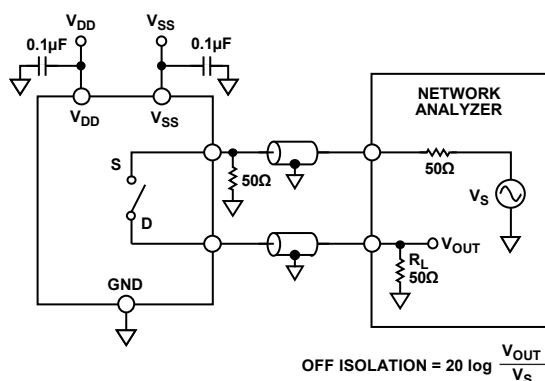
Figure 31. Address to Output Switching Times,  $t_{\text{TRANSITION}}$ Figure 32. Break-Before-Make Delay,  $t_{\text{BBM}}$ Figure 33. Enable Delay,  $t_{\text{ON}}(\text{EN})$ ,  $t_{\text{OFF}}(\text{EN})$



<sup>1</sup>SIMILAR CONNECTION FOR ADG1207.

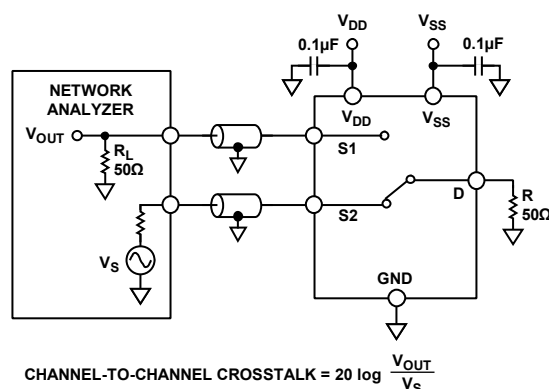
06119-031

Figure 34. Charge Injection



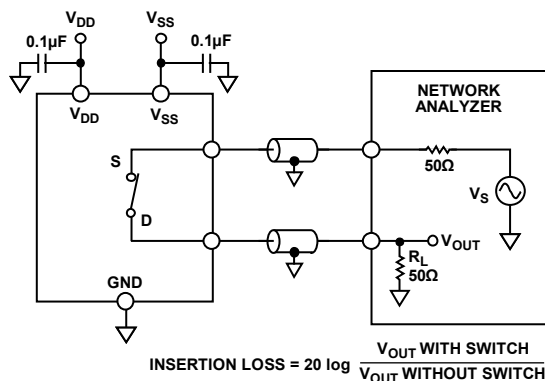
06119-032

Figure 35. Off Isolation



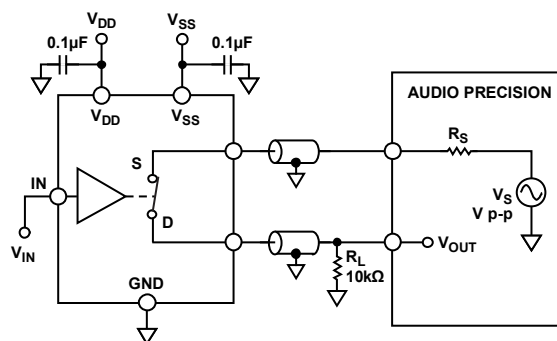
06119-034

Figure 37. Channel-to-Channel Crosstalk



06119-033

Figure 36. Bandwidth

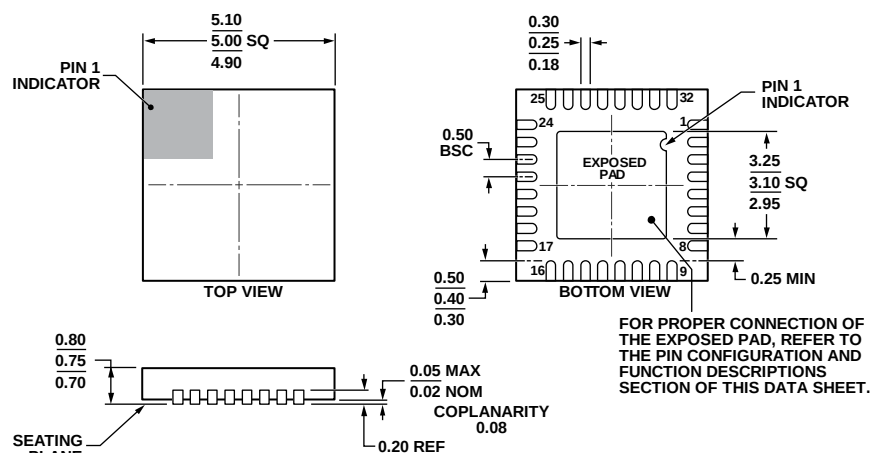


06119-035

Figure 38. THD + N

The drawing illustrates the mechanical specifications of a 28-pin PLCC package. The top view shows a rectangular body with pins on all four sides. Key dimensions include a total length of 9.80 mm, a body length of 9.70 mm, and a pin pitch of 0.65 mm. The body width is 6.40 mm BSC, with individual pin widths of 4.50 mm, 4.40 mm, and 4.30 mm. Pin numbers 1 through 28 are indicated. The side view shows a maximum height of 1.20 mm. The detail view shows a pin with a diameter of 0.20 mm, a thickness of 0.09 mm, and a lead angle of 8°/0°. Other detail dimensions include a coplanarity of 0.10 mm, a seating plane offset of 0.15 mm, and a pin thickness of 0.05 mm. Additional detail dimensions for the pin base are 0.30 mm, 0.19 mm, 0.75 mm, 0.60 mm, and 0.45 mm.

*Dimensions shown in millimeters*



*Dimensions shown in millimeters*

| Model <sup>1</sup> | Temperature Range | Description                                       | Package Option |
|--------------------|-------------------|---------------------------------------------------|----------------|
| ADG1206YRUZ        | −40°C to +125°C   | 28-Lead Thin Shrink Small Outline Package [TSSOP] | RU-28          |
| ADG1206YRUZ-REEL7  | −40°C to +125°C   | 28-Lead Thin Shrink Small Outline Package [TSSOP] | RU-28          |
| ADG1206YCPZ-REEL7  | −40°C to +125°C   | 32-Lead Lead Frame Chip Scale Package [LFCSP]     | CP-32-7        |
| ADG1207YRUZ        | −40°C to +125°C   | 28-Lead Thin Shrink Small Outline Package [TSSOP] | RU-28          |
| ADG1207YRUZ-REEL7  | −40°C to +125°C   | 28-Lead Thin Shrink Small Outline Package [TSSOP] | RU-28          |
| ADG1207YCPZ-REEL7  | −40°C to +125°C   | 32-Lead Lead Frame Chip Scale Package [LFCSP]     | CP-32-7        |

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**NOTES**