19-0389; Rev. 2; 9/96

MAXIM

Fault-Protected Analog Multiplexers

General Description

The MAX354/MAX355 fault-protected multiplexers (muxes) use a series N-channel, P-channel, N-channel structure that protects the devices from overvoltage up to 40V beyond the supply rails during power-up, power-down, and fault conditions. The MAX354/MAX355 also protect sensitive circuit components against voltages near or beyond the normal supplies.

The MAX354 single 8-channel mux and the MAX355 dual 4-channel mux protect analog signals while operating from a single 4.5V to 36V supply or ±4.5V to ±18V dual supplies. These muxes have 350Ω on-resistance and can be used for demultiplexing as well as multiplexing. Input leakage current is less than 0.5nA at +25°C and less than 5nA at +85°C.

All digital inputs have 0.8V and 2.4V logic thresholds, ensuring both TTL and CMOS logic compatibility without pull-up resistors. Break-before-make operation is guaranteed and power consumption is less than 1.5mW.

Applications

Data-Acquisition Systems

Industrial and Process Control

Avionics

ATE Equipment

Signal Routing

Redundant/Backup Systems

Features

- ♦ **350Ω Max On-Resistance**
- ♦ **Improved 2nd Source for MAX358/MAX359 and DG458/DG459**
- ♦ **Pin Compatible with ADG508F/ADG509F**
- ♦ **All Switches Off with Supplies Off**
- ♦ **On Switch Turns Off with Overvoltage**
- ♦ **Output Clamps at 1.5V Below Supply Rails**
- ♦ **0.5nA Max Input Leakage at +25°C (5nA at +85°C)**
- ♦ **No Power-Up Sequencing Required**
- ♦ **TTL and CMOS-Logic Compatibility**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX354CPE	0°C to +70°C	16 Plastic DIP
MAX354CWE	0°C to +70°C	16 Wide SO
MAX354C/D	0°C to +70°C	Dice*
MAX354EPE	-40°C to +85°C	16 Plastic DIP
MAX354EWE	-40°C to +85°C	16 Wide SO
MAX354MJE	-55°C to +125°C	16 CERDIP**
MAX355CPE	0°C to +70°C	16 Plastic DIP
MAX355CWE	0°C to +70°C	16 Wide SO
MAX355C/D	0°C to +70°C	Dice*
MAX355EPE	-40°C to +85°C	16 Plastic DIP
MAX355EWE	-40°C to +85°C	16 Wide SO
MAX355MJE	-55°C to +125°C	16 CERDIP**

** Dice are tested at T_A = +25°C only.*
*** Contact factory for availability.*

Pin Configurations

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND, unless otherwise noted.)

V+ .....-0.3V to +44V
V- .....+0.3V to -44V
V+ to V-.....-0.3V to +44V
Digital Inputs.....(V+ + 0.3V) to (V- - 0.3V)
Input Overvoltage with Mux Power On
  V+ = +15V ..... +25V
  V- = -15V.....-25V
Input Overvoltage with Mux Power Off
  V+ = 0V.....+40V
  V- = 0V .....-40V
Continuous Current into Any Terminal .....±30mA
Peak Current into Any Terminal.....±50mA
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
  Wide SO (derate 9.52mW/°C above +70°C)..... 762mW
  CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
  MAX35_C_ _ .....0°C to +70°C
  MAX35_E_ _.....-40°C to +85°C
  MAX35_M_ _.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
SWITCH									
Analog Signal Range	V_{COM}, V_{NO}	(Note 1)				(V+ - 40)		(V- + 40)	V
Fault-Free Analog Signal Range	V_{COM}, V_{NO}	V+ = +15V, V- = -15V (Note 1)				-12		12	V
On-Resistance (Note 2)	R_{ON}	I_{NO} = 1.0mA, V_{COM} = ±10V		T_A = +25°C			285	350	Ω
				T_A = T_{MIN} to T_{MAX}	C, E			450	
					M			500	
On-Resistance Matching Between Channels	ΔR_{ON}	I_{NO} = 1.0mA, V_{COM} = ±10V (Note 3)		T_A = +25°C			7	12	Ω
				T_A = T_{MIN} to T_{MAX}				15	
NO-Off Leakage Current (Note 4)	$I_{NO(OFF)}$	V_{COM} = ∓10V, V_{NO} = ±10V, V_{EN} = 0V		T_A = +25°C		-0.5	0.01	0.5	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-5.0		5.0	
					M	-50		50	
COM-Off Leakage Current (Note 4)	$I_{COM(OFF)}$	V_{COM} = ∓10V, V_{NO} = ±10V, V_{EN} = 0V	MAX354	T_A = +25°C		-0.5	0.02	0.5	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-25		25	
					M	-100		100	
		V_{COM} = ±10V, V_{NO} = ∓10V, V_{EN} = 0V	MAX355	T_A = +25°C		-0.5	0.02	0.5	
				T_A = T_{MIN} to T_{MAX}	C, E	-15		15	
					M	-50		50	
COM-On Leakage Current (Note 4)	$I_{COM(ON)}$	V_{COM} = ±10V, V_{NO} = ±10V, sequence each switch on	MAX354	T_A = +25°C		-0.5	0.02	0.5	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-30		30	
					M	-200		200	
			MAX355	T_A = +25°C		-0.5	0.02	0.5	
				T_A = T_{MIN} to T_{MAX}	C, E	-15		15	
					M	-100		100	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT							
Output Leakage Current (with Overvoltage)		V_D = 0V, analog overvoltage = ±33V	T_A = +25°C	-5	0.01	5	nA
			T_A = T_{MIN} to T_{MAX}	-2		2	µA
Input Leakage Current (with Overvoltage)		V_{IN} = ±25V, V_O = ±10V	T_A = +25°C	-0.1	0.001	0.1	µA
			T_A = T_{MIN} to T_{MAX}	-2		2	
Input Leakage Current (with Power Supplies Off)		V_{IN} = ±25V, V_{EN} = V_O = 0V, V_{A0} = V_{A1} = V_{A2} = 0V or 5V	T_A = +25°C	-0.1	0.001	0.1	µA
			T_A = T_{MIN} to T_{MAX}	-2		2	
DIGITAL LOGIC INPUT							
Logic High Input Voltage	V_{A_H}, V_{ENH}		T_A = T_{MIN} to T_{MAX}	2.4			V
Logic Low Input Voltage	V_{A_L}, V_{ENL}		T_A = T_{MIN} to T_{MAX}			0.8	V
Input Current with Input Voltage High	I_{A_H}, I_{ENH}	V_A = V_{EN} = 2.4V	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Input Current with Input Voltage Low	I_{A_L}, I_{ENL}	V_A = V_{EN} = 0.8V	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
SUPPLY							
Power-Supply Range				±4.5		±18	V
Positive Supply Current	I+	V_{EN} = V_A = 5V	T_A = +25°C	-300		300	µA
			T_A = T_{MIN} to T_{MAX}	-500		500	
Negative Supply Current	I-	V_{EN} = V_A = 0V	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-100		100	
DYNAMIC							
Transition Time	t_{TRANS}	Figure1	T_A = +25°C		180	250	ns
			T_A = T_{MIN} to T_{MAX}			400	
Enable Turn-On Time	$t_{ON(EN)}$	Figure 2	T_A = +25°C		160	250	ns
			T_A = T_{MIN} to T_{MAX}			400	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 2	T_A = +25°C		80	200	ns
			T_A = T_{MIN} to T_{MAX}			300	
Break-Before-Make Interval	t_{OPEN}	Figure 3	T_A = +25°C	50	100		ns
Charge Injection	V_{CTE}	C_L = 10nF, V_S = 0V, R_S = 0Ω, Figure 4	T_A = +25°C		80		pC
Off Isolation	V_{ISO}	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz, Figure 5	T_A = +25°C		100		dB
Crosstalk Between Channels	V_{CT}	V_{EN} = 2.4V, f = 100kHz, V_{GEN} = $1V_{p-p}$, R_L = 1kΩ, Figure 6	T_A = +25°C		92		dB
Logic Input Capacitance	C_{IN}	f = 1MHz, Figure 7	T_A = +25°C		2.5		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, V_{EN} = V_D = 0V	T_A = +25°C		1.6		pF

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = V_{ENH} = 2.4V, V_{AL} = V_{ENL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DYNAMIC (cont'd)								
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 7, V_{EN} = V_D = 0V	MAX354	T_A = +25°C		11		pF
			MAX355			5		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 7, V_{EN} = V_D = 0V	MAX354	T_A = +25°C		28		pF
			MAX355			14		
Setting Time (Note 5)	t_{SETT}	0.1%		T_A = +25°C		1		µs
		0.01%				2.5		

Note 1: When the analog signal exceeds +13.5V or -13.5V, the blocking action of Maxim's gate structure goes into operation. Only leakage currents flow, and the channel on-resistance rises to infinity (see *Typical Operating Characteristics*).

Note 2: Electrical characteristics such as on-resistance will change when power supplies other than ±15V are used.

Note 3: ΔR_{ON} = $R_{ON(MAX)}$ - $R_{ON(MIN)}$

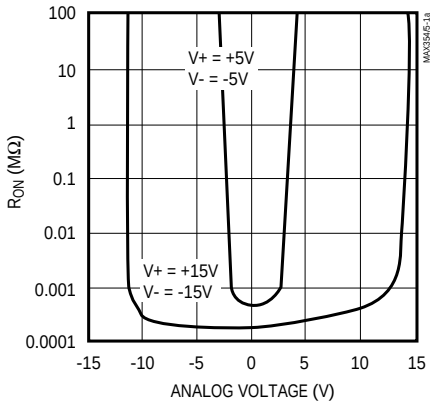
Note 4: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at +25°C.

Note 5: Guaranteed by design.

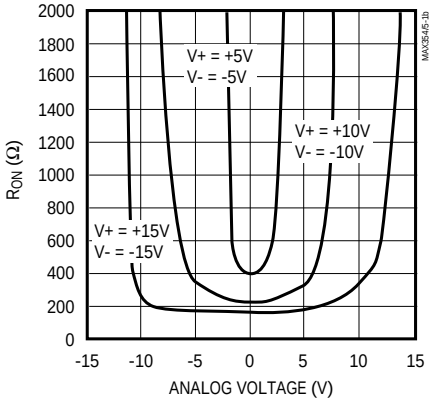
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

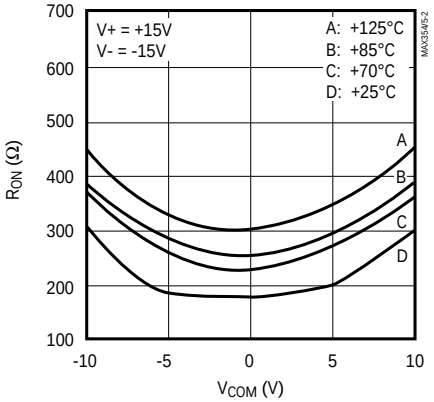
ON-RESISTANCE vs. ANALOG VOLTAGE



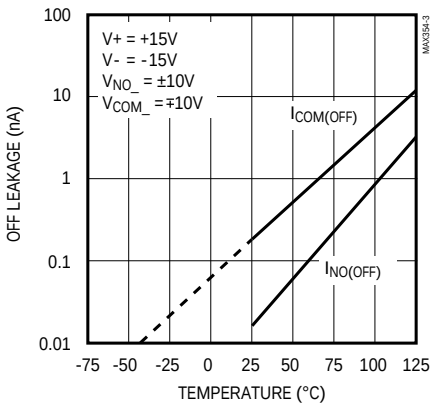
ON-RESISTANCE vs. ANALOG VOLTAGE



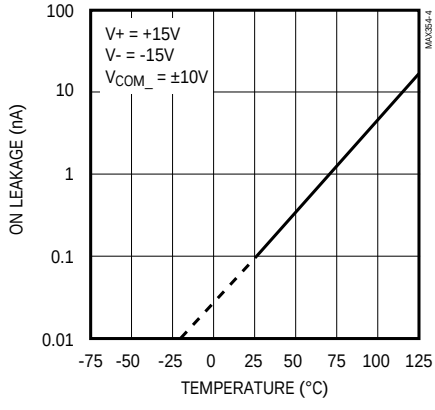
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



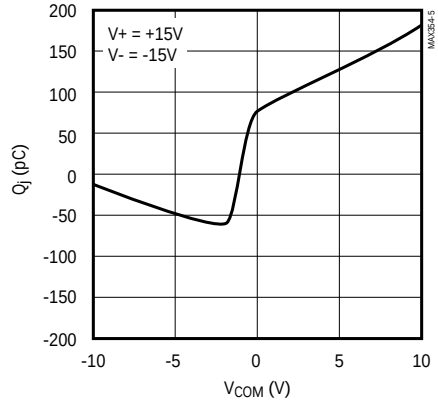
OFF LEAKAGE vs. TEMPERATURE



ON LEAKAGE vs. TEMPERATURE

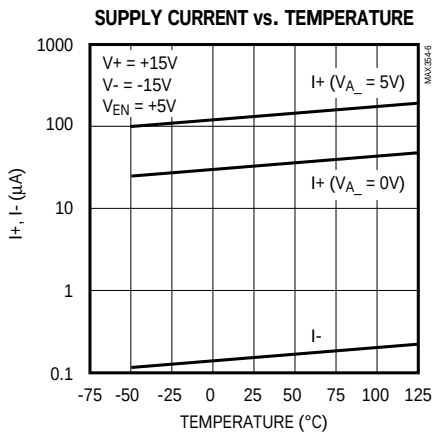


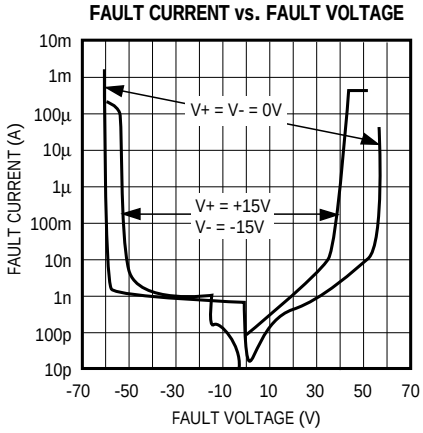
CHARGE INJECTION vs. V_{COM}



Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)





Pin Description

PIN		NAME	FUNCTION
MAX354	MAX355		
1, 15, 16	—	A0, A2, A1	Address Logic Inputs
—	1, 16	A0, A1	Address Logic Inputs
2	2	EN	Enable Logic Input. See truth tables.
3	3	V-	Negative Supply Voltage Input. Connect to GND for single-supply operation.
4–7	—	NO1–NO4	Analog Inputs—bidirectional
—	4–7	NO1A–NO4A	Analog Inputs—bidirectional “A” switch
8	—	COM	Analog Output—bidirectional
—	8, 9	COMA, COMB	Analog Outputs—bidirectional
9–12	—	NO8–NO5	Analog Inputs—bidirectional
—	10–13	NO4B–NO1B	Analog Inputs—bidirectional “B” switch
13	14	V+	Positive Supply Voltage Input
14	15	GND	Ground

Note: Analog inputs and outputs are electrically identical and completely interchangeable.

Test Circuits/Timing Diagrams

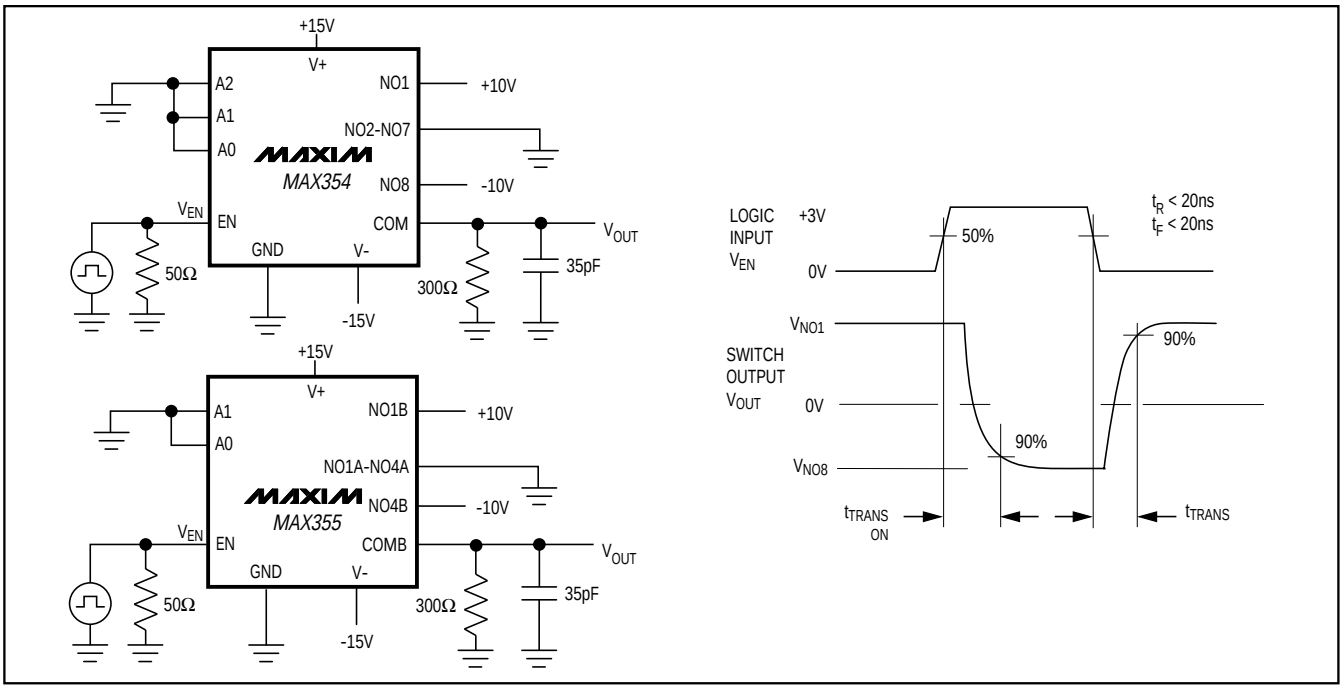


Figure 1. Transition Time

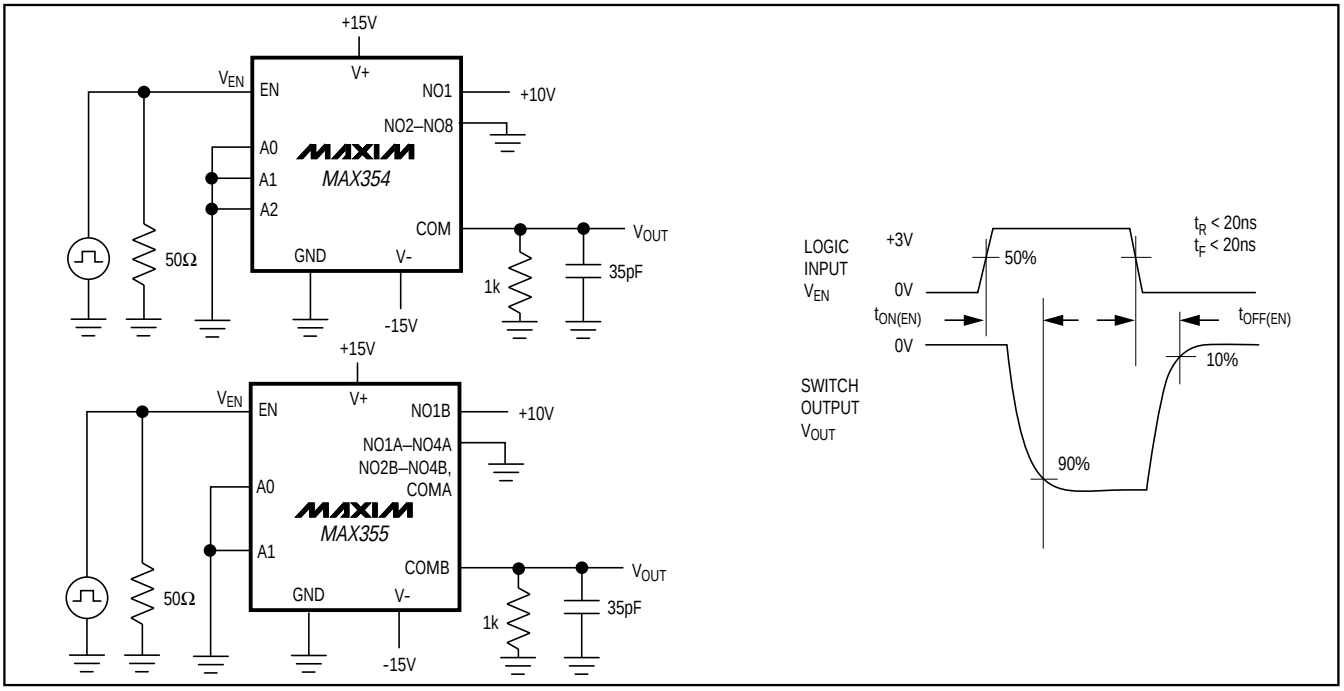


Figure 2. Enable Switching Time

Test Circuits/Timing Diagrams (continued)

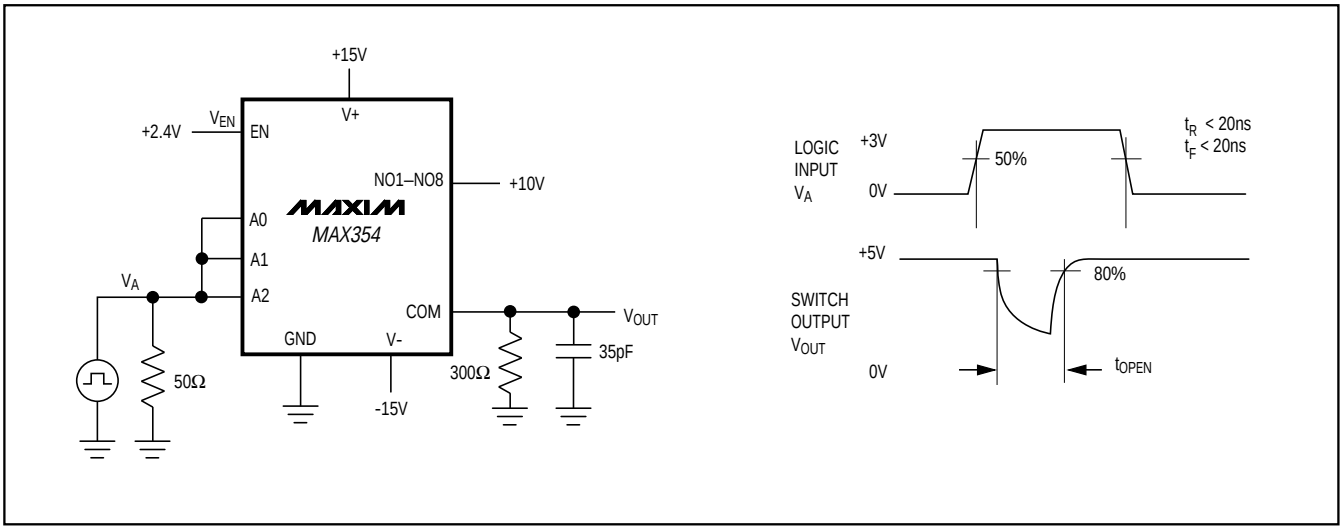


Figure 3. Break-Before-Make Interval

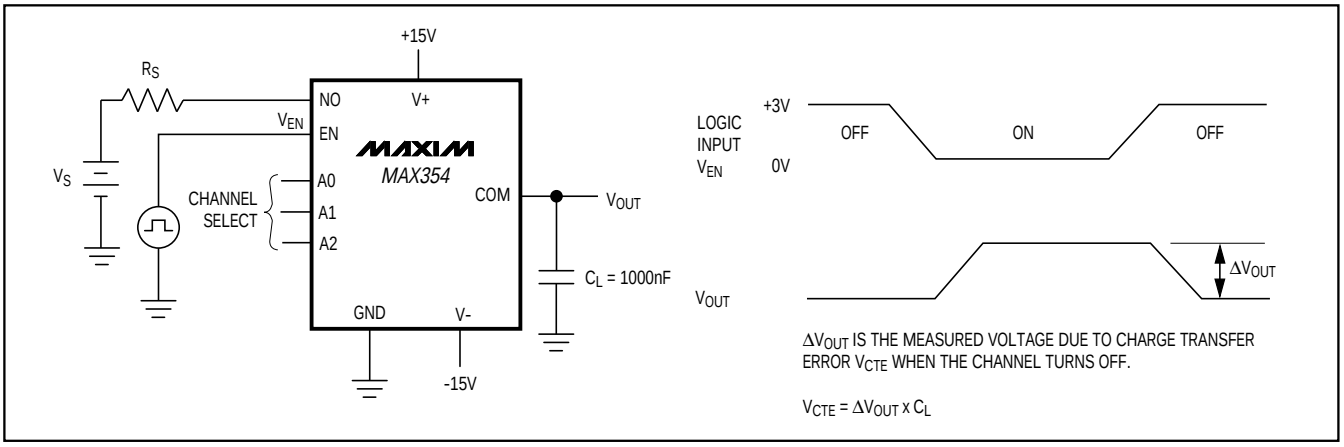


Figure 4. Charge Injection

Fault-Protected Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

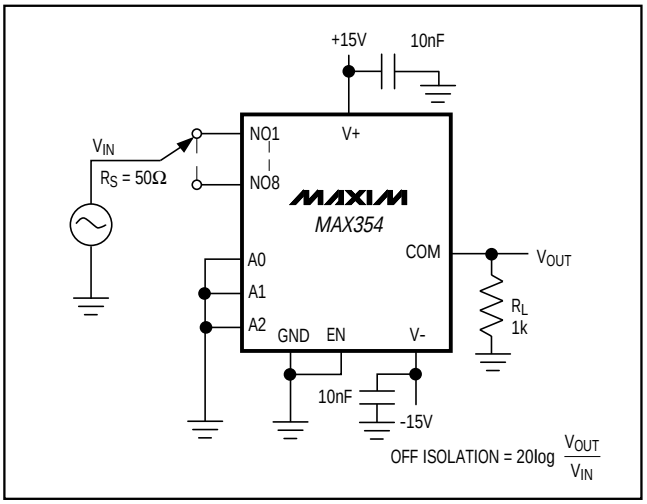


Figure 5. Off Isolation

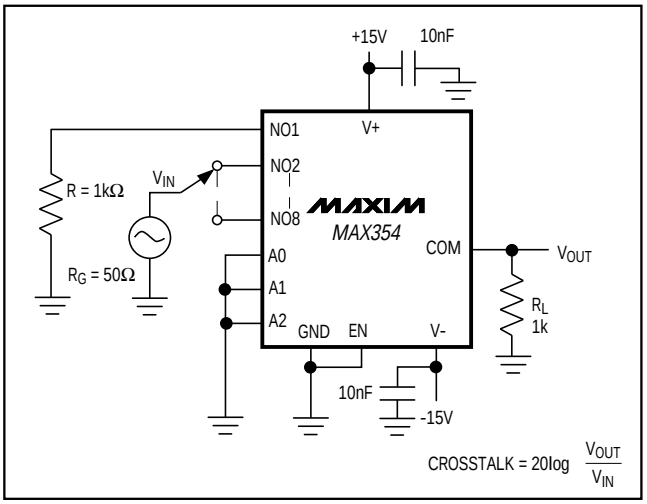


Figure 6. Crosstalk

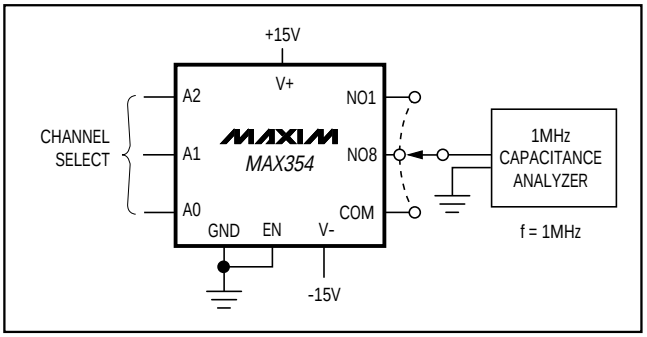


Figure 7. NO/COM Capacitance

Detailed Description

Fault-Protection Circuitry

Maxim's MAX354/MAX355 are fully fault protected for continuous input voltages up to ±40V, whether or not the V+ and V- power supplies are present. These devices use a "series FET" protection scheme that not only protects the multiplexer output from overvoltage, but also limits the input current to sub-microamp levels. When signal voltages exceed or are within approximately 1.5V of the supply rails, on-resistance increases. This greater on-resistance limits fault currents and output voltage, protecting sensitive circuits and components. The protected output clamps at approximately 1.5V below the supply rails and maintains the correct polarity. There are no glitches or polarity reversals going into or coming out of a fault condition.

Figures 8 and 9 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -25V input, N-channel FET Q1 is turned on by the +25V gate-to-source voltage. The P-channel device (Q2), however, has +25V V_{GS} and is turned off, thereby preventing the input signal from reaching the output. If the input voltage is +25V, Q1 has a negative V_{GS}, which turns it off. Similarly, only sub-microamp leakage currents can flow from the output back to the input, since any voltage will turn off either Q1 or Q2.

Figure 10 shows the condition of an off channel with V+ and V- present. As with Figures 8 and 9, either an N-channel or a P-channel device will be off for any input voltage from -40V to +40V. The leakage current with negative overvoltages will immediately drop to a few nanoamps at +25°C. For positive overvoltages, that fault current will initially be 10µA or 20µA, decaying over a few seconds to the nanoamp level. The time constant of this decay is caused by the discharge of stored charge from internal nodes and does not compromise the fault-protection scheme.

Figure 11 shows the condition of the on channel with V+ and V- present. With input voltages less than ±10V, all three FETs are on and the input signal appears at the output. If the input voltage exceeds V+ minus the N-channel threshold voltage (V_{TN}), the N-channel FET will turn off. For voltages more negative than V- minus the P-channel threshold (V_{TP}), the P-channel device will turn off. Since V_{TN} is typically 1.5V and V_{TP} is typically 3V, the multiplexer's output swing is limited to about -12V to +13.5V with ±15V supplies.

Switching Characteristics and Charge Injection

Table 1 shows typical charge injection levels versus power-supply voltages and analog input voltage. The charge injection that occurs during switching creates a voltage transient whose magnitude is inversely proportional to the capacitance on the multiplexer output.

Table 1. MAX354 Charge Injection

Supply Voltage	Analog Input Level	Injected Charge
±5V	+2V 0V -2V	52pC 35pC 16pC
±10V	+5V 0V -5V	105pC 65pC 25pC
±15V	+10V 0V -10V	180pC 80pC 15pC

Test Conditions: C_L, = 1000pF on mux output; the tabulated analog input level is applied to channel 1; channels 2–8 inputs are open circuited. EN = +5V, $V_{A1} = V_{A2} = 0V$, V_O is toggled at a 2kHz rate between 0V and 3V. +100pC of charge creates a +100mV step when injected into a 1000pF load capacitance.

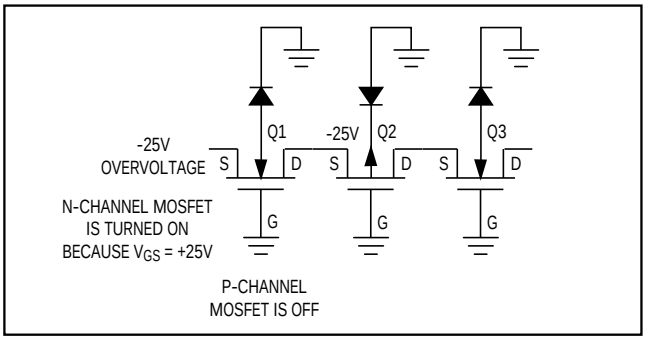


Figure 8. -25V Overvoltage with Multiplexer Power Off

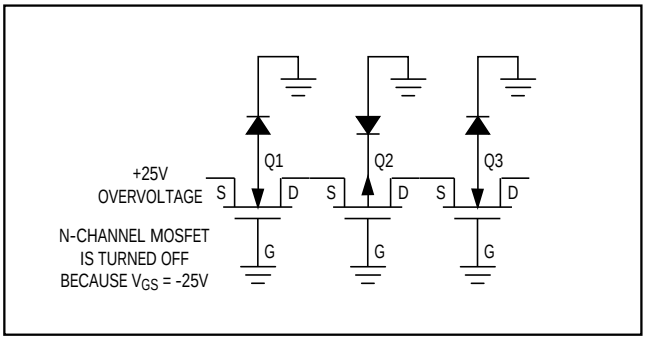


Figure 9. +25V Overvoltage with Multiplexer Power Off

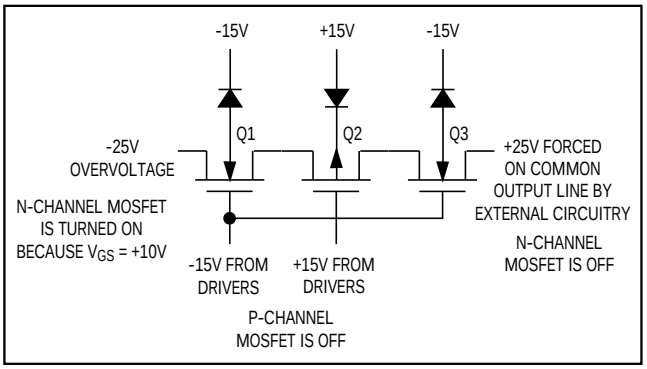


Figure 10. -25V Overvoltage on an Off Channel with Multiplexer Power Supply On

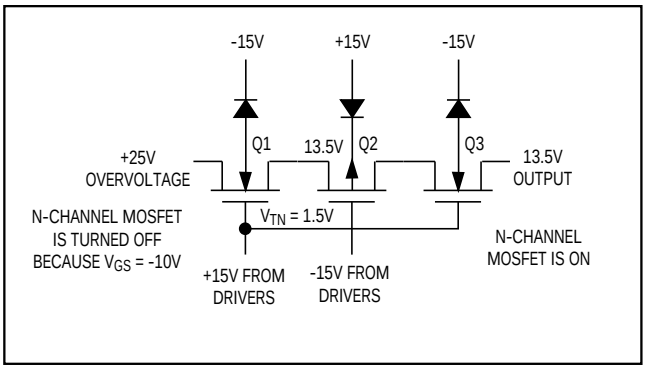


Figure 11. +25V Overvoltage Input to the On Channel

The channel-to-channel switching time is typically 180ns, with about 100ns of break-before-make delay. This 100ns break-before-make delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data acquisition system, the dominant delay is not the switching time of the multiplexer, but is the settling time of the amplifiers and S/H. Another limiting factor is the RC time constant of the multiplexer R_{ON} plus the signal source impedance multiplied by the load capacitance on the output of the multiplexer. Even with low signal source impedances, 100pF of capacitance on the multiplexer output will approximately double the settling time to 0.01% accuracy.

Operation with Supply Voltages Other than ±15V

The main effect of supply voltages other than ±15V is the reduction in output signal range. The MAX354 limits the output voltage to about 1.5V below V+ and about 3V above V-. In other words, the output swing is limited to +3.5V to -2V when operating from ±5V. The *Typical Operating Characteristics* show R_{ON} for +15V and ±5V power supplies. Maxim tests and guarantees the MAX354/MAX355 for operation from ±4.5V to ±18V supplies. The switching delays are increased by about a factor of 2 at ±5V, but break-before-make action is preserved.

The MAX354/MAX355 can operate with a single +4.5V to +30V supply, as well as asymmetrical power supplies such as +15V and -5V. The digital threshold remains approximately 1.6V above the GND pin, and the analog characteristics, such as R_{ON}, are determined by the total voltage difference between V+ and V-. Connect V- to 0V when operating with a +4.5V to +30V single supply.

The MAX354 digital threshold is relatively independent of the power-supply voltages, going from 1.6V typical when V+ is 15V to 1.5V typical when V+ is 5V. This means that the MAX354/MAX355 operate with standard TTL-logic levels, even with ±5V power supplies. In all cases, the threshold of the enable (EN) pin is the same as the other logic inputs.

Digital Interface Levels

The typical digital threshold of both the address lines and the enable pin is 1.6V, with a temperature coefficient of about -3mV/°C. This ensures compatibility with 0.8V to 2.4V TTL-logic swings over the entire temperature range. The digital threshold is relatively independent of the supply voltages, moving from 1.6V typical to 1.5V typical as the power supplies are reduced from ±15V to ±5V. In all cases, the digital threshold is referenced to the GND pin.

The digital inputs can also be driven with CMOS-logic levels swinging from either V+ to V- or from V+ to ground. The digital input current is just a few nanoamps of leakage at all input voltage levels, with a guaranteed maximum of 1µA.

Operation as a Demultiplexer

The MAX354/MAX355 function as demultiplexers where the input is applied to the output pin, and the input pins are used as outputs. The MAX354/MAX355 provide both break-before-make action and full fault protection when operated as demultiplexers, unlike earlier generations of fault-protected muxes.

Channel-to-Channel Crosstalk, Off-Isolation, and Digital Feedthrough

At DC and low frequencies the channel-to-channel crosstalk is caused by variations in output leakage currents as the off-channel input voltages are varied. The MAX354 output leakage varies only a few picoamps as all seven off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX354 output, which is R_{ON} plus the input signal source resistance in most cases, since the load driven by the MAX354 is usually high impedance. For a signal source impedance of 10kΩ or lower, the DC crosstalk exceeds 120dB.

Tables 2a and 2b show typical AC crosstalk and off-isolation performance. Digital feedthrough is masked by the analog charge injection when the output is enabled. When the output is disabled, the digital feedthrough is virtually unmeasureable, since the digital pins are physically isolated from the analog section by the GND and V- pins. The ground plane formed by these lines is continued onto the MAX354/MAX355 die to provide over 100dB isolation between the digital and analog sections.

Table 2a. Typical Off-Isolation Rejection Ratio

Frequency	100kHz	1MHz
One Channel Driven	100dB	80dB

Test Conditions: V_{IN} = 20Vp-p at the tabulated frequency, R_L = 1.5kΩ between OUT and ground, EN = 0V.

$$V_{ISO} = 20\log \frac{20Vp\text{-}p}{VOUT\ (p\text{-}p)}$$

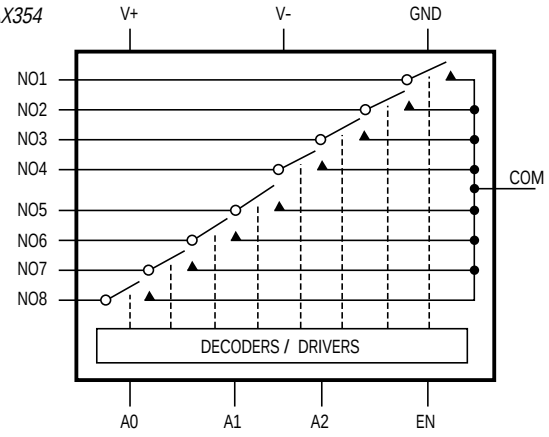
Table 2b. Typical Crosstalk Rejection Ratio

Frequency	100kHz	1MHz
R_L = 1.5kΩ	92dB	72dB
R_L = 10kΩ	76dB	56dB

Test Conditions: Specified R_L connected from OUT to ground, EN = +5V, A_0 = A_1 = A_2 = +5V (Channel 1 selected). 20Vp-p at the tabulated frequency is applied to Channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

Functional Diagrams/Truth Tables

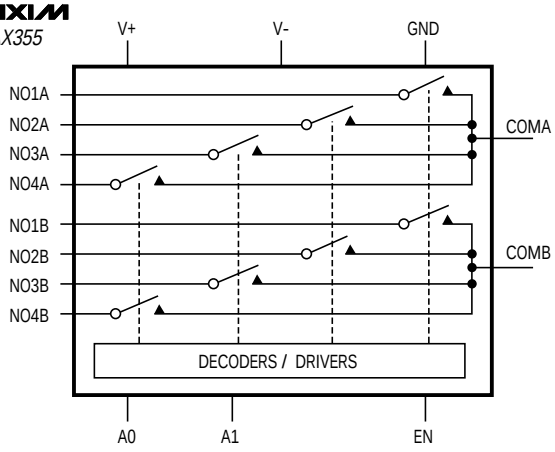
MAXIM
MAX354



MAX354				
A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "0" $V_{AL} \leq +0.8V$, LOGIC "1" $V_{AH} \geq +2.4V$

MAXIM
MAX355



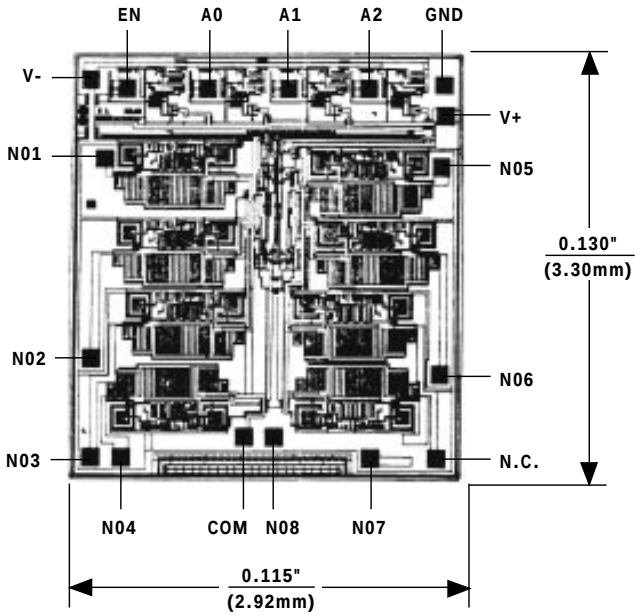
MAX355			
A1	A0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

LOGIC "0" $V_{AL} \leq +0.8V$, LOGIC "1" $V_{AH} \geq +2.4V$

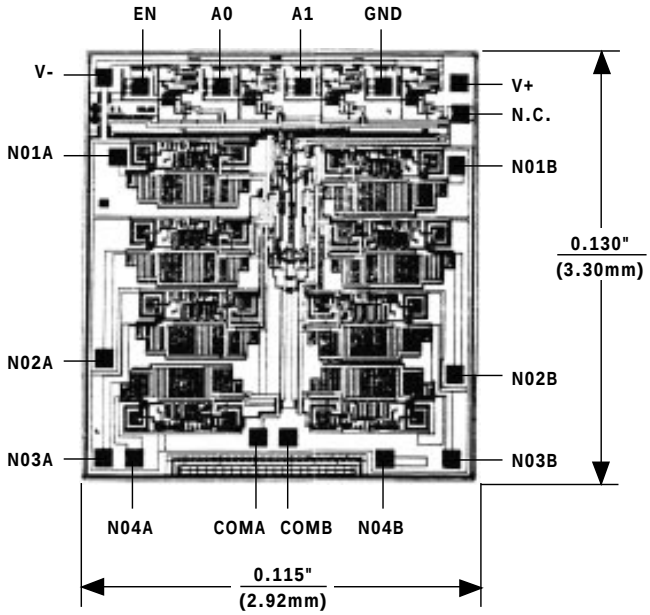
Fault-Protected Analog Multiplexers

Chip Topographies

MAX354



MAX355



TRANSISTOR COUNT: 256
SUBSTRATE CONNECTED TO V+