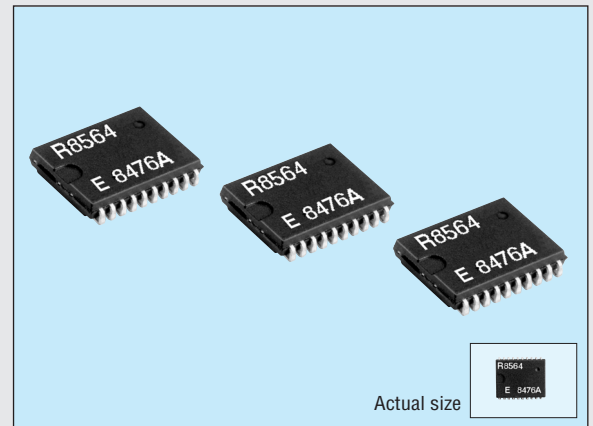


I²C-BUS INTERFACE REAL TIME CLOCK MODULE

RTC-8564JE

- Built-in crystal unit allows adjustment-free efficient operation.
- Compliant with I²C high-speed bus specifications. (400 kHz)
- Equipped with alarm, timer, and frequency output (32.768 kHz, 1024 Hz, 32 Hz, 1 Hz) features.
- Inclusion of century bit to enable correct date even after year 2000
- Operating in wide voltage range from 1.8 to 5.5 V, and in wide range of clock voltage from 1.2 to 5.5 V.
- Low power consumption at 275 nA/3.0 V. (Typ.)



■ Specifications (characteristics)

■ Absolute Max. rating

Item	Symbol	Condition	Min.	Max.	Unit
Supply voltage	V _{DD}	Between V _{DD} and GND	-0.5	+6.5	V
	I _{DD}	V _{DD} pin	-50	50	mA
Input voltage	V _i	Input pin	GND-0.5	V _{DD} +0.5	V
Output voltage	V _o	INT pins			
DC Input current	I _i	—	-10	10	mA
DC Output current	I _o	—	-10	10	mA
Storage temperature Range	T _{STG}	As single part	-55	+125	°C

■ Operating range

Item	Symbol	Condition	Min.	Max.	Unit
Supply voltage range	V _{DD}	I ² C-BUS access at 400 kHz	1.8	5.5	V
Clock voltage range		—	V _{LOW}		
Operating temperature range	T _{OPR}	—	-40	+85	°C

■ Frequency characteristics

Item	Symbol	Condition	Max.	Unit
Frequency precision	Δf/f ₀	T _a =+25 °C, V _{DD} =3.0 V	5±23	× 10 ⁻⁶
Frequency temperature characteristics	T _{OP}	T _a =+25 °C, -10 to +70 °C, V _{DD} =3.0 V	+10 -120	
Frequency voltage characteristics	f _v	T _a =+25 °C, V _{DD} =1.2 V to 5.5 V	±2	× 10 ⁻⁶ /V
Oscillation start-up time	t _{STA}	T _a =+25 °C, V _{DD} =1.8 V	3	s
Aging	f _a	T _a =+25 °C, V _{DD} =3.0 V	±5	× 10 ⁻⁶ /year

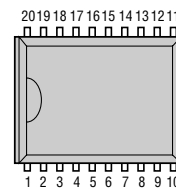
■ DC characteristics

(V_{DD}=1.8 to 5.5 V, T_a=-40 to +85 °C)

Item	Pin	Symbol	Condition	Min.	Typ.	Max.	Unit	
Power current (during access)	—	I _{DDO}	f _{SCL} =400 kHz f _{SCL} =100 kHz	—	—	800 200	μA	
Power current (not during access)		I _{DD}	f _{SCL} =0 Hz, V _{DD} =5.0 V f _{SCL} =0 Hz, V _{DD} =3.0 V f _{SCL} =0 Hz, V _{DD} =2.0 V		0.33 0.275 0.25	0.80 0.70 0.65		
			I _{DD32k}		f _{SCL} =0 Hz, V _{DD} =5.0 V f _{SCL} =0 Hz, V _{DD} =3.0 V f _{SCL} =0 Hz, V _{DD} =2.0 V	2.5 1.5 1.1		3.4 2.2 1.6
		V _{IL}			—	GND-0.5 0.7×V _{DD}		0.3×V _{DD} V _{DD} +0.5
		V _{IH}						
“L” input voltage		SDA	I _{OL} (SDA)		V _{OL} =0.4 V, V _{DD} =5 V	-3		—
“H” input voltage	INT	I _{OL} (INT)	-1					
“L” output voltage	CLKOUT	I _{OL} (CLKOUT)	—	1				
“H” output voltage		I _{OH} (CLKOUT)	—	1				
Leakage current	—	I _{LO}	V _O =V _{DD} or GND	-1	—	1	μA	
Low voltage detection		V _{LOW}	T _a =-40 °C to +85 °C T _a =20 °C to +70 °C	—	0.9 0.9	1.1 1.0	V	

The I²C-Bus is a trademark of Philips Electronics N.V.

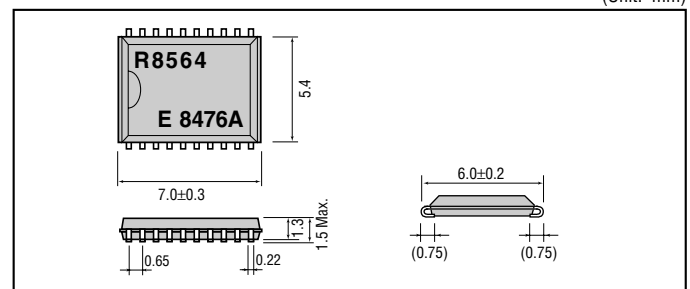
■ Terminal connection



No.	Pin terminal
1	N.C
2	N.C
3	CLKOE
4	V _{DD}
5	CLKOUT
6	SCL
7	SDA
8	(GND)
9	GND
10	INT
11	N.C
12	N.C
13	N.C
14	N.C
15	N.C
16	N.C
17	N.C
18	N.C
19	N.C
20	N.C

■ External dimensions

(Unit: mm)



Register table

Address	Register symbol	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Control 1	TEST	0	STOP	0	TEST	0	0	0
1	Control 2	0	0	0	TI/TP	AF	TF	AIE	TIE
2	Sec	VL	S 40	S 20	S 10	S 8	S 4	S 2	S 1
3	Min	*	Min 40	Min 20	Min 10	Min 8	Min 4	Min 2	Min 1
4	Hour	*	*	Hour 20	Hour 10	Hour 8	Hour 4	Hour 2	Hour 1
5	Day	*	*	Day 20	Day 10	Day 8	Day 4	Day 2	Day 1
6	Week	*	*	*	*	*	W 4	W 2	W 1
7	Month/Century	C	*	*	Month 10	Month 8	Month 4	Month 2	Month 1
8	Year	Year 80	Year 40	Year 20	Year 10	Year 8	Year 4	Year 2	Year 1
9	Minutes Alarm	AE	A-Min 40	A-Min 20	A-Min 10	A-Min 8	A-Min 4	A-Min 2	A-Min 1
A	Hours Alarm	AE	A-Hr 40	A-Hr 20	A-Hr 10	A-Hr 8	A-Hr 4	A-Hr 2	A-Hr 1
B	Day Alarm	AE	*	A-Day 20	A-Day 10	A-Day 8	A-Day 4	A-Day 2	A-Day 1
C	Week Alarm	AE	*	*	*	*	A-W 4	A-W 2	A-W 1
D	CLKOUT frequency	FE	*	*	*	*	*	FD1	FD0
E	Timer control	TE	*	*	*	*	*	TD1	TD0
F	Timer	128	64	32	16	8	4	2	1

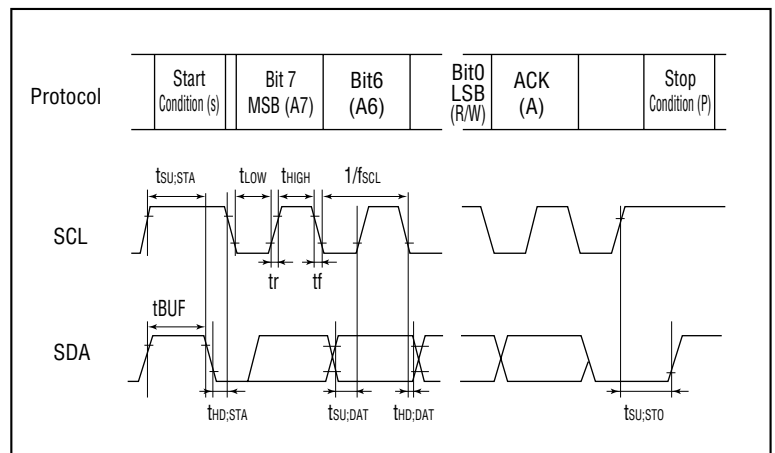
0 : Always set this bit to "0".

Switching characteristics

(V_{DD}=1.8 to 5.5 V, T_a=-40 °C to +85 °C)

Item	Symbol	Min.	Max.	Unit
SCL clock frequency	f _{SCL}	—	400	kHz
Tolerance spike time on bus	t _{SW}	—	50	ns
Start condition set-up time	t _{SU;STA}	0.6	—	μs
Start condition Hold time	t _{HD;STA}	—	—	—
SCL "L" time	t _{LOW}	1.3	—	μs
SCL "H" time	t _{HIGH}	0.6	—	μs
SCL and SDA rise time	t _r	—	0.3	μs
SCL and SDA fall time	t _f	—	—	—
Date set-up time	t _{SU;DAT}	100	—	ns
Date hold time	t _{HD;DAT}	0	—	ns
Stop condition set-up time	t _{SU;STO}	4.0	—	μs

Timing chart



Block diagram

