

JOHNSON DECADE COUNTER WITH 10 DECODED OUTPUTS

FEATURES

- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4017 are high-speed Si-gate CMOS devices and are pin compatible with the "4017" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4017 are 5-stage Johnson decade counters with 10 decoded active HIGH outputs (Q_0 to Q_9), an active LOW output from the most significant flip-flop ($\bar{Q}_{5-9}$), active HIGH and active LOW clock inputs (CP_0 and $\bar{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while $\bar{CP}_1$ is LOW or a HIGH-to-LOW transition at $\bar{CP}_1$ while CP_0 is HIGH (see also function table).

When cascading counters, the $\bar{Q}_{5-9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($Q_0 = \bar{Q}_{5-9} = \text{HIGH}$; Q_1 to $Q_9 = \text{LOW}$) independent of the clock inputs (CP_0 and $\bar{CP}_1$).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_0 , $\bar{CP}_1$ to Q_n	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	20	21	ns
f_{max}	maximum clock frequency		77	67	MHz
C_I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	35	36	pF

$GND = 0 \text{ V}$; $T_{amb} = 25^\circ \text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

C_L = output load capacitance in pF

f_o = output frequency in MHz

V_{CC} = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_I = GND$ to V_{CC}

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

16-lead DIL; plastic (SOT382).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 4, 7, 10, 1, 5, 6, 9, 11	Q_0 to Q_9	decoded outputs
8	GND	ground (0 V)
12	$\bar{Q}_{5-9}$	carry output (active LOW)
13	$\bar{CP}_1$	clock input (HIGH-to-LOW, edge-triggered)
14	CP_0	clock input (LOW-to-HIGH, edge-triggered)
15	MR	master reset input (active HIGH)
16	V_{CC}	positive supply voltage

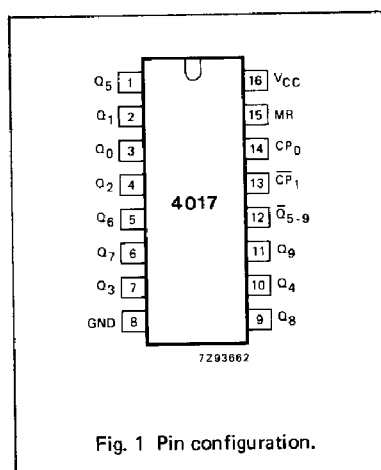


Fig. 1 Pin configuration.

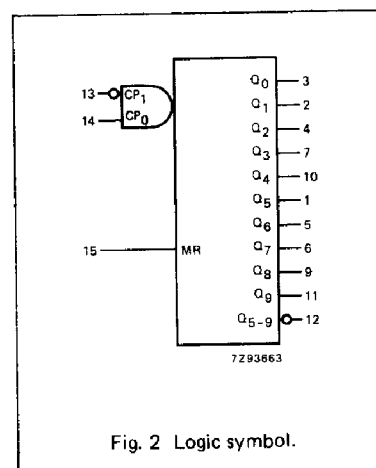


Fig. 2 Logic symbol.

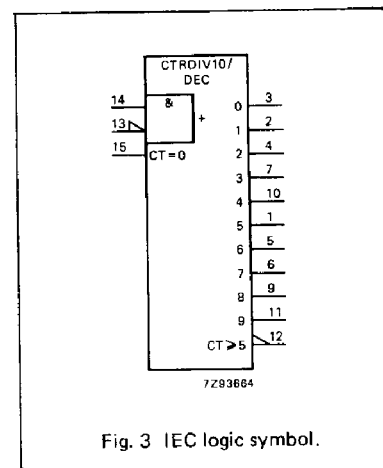


Fig. 3 IEC logic symbol.

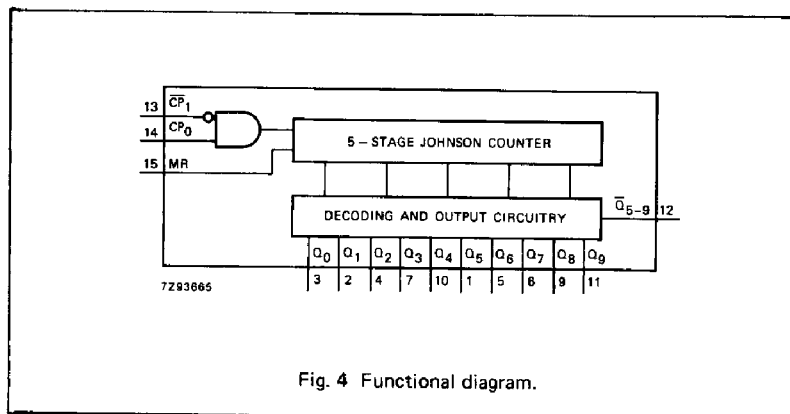


Fig. 4 Functional diagram.

FUNCTION TABLE

MR	CP ₀	$\overline{CP}_1$	OPERATION
H	X	X	$Q_0 = Q_{5-9} = H$; Q_1 to $Q_9 = L$
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition
↓ = HIGH-to-LOW clock transition

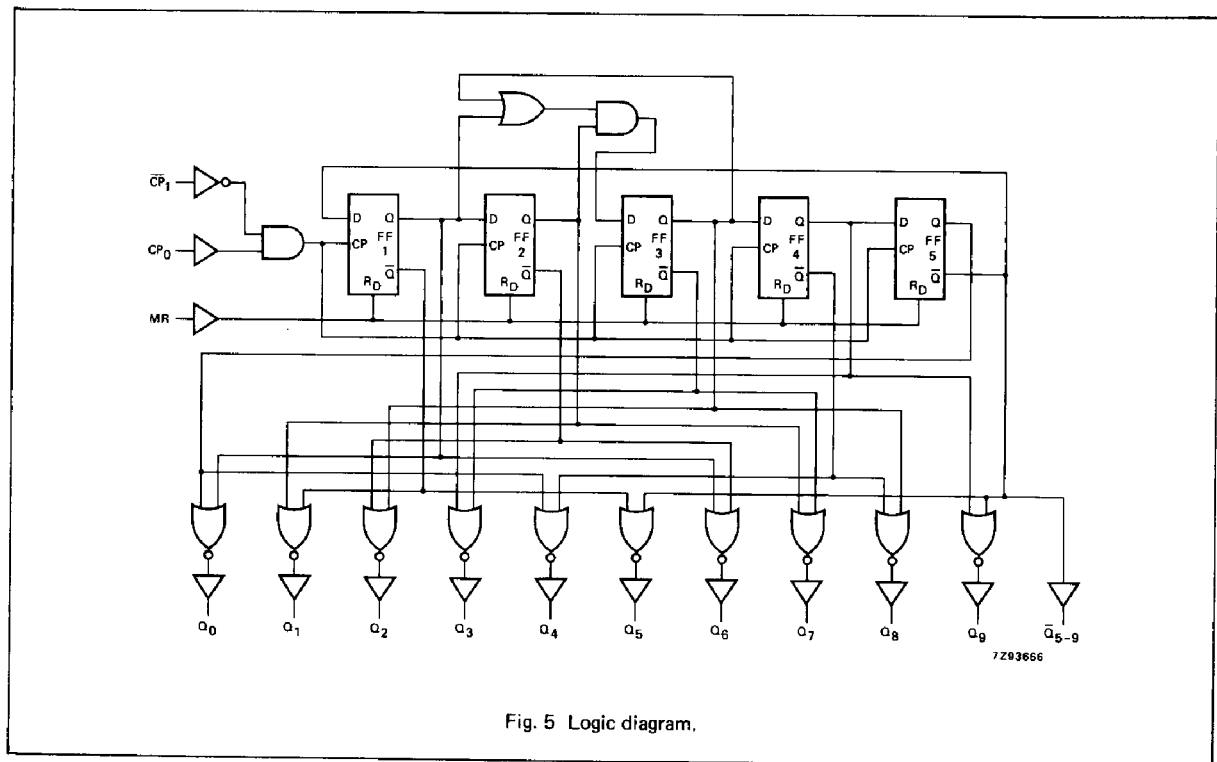


Fig. 5 Logic diagram.

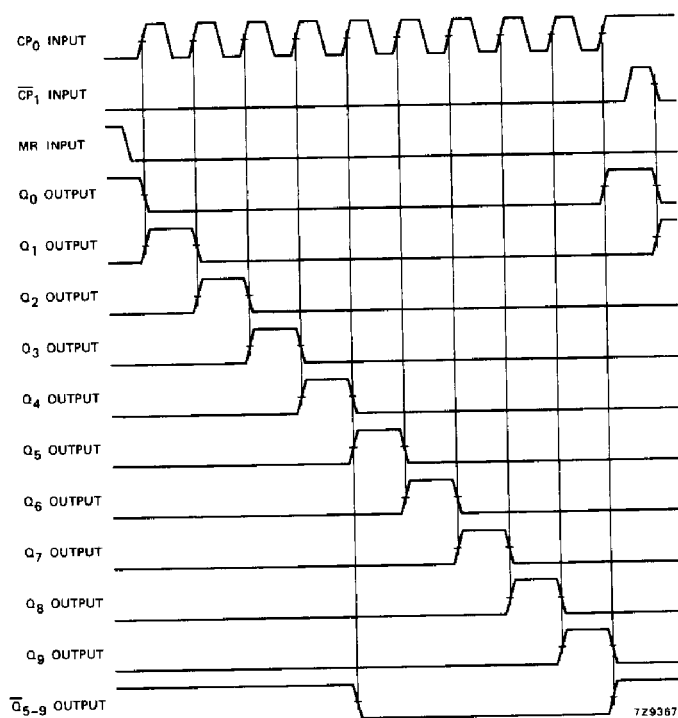


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q _n		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9	
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q ₅₋₉		63 23 18	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 9	
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q _n		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9	
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q ₅₋₉		61 22 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig. 9	
t _{PHL}	propagation delay MR to Q ₁₋₉		52 19 15	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8	
t _{PLH}	propagation delay MR to Q ₅₋₉ , Q ₀		55 20 16	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig. 8	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 9	
t _W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t _W	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t _{rem}	removal time MR to CP ₀ , CP ₁	5 5 5	-17 -6 -5		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 8	
t _{su}	set-up time CP ₁ to CP ₀ ; CP ₀ to CP ₁	50 10 9	-8 -3 -2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7	
t _h	hold time CP ₀ to CP ₁ ; CP ₁ to CP ₀	50 10 9	17 6 5		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 7	
f _{max}	maximum clock pulse frequency	6.0 30 25	23 70 83		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 8	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{CP}_1$	0.40
CP_0	0.25
MR	0.50

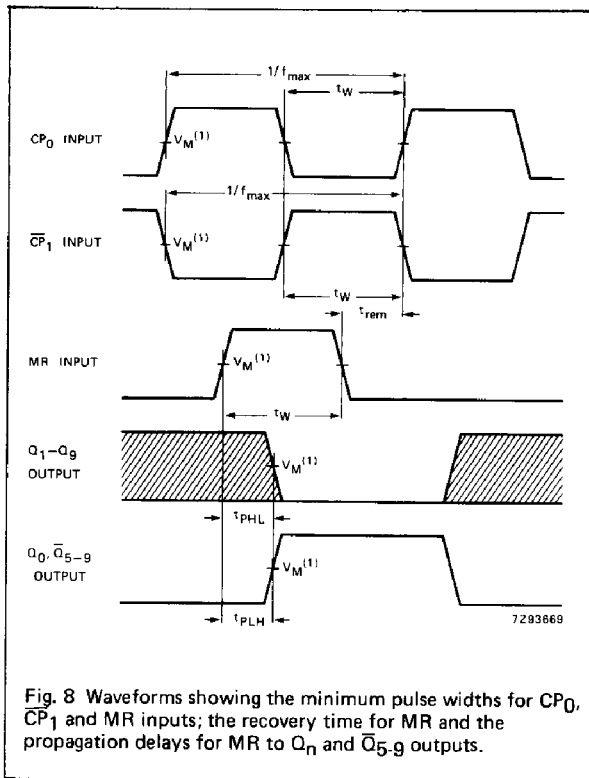
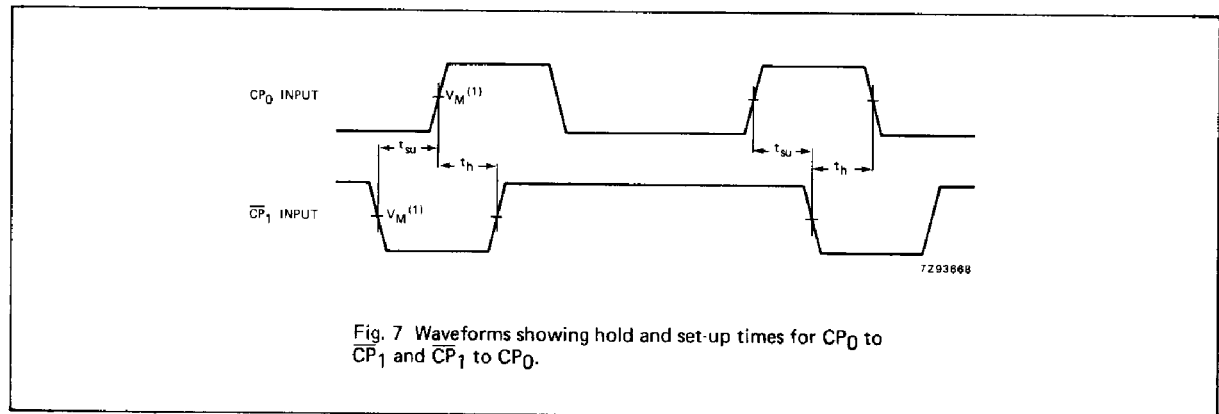
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

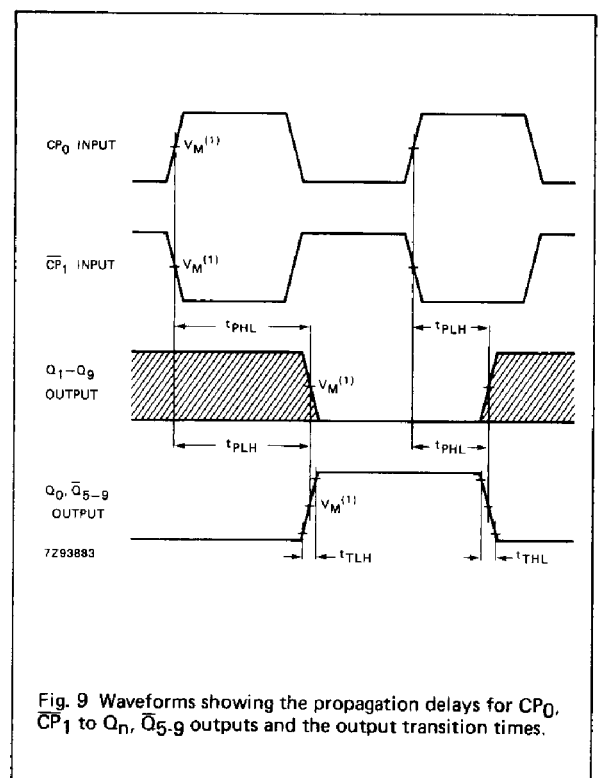
SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} V	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q _n		25	46		58		69	ns	4.5	Fig. 9
t _{PHL} / t _{PLH}	propagation delay CP ₀ to Q _{5,9}		25	46		58		69	ns	4.5	Fig. 9
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q _n		25	50		63		75	ns	4.5	Fig. 9
t _{PHL} / t _{PLH}	propagation delay CP ₁ to Q _{5,9}		25	50		63		75	ns	4.5	Fig. 9
t _{PHL}	propagation delay MR to Q ₁₋₉		22	46		58		69	ns	4.5	Fig. 8
t _{PLH}	propagation delay MR to Q _{5,9} , Q ₀		20	46		58		69	ns	4.5	Fig. 8
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 9
t _W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig. 8
t _W	master reset pulse width; HIGH	16	4		20		24		ns	4.5	Fig. 8
t _{rem}	removal time MR to CP ₀ , CP ₁	5	-5		5		5		ns	4.5	Fig. 8
t _{su}	set-up time CP ₁ to CP ₀ ; CP ₀ to CP ₁	10	-3		13		15		ns	4.5	Fig. 7
t _h	hold time CP ₀ to CP ₁ ; CP ₁ to CP ₀	10	6		13		15		ns	4.5	Fig. 7
f _{max}	maximum clock pulse frequency	30	61		24		20		MHz	4.5	Fig. 8

AC WAVEFORMS



Note to Figs 8 and 9

Conditions:
 CP_1 = LOW while CP_0 is triggered on a LOW-to-HIGH transition and CP_0 = HIGH, while CP_1 is triggered on a HIGH-to-LOW transition.



Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

Some applications for the "4017" are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 10 shows a technique for extending the number of decoded output states for the "4017". Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



It is essential not to enable the counter on $\overline{CP}_1$ when CP_0 is HIGH, or on CP_0 when $\overline{CP}_1$ is LOW, as this would cause an extra count.

Figure 11 shows an example of a divide-by 2 through divide-by 10 circuit using one “4017”. Since “4017” has an asynchronous reset, the output pulse widths are narrow (minimum expected pulse width is 6 ns). The output pulse widths can be enlarged by inserting a RC network at the MR input.

