FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28828-1E

ASSP For Screen Display Control

CMOS

On-Screen Display Controller

MB90099

■ DESCRIPTION

The MB90099 is an on-screen display controller for displaying text and graphics on the TV screen. The three-channel output control function, compact package and low voltage operation make this device suitable for on-screen displays in portable devices including camera-integrated VTRs and digital still cameras.

The MB90099 controls a display area of 28 characters by 12 lines, and provides 1,024 different characters, each composed of 12 × 18 dots. All 1,024 characters in font ROM can be set by the user. The display functions include a wealth of character with qualifying functions such as character background shading (shadow casting) and individual character size setting, with 16-color display selection for each character. Also included are the line background, screen background, and sprite character functions, providing a wide variety of screen display capabilities.

■ FEATURES

- Character screen configuration : 28 characters × 12 lines (maximum)
- Character types : 1,024 characters (integrated in ROM, user definable through the entire area)

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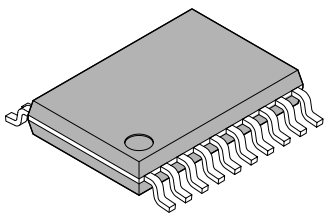
■ PACKAGE

20-pin Plastic SSOP



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- Font configuration : 12 × 18 dots (font ROM comfiguration)

  Horizontal/vertical character display size setting enabled.

  Two horizontal width settings (S/L) per character.
  S size : 6 dots
  L size : 12 dots

  Two vertical height settings (HA/HB) per line.
  HA : 18 dots
  HB : 12 dots

- Display modes : Character trimming : Enbled/Disabled (set for each line)

  Character background :
  None/Solid-fill/Shaded background (concaved) /Shaded background (convexed) (set for each character)

  Horizontal character merge/independent display with shaded background (set for each character)

  Vertical line merge/independent display with shaded background (set for each line)

  Character background display extended to line spacings : Enbled/Disabled (set for each line)

  Line background :
  None/Solid-fill/Shaded background (concaved) /Shaded background (convexed) (set for each line)
  (Display extends into left and right screen margins and into line spacings)

  Character enlargement :
  4 types : Normal, Double width, Double height, Double width × double height (set for each line)
  Enlarged character dot interpolation function (set for each line)

- Character screen display position control : Horizontal display position :
  Control in 2-dot units (movable through the entire screen)

  Vertical display position :
  Control in 2-dot units (movable through the entire screen)

  Line spacing control :
  Control in 1-dot units (set between 0 to 7 dots for each line, applied simultaneously to two areas above and below the line)

- Sprite character control : Sprite character display : Enable/Disabled

  Sprite character types : 256 types (character codes 000_H to $0FF_H$)

  Sprite character trimming : Enabled/Disabled

  Sprite character configuration : 2 types : 1 character/Stack of 2 characters

  Sprite character horizontal display position : Control in 1-dot units (movable through the entire screen)

  Sprite character vertical display position : Control in 1-dot units (movable through the entire screen)

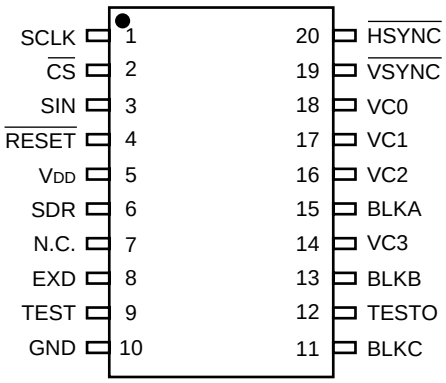
- Screen background control : Screen background color : Enabled/Disabled

- Display colors : Character color : 16 colors (set for each character)
  Character trimming color : 16 colors (set for each line)
  Character background color : 16 colors (set for each character) *
  Line background color : 16 colors (set for each line)
  Screen background color : 16 colors
  Sprite character color : 16 colors
  Sprite character trimming color : 16 colors
  Shaded background frame highlight color : 16 colors
  Shaded background frame shadow color : 16 colors
- Display signal output : Color signal output : 4 bits (supports 16 colors)
  Display period signals : 3 channels (output selector circuit provided)
- External interface : 16-bit serial input :
  Chip select
  Serial clock
  Serial data
- Package : SSOP-20
- Supply voltage : 2.4 V to 3.6 V

* : Character background color (color code) = “0” is transparent (displays lower-layer color) .

■ PIN ASSIGNMENT

(TOP VIEW)

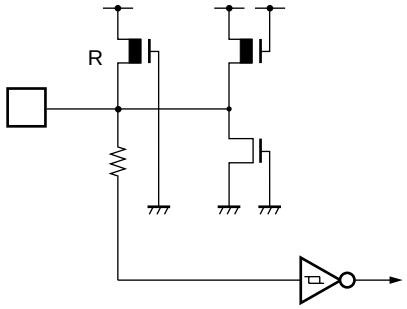
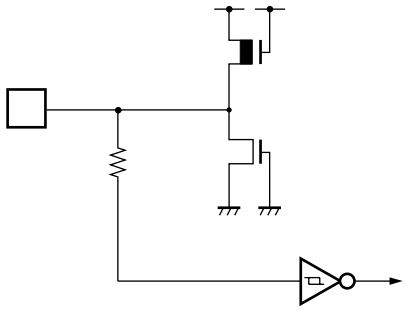
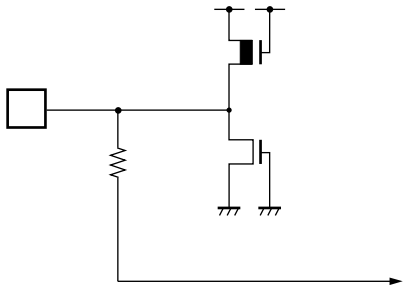
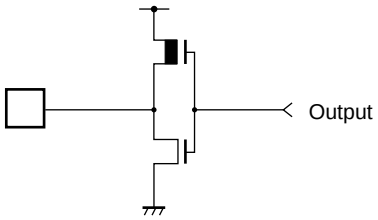


(FPT-20P-M03)

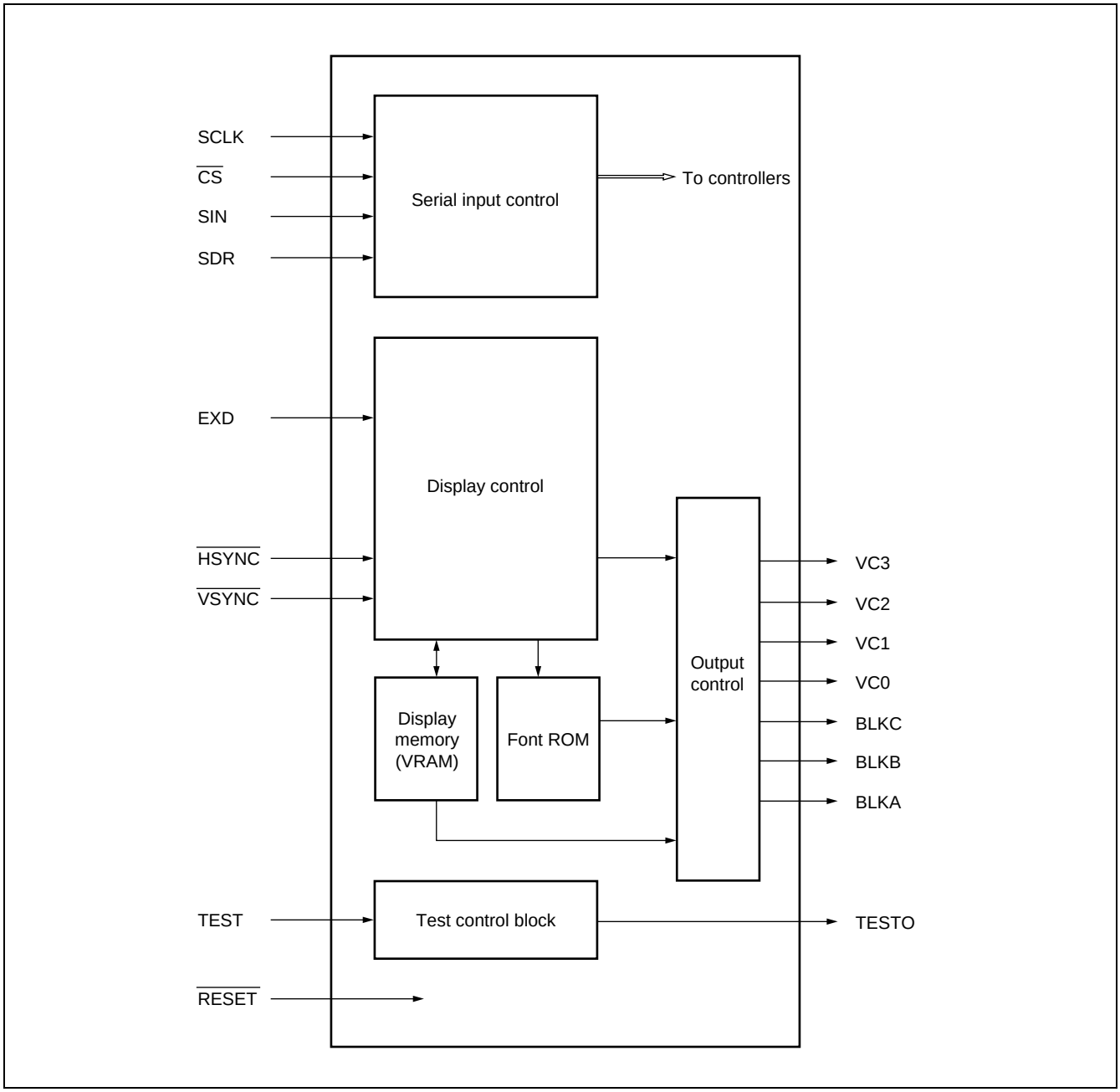
■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O	Circuit type	Function
1	SCLK	I	A	Shift clock input pin for serial transfer. This pin has an internal pull-up resistor.
2	$\overline{CS}$	I	A	Chip select pin. Input a low level signal during serial transfer. This pin has an internal pull-up resistor.
3	SIN	I	A	Serial data input pin. This pin has an internal pull-up resistor.
4	$\overline{RESET}$	I	B	Reset input pin. Input a low level signal at power-on time.
5	V_{DD}	—	—	+3 V power supply pin.
6	SDR	I	C	Data input direction select pin for serial transfer. Input a low level signal at LSB-first transfer mode, or a high level signal at MSB-first transfer mode.
7	N.C.	—	—	Not connected. This pin should be left open.
8	EXD	I	B	Display dot clock input pin.
9	TEST	I	C	LSI test input pin. Input a low level signal during normal use.
10	GND	—	—	Ground pin.
11	BLKC	O	D	Display period signal output pin for output channel C.
12	TESTO	O	D	LSI test output pin. This pin should be left open during normal use.
13	BLKB	O	D	Display period signal output pin for output channel B.
15	BLKA	O	D	Display period signal output pin for output channel A.
14 16 17 18	VC3 VC2 VC1 VC0	O O O O	D	Color code signal output pins.
19	$\overline{VSYNC}$	I	B	Vertical synchronization signal input pin.
20	$\overline{HSYNC}$	I	B	Horizontal synchronization signal input pin.

■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		CMOS level, hysteresis input, pull-up resistance (25 kΩ to 200 kΩ) .
B		CMOS level, hysteresis input.
C		CMOS level input.
D		CMOS level output.

■ BLOCK DIAGRAM



■ COMPONENT ELEMENTS

- Serial input control block
  Receives serial commands and data. Decodes commands, and allocates commands and data to the appropriate control blocks.
- Display control block
  Performs display control functions synchronized with the input sync signals.
- Display memory (VRAM) block
  VRAM memory for character data (24 bits × 28 characters × 12 lines) and line data (24 bits × 12 lines) .
- Font ROM block
  ROM memory for display character fonts. Configured for 1,024 characters of 12 dots × 18 dots.
- Output control block
  Generates output signals by applying display processing to the font data read from the font ROM.
- Test control block
  Circuits for factory testing of the LSI before delivery.

■ ABSOLUTE MAXIMUM RATINGS

(V_{GND} = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{DD}	V_{GND} – 0.5	V_{GND} + 4.0	V	
Input voltage	V_{IN}	V_{GND} – 0.5	V_{DD} + 0.5	V	
Output voltage	V_{OUT}	V_{GND} – 0.5	V_{DD} + 0.5	V	
Power consumption	Pd	—	100	mW	
Operating temperature	Ta	–20	+70	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(V_{GND} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{DD}	2.4	3.6	V	
“H” level input voltage 1	V_{IHS}	0.8 × V_{DD}	V_{DD} + 0.3	V	*1
“L” level input voltage 1	V_{ILS}	V_{GND}	0.2 × V_{DD}	V	*1
“H” level input voltage 2	V_{IH}	0.7 × V_{DD}	V_{DD} + 0.3	V	*2
“L” level input voltage 2	V_{IL}	V_{GND}	0.3 × V_{DD}	V	*2
Operating temperature	Ta	–20	+70	°C	

*1 : Input pins excluding TEST and SDR pins.

*2 : TEST and SDR input pins.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{GND} = 0 V, Ta = –20 °C to +70 °C)

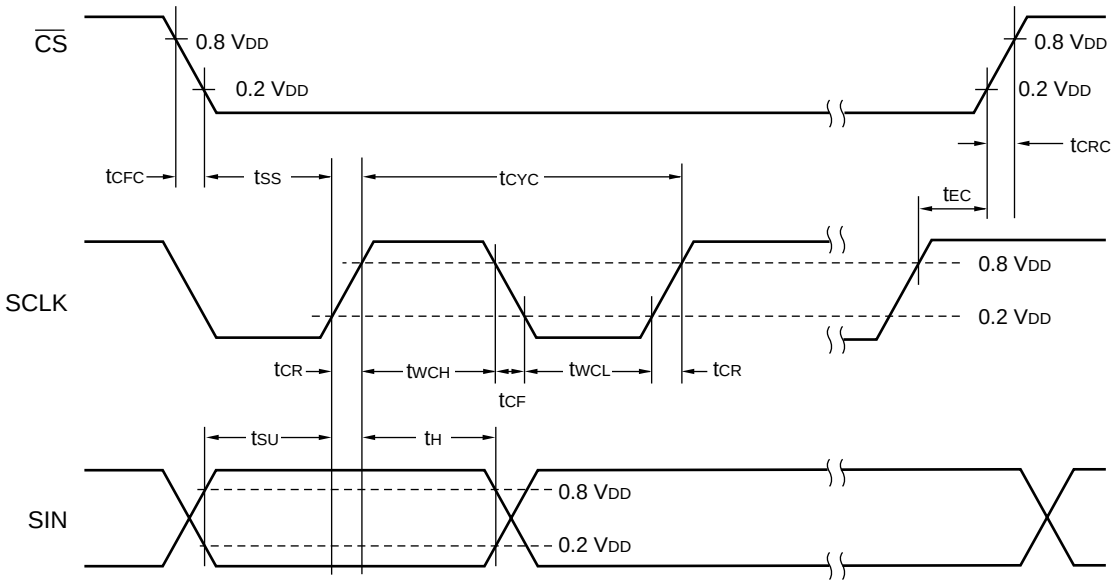
Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
"H" level output voltage	V_{OH}	VC3, VC2, VC1, VC0, BLKC, BLKB, BLKA	V_{DD} = 3.3 V I_{OH} = –4 mA	V_{DD} – 0.5	—	V_{DD}	V
"L" level output voltage	V_{OL}		V_{DD} = 3.3 V I_{OL} = 4 mA	V_{GND}	—	0.4	V
"H" level input current	I_{IH}	SDR, $\overline{HSYNC}$, $\overline{VSYNC}$, EXD, TEST, $\overline{RESET}$	V_{DD} = 3.3 V V_{IH} = V_{DD}	—	—	+10	µA
"L" level input current	I_{IL}		V_{DD} = 3.3 V V_{IL} = 0 V	—	—	–10	µA
Pull-up resistance	R_{PULL}	SIN, SCLK, $\overline{CS}$	V_{DD} = 3.3 V	25	50	200	kΩ
Power supply current	I_{CC}	V_{DD}	V_{DD} = 2.4 V f_{DC} = 8 MHz	—	—	5	mA
			V_{DD} = 3.6 V f_{DC} = 8 MHz	—	—	6	mA
Input capacitance	C	Except V_{DD}, GND	—	—	—	16	pF

2. AC Characteristics

(1) Serial input timings

(V_{DD} = 2.4 V to 3.6 V, V_{GND} = 0 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min.	Max.	
Shift clock cycle time	t_{CYC}	SCLK	250	—	ns
Shift clock pulse width	t_{WCH}	SCLK	100	—	ns
	t_{WCL}		100	—	ns
Shift clock signal rise/fall time	t_{CR}	SCLK	—	200	ns
	t_{CF}		—	200	ns
Shift clock start time	t_{SS}	SCLK	100	—	ns
Data setup time	t_{SU}	SIN	100	—	ns
Data hold time	t_H		50	—	ns
Chip select end time	t_{EC}	$\overline{CS}$	100	—	ns
Chip select signal rise/fall time	t_{CRC}	$\overline{CS}$	—	200	ns
	t_{CFC}		—	200	ns



(2) Vertical and horizontal sync signal input timing

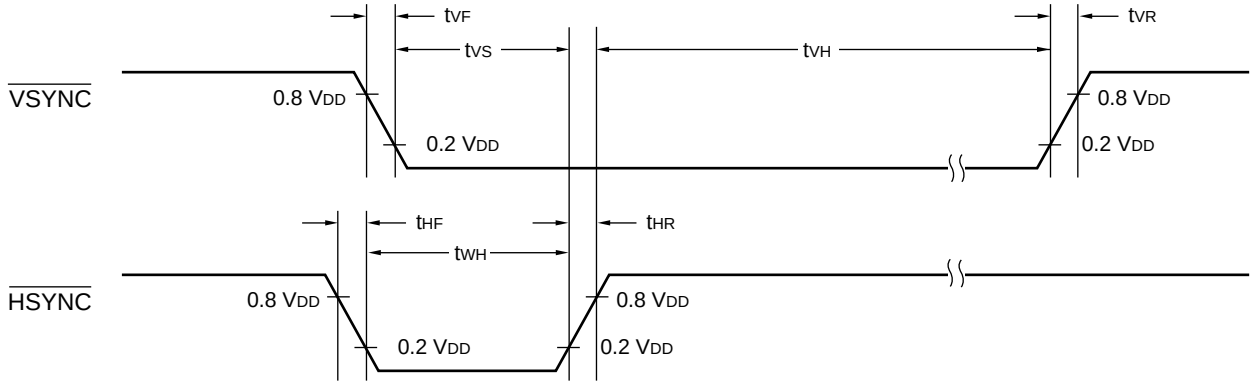
(V_{DD} = 2.4 V to 3.6 V, V_{GND} = 0 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min.	Max.	
Horizontal sync signal rise time	t_{HR}	$\overline{HSYNC}$	—	200	ns
Horizontal sync signal fall time	t_{HF}		—	200	ns
Vertical sync signal rise time	t_{VR}	$\overline{VSYNC}$	—	200	ns
Vertical sync signal fall time	t_{VF}		—	200	ns
Horizontal sync signal pulse width *1	t_{WH}	$\overline{HSYNC}$	18	—	Dot clock
			—	6	µs
Vertical sync signal detection setup time*2	t_{VS}	$\overline{VSYNC}$	4	1H – 4	Dot clock
Vertical sync signal detection hold time	t_{VH}	$\overline{VSYNC}$	2	20	h

*1 : During the horizontal sync signal pulse period, the MB90099 stops its internal operation, disabling writing to the internal VRAM. Therefore, the horizontal sync signal pulse width and VRAM write cycle (command 2 or command 4 issuance cycle) should be set so that the horizontal sync signal pulse width is shorter than the VRAM write cycle.

*2 : In the vertical sync signal detection cycle, do not change the vertical sync signal (detection edge) when it is close to the horizontal sync signal edge. This may result in distortion of the display due to fluctuations in the sync signal.

- $\overline{VSYNC}$: Leading-edge operation
  $\overline{HSYNC}$: $\overline{VSYNC}$ detection at the trailing edge



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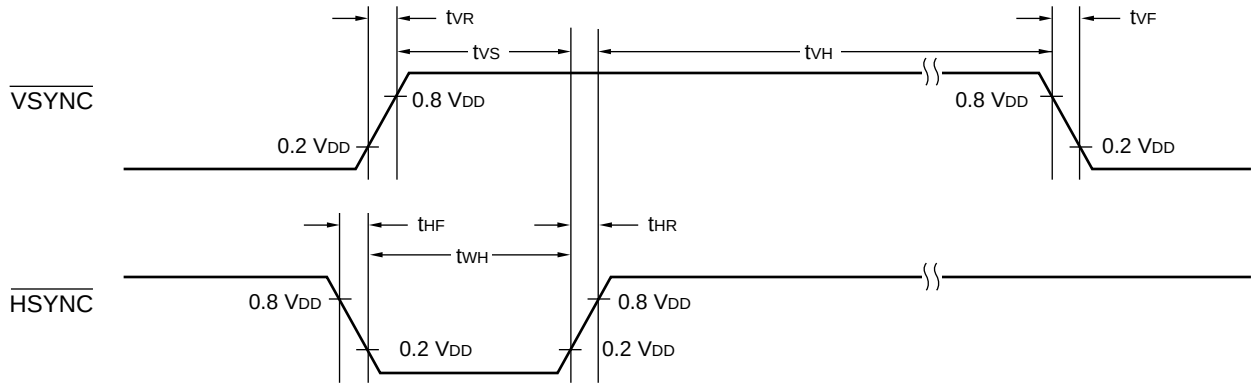
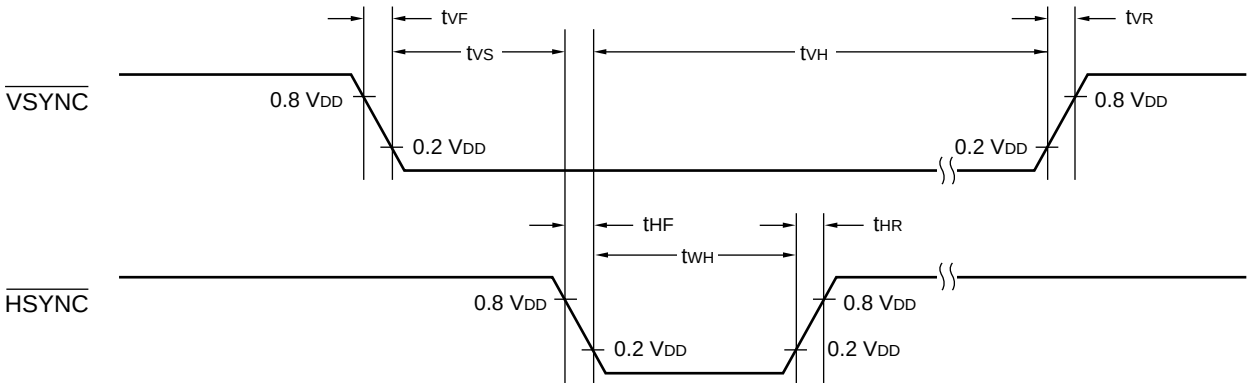
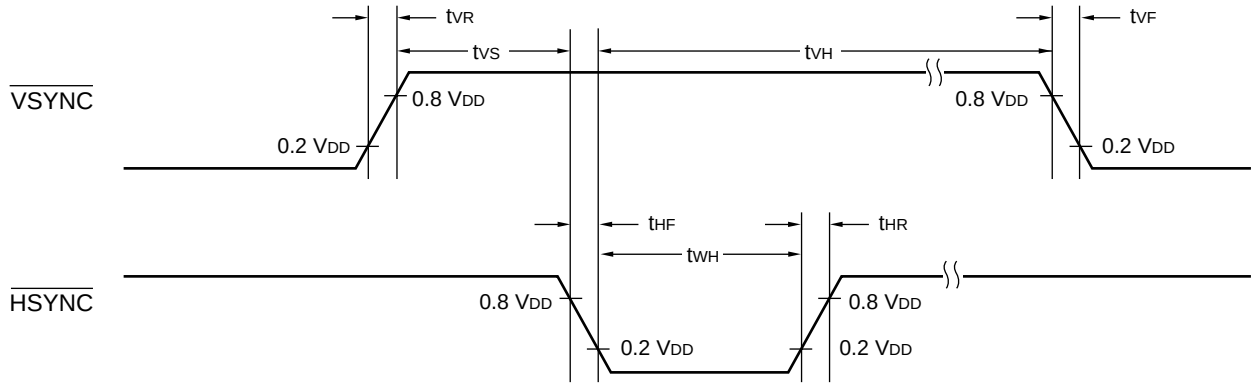
- $\overline{\text{VSYNC}}$: Trailing-edge operation
  $\overline{\text{HSYNC}}$: $\overline{\text{VSYNC}}$ detection at the trailing edge



- $\overline{\text{VSYNC}}$: Leading-edge operation
  $\overline{\text{HSYNC}}$: $\overline{\text{VSYNC}}$ detection at the leading edge



- $\overline{\text{VSYNC}}$: Trailing-edge operation
  $\overline{\text{HSYNC}}$: $\overline{\text{VSYNC}}$ detection at the leading edge



Note : The above diagrams assume that I/O pin control command (command 13-0) has set the sync signal input logic control setting (SIX bit) to negative logic (“0”) . However, if the positive logic setting (SIX bit = “1”) is used, the H and L levels are reversed.

(3) Dot clock external input timing

(V_{DD} = 2.7 V to 3.3 V, V_{GND} = 0 V, Ta = –20 °C to +70 °C)

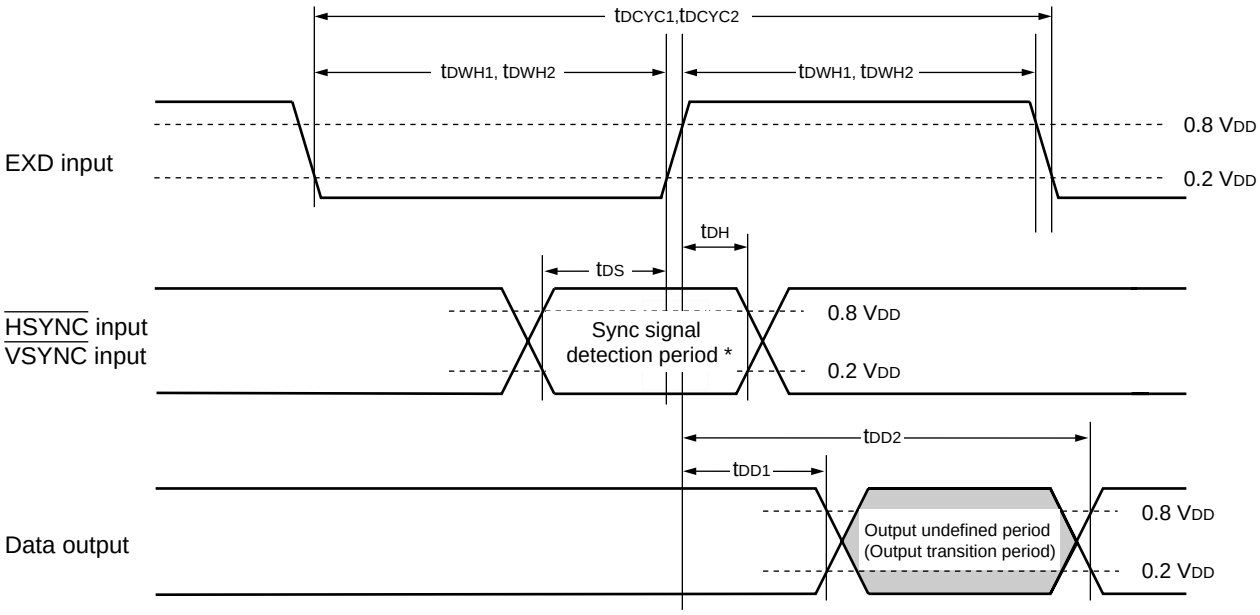
Parameter	Symbol	Pin name	Value		Unit	Note
			Min.	Max.		
Dot clock cycle time	t_{DCYC1}	EXD	112	166	ns	*1
	t_{DCYC2}	EXD	56	83	ns	*2
Dot clock pulse time	t_{DWH1}	EXD	48	—	ns	*1
	t_{DWL1}		48	—	ns	
	t_{DWH2}	EXD	24	—	ns	*2
	t_{DWL2}		24	—	ns	
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ setup time	t_{DS}	$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$	13	—	ns	*3
$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$ hold time	t_{DH}		0	—	ns	*3
Data output delay time 1	t_{DD1}	VC3, VC2, VC1, VC0, BLKA, BLKB, BLKC	7	t_{DD2}	ns	*3
Data output delay time 2	t_{DD2}		t_{DD1}	45	ns	

Note : The above items assume a supply voltage of V_{DD} = 2.7 V to 3.3 V.

*1 : Assuming input frequency = dot clock × 1.

*2 : Assuming input frequency = dot clock × 2.

*3 : Assuming input frequency = dot clock × 1 or dot clock × 2.



AC measurement conditions

C = 70 pF	V_{OH} = 0.8 V_{DD}
t_r = 5 ns	V_{OL} = 0.2 V_{DD}
t_f = 5 ns	V_{IH} = 0.8 V_{DD}
	V_{IL} = 0.2 V_{DD}

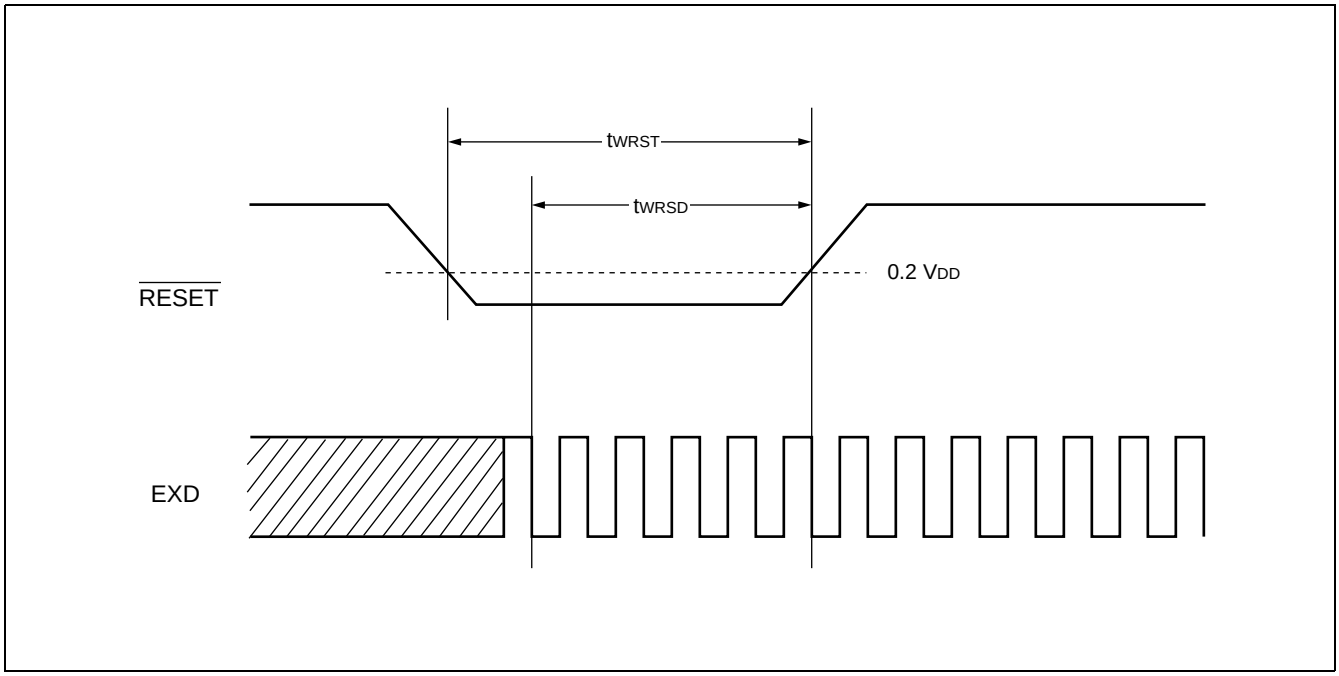
* : Do not vary the input sync signal during the sync signal detection period.
Changes in the signal during this period may cause distortion in the display.

(4) Reset input timing

(V_{DD} = 2.4 V to 3.6 V, V_{GND} = 0 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Pin name	Value		Unit	Note
			Min.	Max.		
Reset pulse width	t_{WRST}	$\overline{RESET}$	1	—	µs	
Clock input	t_{WRSD}	EXD	5	—	Dot clock	*

* : Clock input is required during reset.



■ DISPLAY CONTROL COMMANDS

1. Command list

Com-mand no.	Function	Command code/data												
		15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
0	VRAM write address setting	0 0 0 0	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0
1	Character data setting 1	0 0 0 1	MO1	MO0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0
2	Character data setting 2	0 0 1 0	MR	MS	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
3	Line control data setting 1	0 0 1 1	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0
4	Line control data setting 2	0 1 0 0	LDS	LGS	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0
5-00	Screen output control 1A	0 1 0 1	0	0	0	0	SDS	UDS	0	DSP	0	OA2	OA1	OA0
5-01	Screen output control 1B	0 1 0 1	0	0	0	1	SOB	BGB	BLB	0	0	OB2	OB1	OB0
5-02	Screen output control 1C	0 1 0 1	0	0	1	0	SOC	BGC	BLC	0	0	OC2	OC1	OC0
5-2	Vertical display position control	0 1 0 1	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
5-3	Horizontal display position control	0 1 0 1	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0
6-1	Shaded background frame color control	0 1 1 0	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0
7-3	Screen background control	0 1 1 1	1	1	0	0	0	0	0	0	U3	U2	U1	U0
8-0	Sprite character control 1	1 0 0 0	0	0	SFB	SFA	SF3	SF2	SF1	SF0	SC3	SC2	SC1	SC0
8-1	Sprite character control 2	1 0 0 0	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0
9-0	Sprite character control 4	1 0 0 1	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0
9-1	Sprite character control 5	1 0 0 1	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0
11-0	Screen extension control	1 0 1 1	0	0	0	0	0	EG0	0	0	0	0	0	0
11-2	Dot clock control 1	1 0 1 1	1	0	0	0	0	0	0	0	0	DC2	DC1	DC0

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Com-mand no.	Function	Command code/data												
		15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
13-0	I/O pin control	1 1 0 1	0	0	VVE	VHE	HE	0	SIX	0	0	0	DBX	DCX
13-1	Horizontal blanking control 1	1 1 0 1	0	1	0	0	0	0	BB5	BB4	BB3	BB2	BB1	BB0
13-2	Horizontal blanking control 2	1 1 0 1	1	0	0	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0

2. Command Description

- **Command 0 (VRAM write address setting)**

Command 0 sets the write address in VRAM, and controls the execution of “VRAM fill”. The write address is specified by row and column addresses. VRAM fill is activated by executing character data setting 2 (command 2) .

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0

AY3 to AY0 : Row address (0 to B_H)

AX4 to AX0 : Column address (0 to $1B_H$)

FL : VRAM Fill control (0 : OFF, 1 : ON)

- **Command 1 (Character data setting 1)**

Command 1 specifies character data. The character data is written to VRAM and reflected on the screen by the execution of command 2 (character data setting 2) .

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	MO1	MO0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0

MO1, MO0 : Character output control

MM1, MM0 : Character background control
(0, 0 : Off)
(0, 1 : Solid fill)
(1, 0 : Concaved shaded)
(1, 1 : Convexed shaded)

MC3 to MC0 : Character color (16 colors)

MB3 to MB0 : Background color (16 colors)

- **Command 2 (Character data setting 2)**

Command 2 writes additional character data to the location in VRAM spacified by command 0 (VRAM write address setting),along with the character data set by command 1 (caracter data setting 1).

The VRAM write address is automatically incremented after command 2 is executed.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	MR	MS	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0

MR : Shaded background succeeding character merge control
(0 : Not merged with succeeding character)
(1 : Merged with succeeding character)

MS : Character horizontal size control
(0 : S size, 6 dots)
(1 : L size, 12 dots)

M9 to M0 : Character code

- **Command 3 (Line control data setting 1)**

Command 3 specifies line control data. The line control data is written to VRAM and reflected on the screen by the execution of command 4 (line control data setting 2) .

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0

LHS : Line character vertical size type control
(0 : Character vertical size A)
(1 : Character vertical size B)

LW2 to LW0 : Line spacing control
(0 to 7 dots, in 1-dot units)

LF3 to LF0 : Trimming color (16 colors)

LFD, LFC : Trimming output control
(0, 0 : All Off)
(0, 1 : Trimming On for character only, no character background)
(1, 0 : Trimming On for solid-fill character only, no character background)
(1, 1 : All On)

LFB, LFA : Trimming control
(0, 0 : Trimming Off)
(0, 1 : Reserved (setting prohibited))
(1, 0 : Reserved (setting prohibited))
(1, 1 : Eight-direction trimming)

- **Command 4 (Line control data setting 2)**

Command 4 specifies additional line control data and writes this data, along with the line control data set by command 3 (line control data setting 1) to the row address in VRAM specified by command 0 (VRAM write address setting) .

Executing this command will not alter the VRAM write address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	LDS	LGS	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0

LDS : Line character output control (control of character + trimming + character background)
(0 : Off, 1 : On)

LGS : Line enlargement interpolation control
(0 : Off, 1 : On)

LG1, LG0 : Line enlargement control
(0, 0 : Normal)
(0, 1 : Double width)
(1, 0 : Double height)
(1, 1 : Double width × double height)

LE : Character background extension control
(0 : Normal, 1 : Extended)

LD : Shaded background succeeding line merge control
(0 : Independent)
(1 : Merged with succeeding line)

LM1, LM0 : Line background control
(0, 0 : Off)
(0, 1 : Solid fill)
(1, 0 : Concaved shaded)
(1, 1 : Convexed shaded)

L3 to L0 : Line background color (16 colors)

- **Command 5-00 (Screen output control 1A)**

Command 5-00 controls screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0	SDS	UDS	0	DSP	0	OA2	OA1	OA0

SDS : Sprite character output control
(0 : Off, 1 : On) *

UDS : Screen background output control
(0 : Off, 1 : On) *

DSP : Display output control (Control of character + trimming + character background + line background)
(0 : Off, 1 : On) *

OA2 to OA0 : Output-A character control (8 types)

* : Input of an 'L' level signal to the $\overline{\text{RESET}}$ pin will initialize SDS = 0, UDS = 0, and DSP = 0.

- **Command 5-01 (Screen output control 1B)**

Command 5-01 controls output-B screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	1	SOB	BGB	BLB	0	0	OB2	OB1	OB0

SOB : Output-B sprite character output control
(0 : Off, 1 : On)

BGB : Output-B screen background output control
(0 : Off, 1 : On)

BLB : Output-B line background output control
(0 : Off, 1 : On)

OB2 to OB0 : Output-B character control (8 types)

• **Command 5-02 (Screen output control 1C)**

Command 5-02 controls output-C screen display output.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	0	SOC	BGC	BLC	0	0	OC2	OC1	OC0

SOC : Output-C sprite character output control
(0 : Off, 1 : On)

BGC : Output-C screen background output control
(0 : Off, 1 : On)

BLC : Output-C line background output control
(0 : Off, 1 : On)

OC2 to OC0 : Output-C character control (8 types)

• **Command 5-2 (Vertical display position control)**

Command 5-2 controls the vertical display position on the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Y8 to Y0 : Vertical display position control (0 to 1022 in 2-dot units)

• **Command 5-3 (Horizontal display position control)**

Command 5-3 controls the horizontal display position on the screen.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0

X8 to X0 : Horizontal display position control (0 to 1022 in 2-dot units)

• **Command 6-1 (Shaded background frame color control)**

Command 6-1 controls the frame color of the shaded background.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0

BH3 to BH0 : Shaded background frame highlight color (16 colors)

BS3 to BS0 : Shaded background frame shadow color (16 colors)

• **Command 7-3 (Screen background control)**

Command 7-3 controls the screen background color.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	0	0	0	0	0	U3	U2	U1	U0

U3 to U0 : Screen background color (16 colors)

- **Command 8-0 (Sprite character control 1)**

Command 8-0 controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	SFB	SFA	SF3	SF2	SF1	SF0	SC3	SC2	SC1	SC0

SFB, SFA : Sprite character trimming control
(0, 0 : Trimming Off)
(0, 1 : Reserved)
(1, 0 : Reserved)
(1, 1 : Eight-direction trimming)

SF3 to SF0 : Sprite character trimming color (16 colors)

SC3 to SC0 : Sprite character color (16 colors)

- **Command 8-1 (Sprite character control 2)**

Command 8-1 controls sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0

SD1, SD0 : Sprite character configuration control
(0, 0 : 1 character)
(0, 1 : Reserved (setting prohibited))
(1, 0 : Stack of 2 characters)
(1, 1 : Reserved (setting prohibited))

SM7 to SM0 : Sprite character code
(000_H to $0FF_H$ for 256 different characters)

- **Command 9-0 (Sprite character control 4)**

Command 9-0 controls the vertical display position of sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0

SY9 to SY0 : Sprite character vertical display position control
(0 to 1023 in 1-dot units)

- **Command 9-1 (Sprite character control 5)**

Command 9-1 controls the horizontal display position of sprite characters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0

SX9 to SX0 : Sprite character horizontal display position control
(0 to 1023 in 1-dot units)

• **Command 11-0 (Screen extension control)**

(Reserved)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	0	EG0	0	0	0	0	0	0

EG0 : (Reserved)
(0 : Normal)
(1 : Reserved (setting prohibited))

• **Command 11-2 (Dot clock control 1)**

Command 11-2 controls dot clock selection.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	0	0	0	0	0	0	0	0	DC2	DC1	DC0

DC2 to DC0 : Dot clock selection control
(0, 1, 0) : External dot clock input
(0, 1, 1) : Frequency-doubled external dot clock input

• **Command 13-0 (I/O pin control)**

Command 13-0 controls I/O pin functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	0	VVE	VHE	HE	0	SIX	0	0	0	DBX	DCX

VVE : Edge selection for vertical synchronization detection
(0 : Leading edge, 1 : Trailing edge)

VHE : HSYNC edge selection for vertical synchronization detection
(0 : Leading edge, 1 : Trailing edge)

HE : Edge selection for horizontal synchronization operation
(0 : Trailing edge, 1 : Leading edge)

SIX : Logic control for sync signal input
(0 : Negative logic, 1 : Positive logic)

DCX : Logic control for display color signal output
(0 : Positive logic, 1 : Negative logic) *

DBX : Logic control for display output period signal
(0 : Positive logic, 1 : Negative logic) *

* : Input of an 'L' level signal to the $\overline{\text{RESET}}$ pin will initialize DCX = 0, and DBX = 0.

• **Command 13-1 (Horizontal blanking control 1)**

Command 13-1 controls the back porch of the horizontal blanking function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	1	0	0	0	0	BB5	BB4	BB3	BB2	BB1	BB0

BB5 to BB0 : Back porch control (0 to 126, in 2-dot units)

- **Command 13-2 (Horizontal blanking control 2)**

Command 13-2 controls the front porch of the horizontal blanking function.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	1	0	0	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	BF0

BF8 to BF0 : Front porch control (0 to 1022, in 2-dot units)

3. Notes on Issuing Commands

(1) Initialization

When a reset signal is input (“L” level signal input to the $\overline{\text{RESET}}$ pin) , the MB90099 enters display-off state(*). The contents of VRAM (character RAM and line RAM) are undefined.

Immediately after release of the input signal to the MB90099, issue the following commands to initialize control operation.

- Dot clock control 1 (command 11-2)
- I/O pin control (command 13-0)

This must be done before setting all command data and all RAM contents. (VRAM settings require normal dot clock input and normal sync signal input.)

* : The reset input initializes control bits as follows.

Screen output control 1A (command 5-00)

SDS = 0 Sprite Off

UDS = 0 Screen background Off

DSP = 0 Character, character background, line background Off

I/O pin control (command 13-0)

DCX = 0 VC0, VC1, VC2, VC3 pins set to positive logic output

DBX = 0 BLKA, BLKB, BLKC pins set to positive logic output

(2) Command refresh

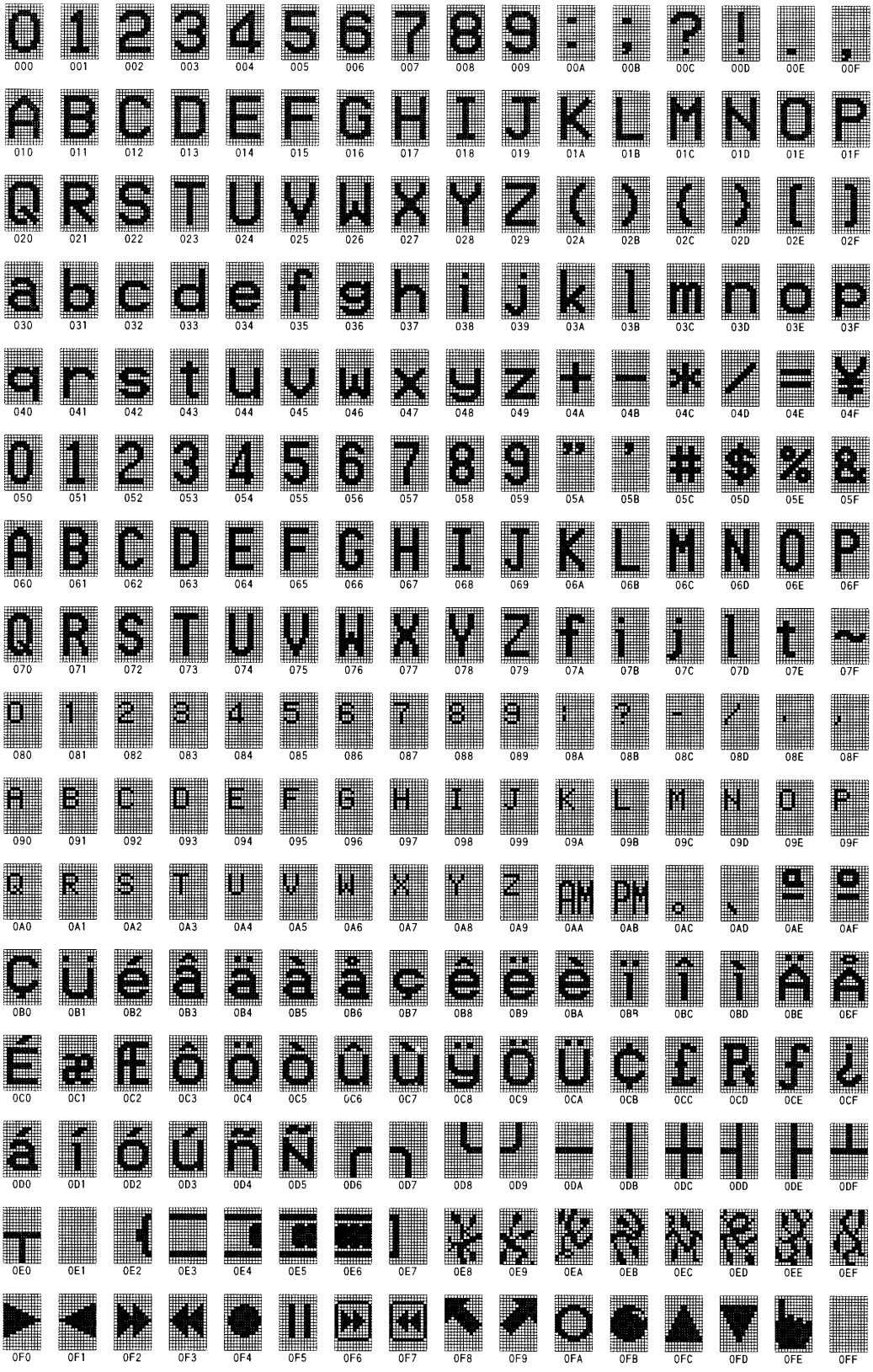
Command data to the MB90099 and the contents of internal VRAM are stored as long as power is supplied to the MB90099. However, there may be cases in which the serial control, sync, or dot clock signals become abnormal due to causes such as external noise, preventing the internal registers and VRAM from being set properly. It is therefore recommended that all command data and VRAM data be refreshed periodically to ensure that this data is correct.

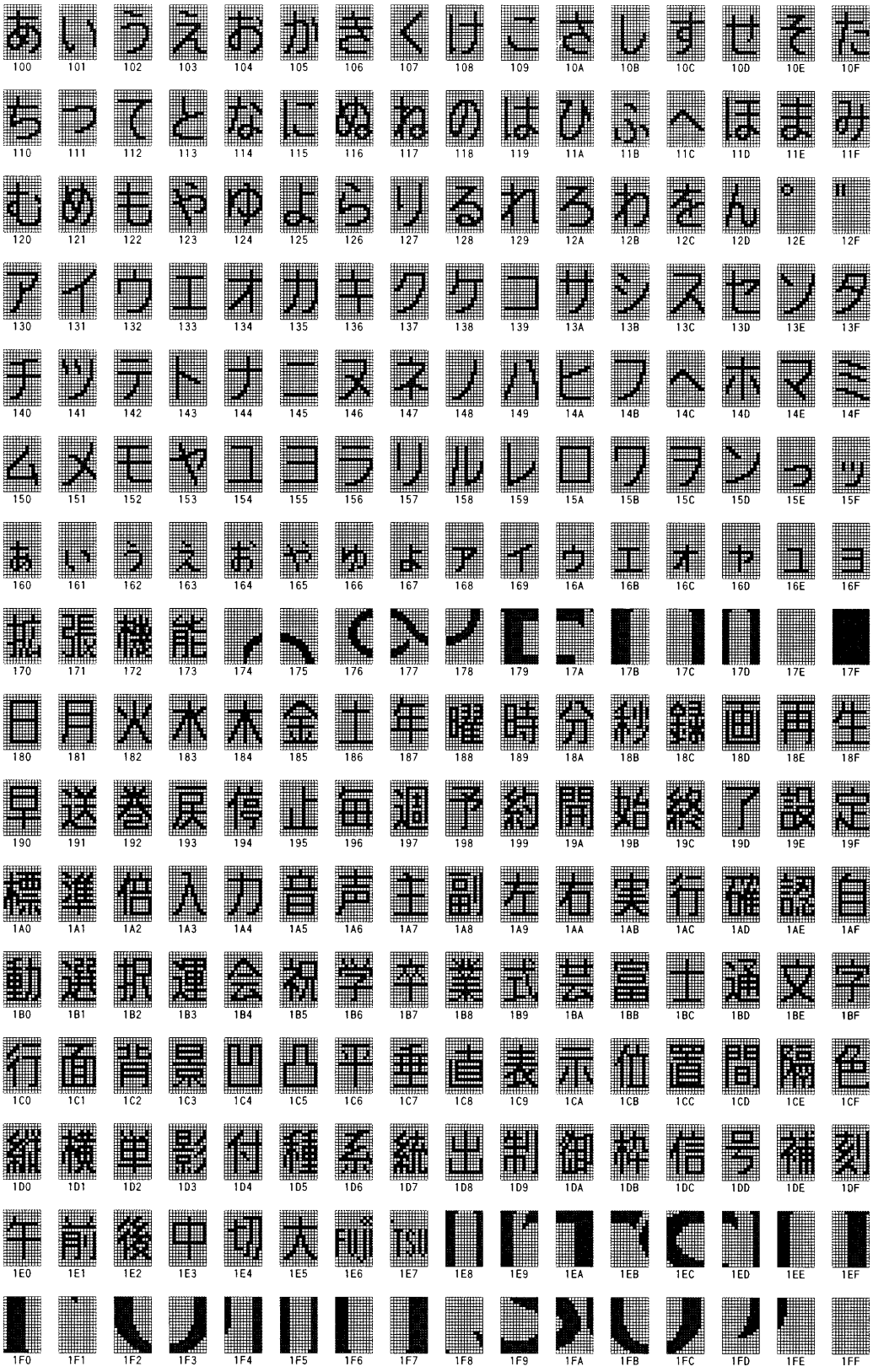
(3) Command issue timing

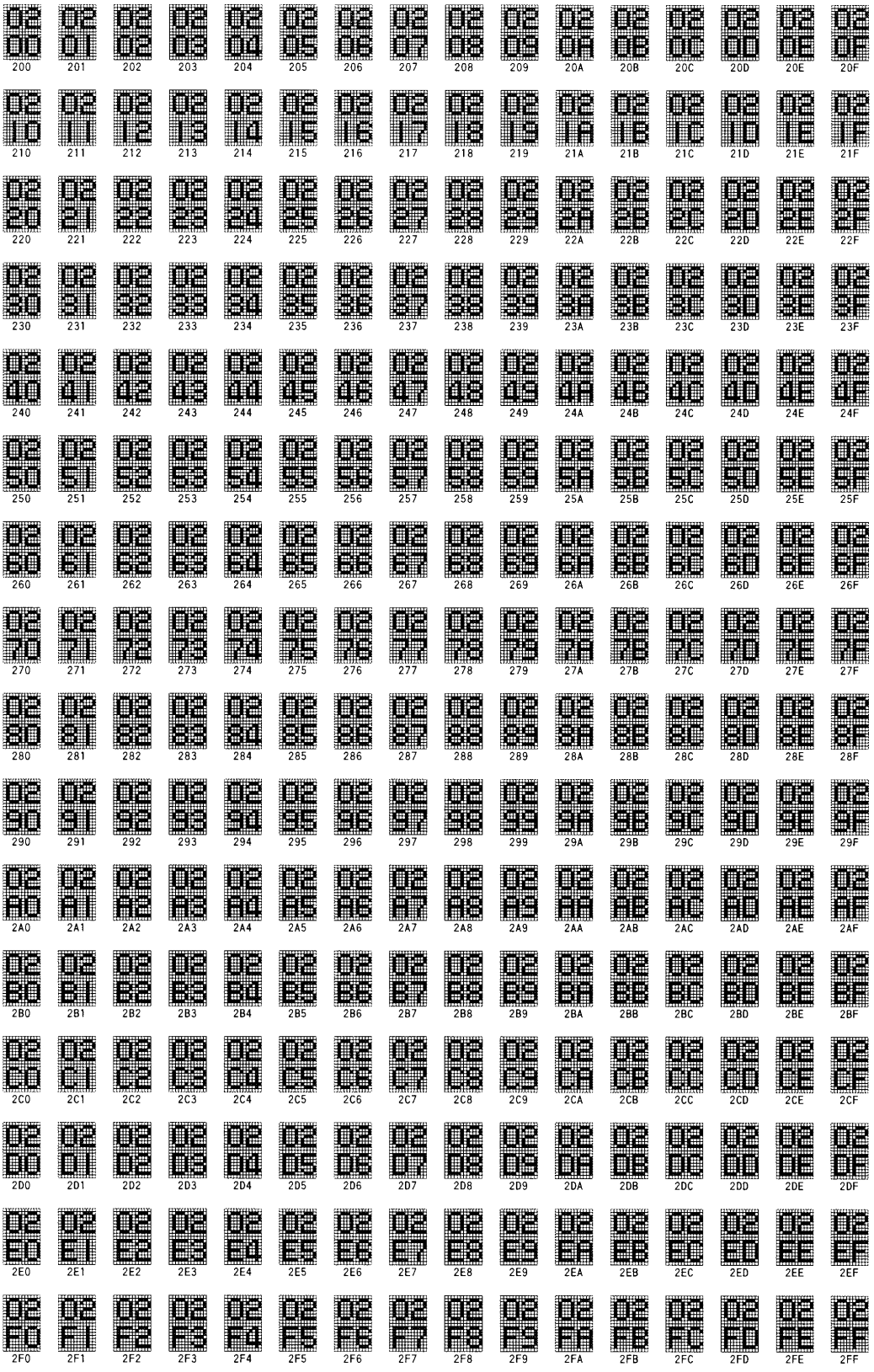
When any control command, including a VRAM write command such as a character data setting or line control data setting command is issued, the command is executed immediately and the result is reflected on the screen. When such a command is issued during a display period, the display in the relevant field may experience momentary distortion. To avoid this, it is recommended that commands be issued during the vertical blanking interval. However that with a command 5-00 (screen output control 1A) in which one or more of the DSP, SDS, or UDS control bits is switched from OFF to ON, the display will wait until the next vertical sync signal after the command is issued and the display will start from the top of the scanning field.

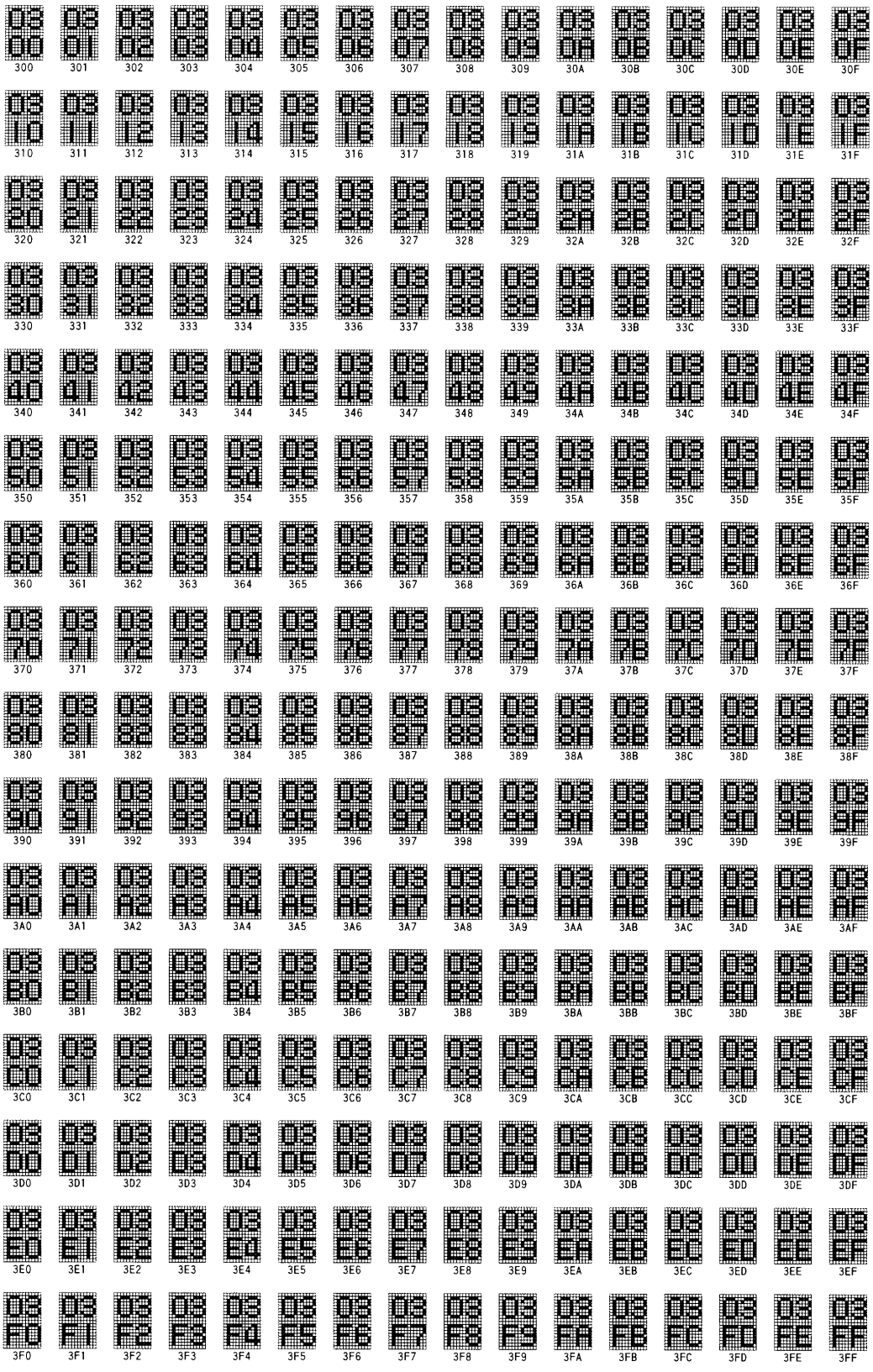
■ MB90099-001 FONT DATA

The MB90099-001 is a standard ROM product.





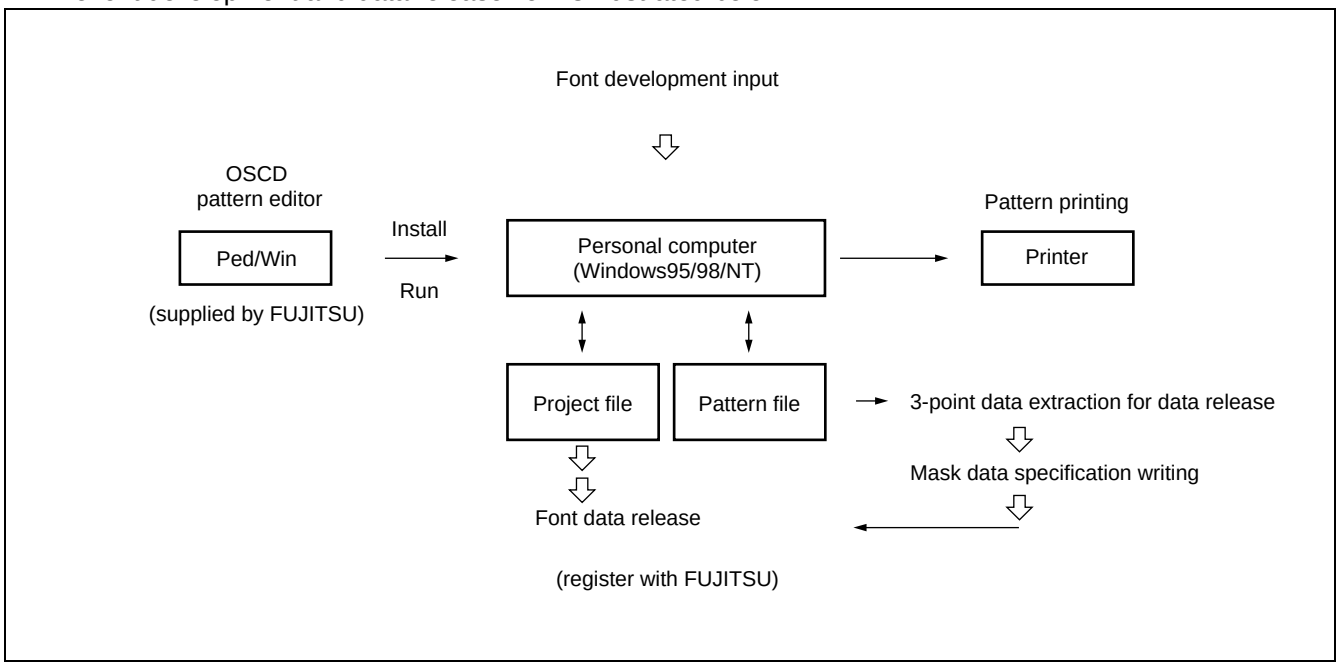

02 00 200
02 01 201
02 02 202
02 03 203
02 04 204
02 05 205
02 06 206
02 07 207
02 08 208
02 09 209
02 0A 20A
02 0B 20B
02 0C 20C
02 0D 20D
02 0E 20E
02 0F 20F
02 10 210
02 11 211
02 12 212
02 13 213
02 14 214
02 15 215
02 16 216
02 17 217
02 18 218
02 19 219
02 1A 21A
02 1B 21B
02 1C 21C
02 1D 21D
02 1E 21E
02 1F 21F
02 20 220
02 21 221
02 22 222
02 23 223
02 24 224
02 25 225
02 26 226
02 27 227
02 28 228
02 29 229
02 2A 22A
02 2B 22B
02 2C 22C
02 2D 22D
02 2E 22E
02 2F 22F
02 30 230
02 31 231
02 32 232
02 33 233
02 34 234
02 35 235
02 36 236
02 37 237
02 38 238
02 39 239
02 3A 23A
02 3B 23B
02 3C 23C
02 3D 23D
02 3E 23E
02 3F 23F
02 40 240
02 41 241
02 42 242
02 43 243
02 44 244
02 45 245
02 46 246
02 47 247
02 48 248
02 49 249
02 4A 24A
02 4B 24B
02 4C 24C
02 4D 24D
02 4E 24E
02 4F 24F
02 50 250
02 51 251
02 52 252
02 53 253
02 54 254
02 55 255
02 56 256
02 57 257
02 58 258
02 59 259
02 5A 25A
02 5B 25B
02 5C 25C
02 5D 25D
02 5E 25E
02 5F 25F
02 60 260
02 61 261
02 62 262
02 63 263
02 64 264
02 65 265
02 66 266
02 67 267
02 68 268
02 69 269
02 6A 26A
02 6B 26B
02 6C 26C
02 6D 26D
02 6E 26E
02 6F 26F
02 70 270
02 71 271
02 72 272
02 73 273
02 74 274
02 75 275
02 76 276
02 77 277
02 78 278
02 79 279
02 7A 27A
02 7B 27B
02 7C 27C
02 7D 27D
02 7E 27E
02 7F 27F
02 80 280
02 81 281
02 82 282
02 83 283
02 84 284
02 85 285
02 86 286
02 87 287
02 88 288
02 89 289
02 8A 28A
02 8B 28B
02 8C 28C
02 8D 28D
02 8E 28E
02 8F 28F
02 90 290
02 91 291
02 92 292
02 93 293
02 94 294
02 95 295
02 96 296
02 97 297
02 98 298
02 99 299
02 9A 29A
02 9B 29B
02 9C 29C
02 9D 29D
02 9E 29E
02 9F 29F
02 A0 2A0
02 A1 2A1
02 A2 2A2
02 A3 2A3
02 A4 2A4
02 A5 2A5
02 A6 2A6
02 A7 2A7
02 A8 2A8
02 A9 2A9
02 AA 2AA
02 AB 2AB
02 AC 2AC
02 AD 2AD
02 AE 2AE
02 AF 2AF
02 B0 2B0
02 B1 2B1
02 B2 2B2
02 B3 2B3
02 B4 2B4
02 B5 2B5
02 B6 2B6
02 B7 2B7
02 B8 2B8
02 B9 2B9
02 BA 2BA
02 BB 2BB
02 BC 2BC
02 BD 2BD
02 BE 2BE
02 BF 2BF
02 C0 2C0
02 C1 2C1
02 C2 2C2
02 C3 2C3
02 C4 2C4
02 C5 2C5
02 C6 2C6
02 C7 2C7
02 C8 2C8
02 C9 2C9
02 CA 2CA
02 CB 2CB
02 CC 2CC
02 CD 2CD
02 CE 2CE
02 CF 2CF
02 D0 2D0
02 D1 2D1
02 D2 2D2
02 D3 2D3
02 D4 2D4
02 D5 2D5
02 D6 2D6
02 D7 2D7
02 D8 2D8
02 D9 2D9
02 DA 2DA
02 DB 2DB
02 DC 2DC
02 DD 2DD
02 DE 2DE
02 DF 2DF
02 E0 2E0
02 E1 2E1
02 E2 2E2
02 E3 2E3
02 E4 2E4
02 E5 2E5
02 E6 2E6
02 E7 2E7
02 E8 2E8
02 E9 2E9
02 EA 2EA
02 EB 2EB
02 EC 2EC
02 ED 2ED
02 EE 2EE
02 EF 2EF
02 F0 2F0
02 F1 2F1
02 F2 2F2
02 F3 2F3
02 F4 2F4
02 F5 2F5
02 F6 2F6
02 F7 2F7
02 F8 2F8
02 F9 2F9
02 FA 2FA
02 FB 2FB
02 FC 2FC
02 FD 2FD
02 FE 2FE
02 FF 2FF


300 301 302 303 304 305 306 307 308 309 30A 30B 30C 30D 30E 30F
310 311 312 313 314 315 316 317 318 319 31A 31B 31C 31D 31E 31F
320 321 322 323 324 325 326 327 328 329 32A 32B 32C 32D 32E 32F
330 331 332 333 334 335 336 337 338 339 33A 33B 33C 33D 33E 33F
340 341 342 343 344 345 346 347 348 349 34A 34B 34C 34D 34E 34F
350 351 352 353 354 355 356 357 358 359 35A 35B 35C 35D 35E 35F
360 361 362 363 364 365 366 367 368 369 36A 36B 36C 36D 36E 36F
370 371 372 373 374 375 376 377 378 379 37A 37B 37C 37D 37E 37F
380 381 382 383 384 385 386 387 388 389 38A 38B 38C 38D 38E 38F
390 391 392 393 394 395 396 397 398 399 39A 39B 39C 39D 39E 39F
3A0 3A1 3A2 3A3 3A4 3A5 3A6 3A7 3A8 3A9 3AA 3AB 3AC 3AD 3AE 3AF
3B0 3B1 3B2 3B3 3B4 3B5 3B6 3B7 3B8 3B9 3BA 3BB 3BC 3BD 3BE 3BF
3C0 3C1 3C2 3C3 3C4 3C5 3C6 3C7 3C8 3C9 3CA 3CB 3CC 3CD 3CE 3CF
3D0 3D1 3D2 3D3 3D4 3D5 3D6 3D7 3D8 3D9 3DA 3DB 3DC 3DD 3DE 3DF
3E0 3E1 3E2 3E3 3E4 3E5 3E6 3E7 3E8 3E9 3EA 3EB 3EC 3ED 3EE 3EF
3F0 3F1 3F2 3F3 3F4 3F5 3F6 3F7 3F8 3F9 3FA 3FB 3FC 3FD 3FE 3FF

■ FONT DEVELOPMENT AND DATA RSLEASE

The MB90099 features the font ROM in which all 1024 characters are user-definable. For font data development, use the OSDC pattern editor Ped/Win. Ped/Win is an OSCD proprietary pattern editor for use on personal computers operating Windows95/98/NT4.0 (Japanese language) environments.

The font development and data release flow is illustrated below.



(1) Font data release

Font data is released in project files only. Pattern files should not be released. A portion of the pattern file data will be used for data matching in order to verify registration of release data by FUJITSU. For this reason, users are requested to write a portion of the pattern data content in mask data specifications.

Note : Pattern data output should not be generated until after the completion of font creation and project creation. Also, the project file should not be updated after pattern file generation is completed. If the project contents are updated after pattern file generation, pattern files should be generated again.

(2) Project files

After font data and other supplementary data is created, it is stored in a project file. Normally one project file is created for each model.

- **Project file names**
  Project file names should be in the format “MB90099-XXX” where “XXX” is a ROM number assigned by FUJITSU. Users should contact their FUJITSU sales representative. If no ROM number has been assigned, any number preceded by an alphabetic character may be used. Project files which are developed solely for test purposes and not intended for font release may be assigned any file name.
- **Comments related to new project files**
  Comment lines in the form of any desired character strings may be added at the time a project file is created. Comments will be printed when the font is printed, and can be modified as needed whenever that Ped/Win is operating.

(3) Pattern files

Font data may be placed in pattern files. Because pattern data is saved in the project file, normally it is only necessary to create a pattern file at the time of font release for the purpose of extracting verification data (writing to mask data specifications) . Pattern files should not be released.

- **Pattern file loading**
  Pattern files can be loaded for some OSCD models other than the MB90099.
- **Pattern file output generation**
  Do not create more than one pattern file for the same project. This may cause errors . In such cases, the project name should be altered to create another project.
- **Extracting verification data**
  Three data points, the first and last addresses and one other random address, should be extracted from pattern file data and written into the mask data specifications. The random address should not include the data values “00” or “FF.”

Note : Ped/Win display functions are based on OSDC specifications, however some display specifications may not be identical to actual OSDC specifications. Users should consult specification documents for details.

(Data comparison)

After data release, once ROM mask processing is completed FUJITSU will extract the ROM data used in this process. Users should verify that the extracted data is identical to the pattern file data that was submitted, and return a written statement of data comparison indicating whether that data is identical or not . If the data is not identical, contact FUJITSU’s sales representative immediately. Data errors may cause errors in ES production.

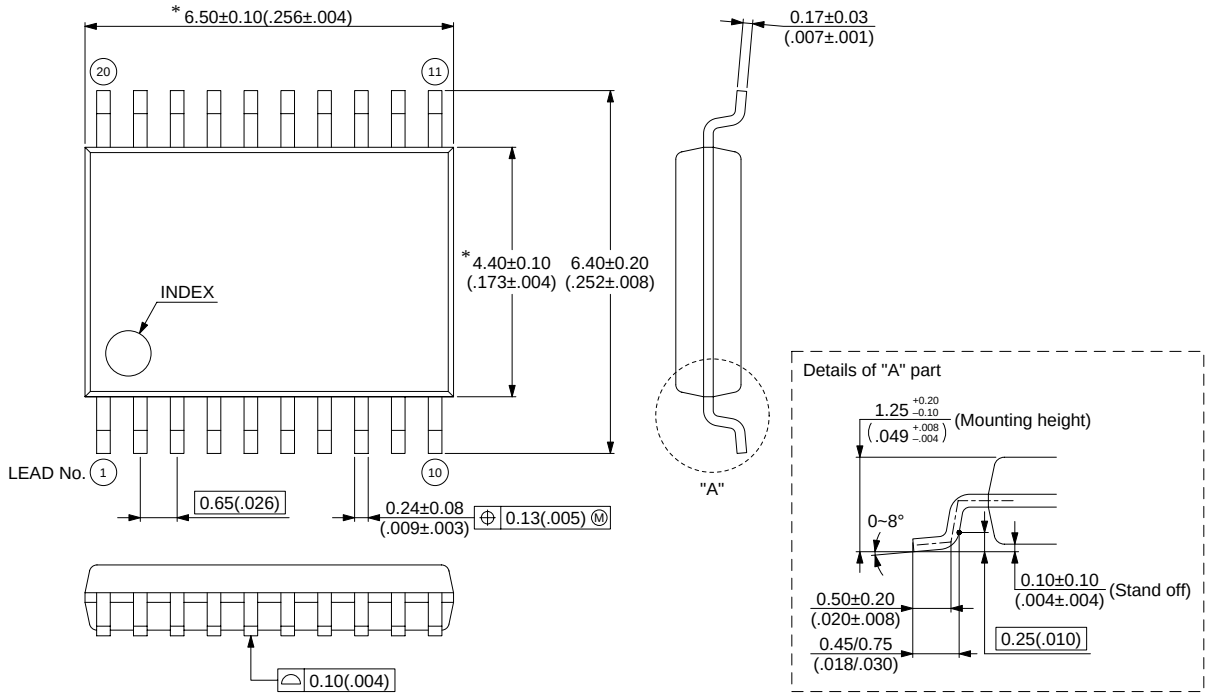
■ ORDERING INFORMATION

Model	Package	Remarks
MB90099PFV	20-pin Plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSION

20-pin Plastic SSOP
(FPT-20P-M03)

* : These dimensions do not include resin protrusion.



Dimensions in mm (inches)

FUJITSU LIMITED

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F0011

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Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.