TMP82C51AP-2 / TMP82C51AP-10
TMP82C51AM-2 / TMP82C51AM-10

PROGRAMMABLE COMMUNICATION INTERFACE

1. GENERAL DESCRIPTION

The TMP82C51A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART) that is fabricated using C-MOS silicon gate technology. The 82C51A is mainly used for 8-bit microcomputer extention system, which require serial data communications.

The TMP82C51AP-2/TMP82C51AP-10 is packaged in the 28 pin standard Dual Inline Package.

The TMP82C51AM-2/TMP82C51AM-10 is packaged in the 28 pin Small Out Line Package.

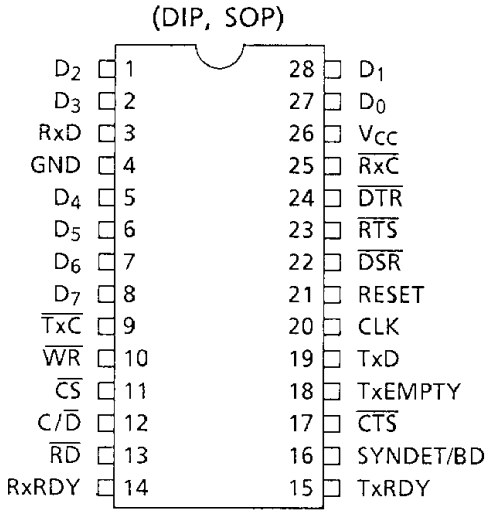
FEATURES

- Synchronous:
  5-8 Bit Characters
  Internal or External Character Synchronization
  Single or Double Character Synchronization (Inrternal)
  Automatic Sync Character(s) Insertion
- Asynchronous:
  5-8 Bit Characters
  Clock Rate -1, 16 or 64 Times Transfer Rate
  Break Character Generation
  1, 1.5 or 2 stop Bits
  False Start Bit Detection
  Automatic Break Detect and Handling
- Transfer Rate

	TMP82C51A-2	TMP82C51A-10
	DC-104K bps	DC-300K bps

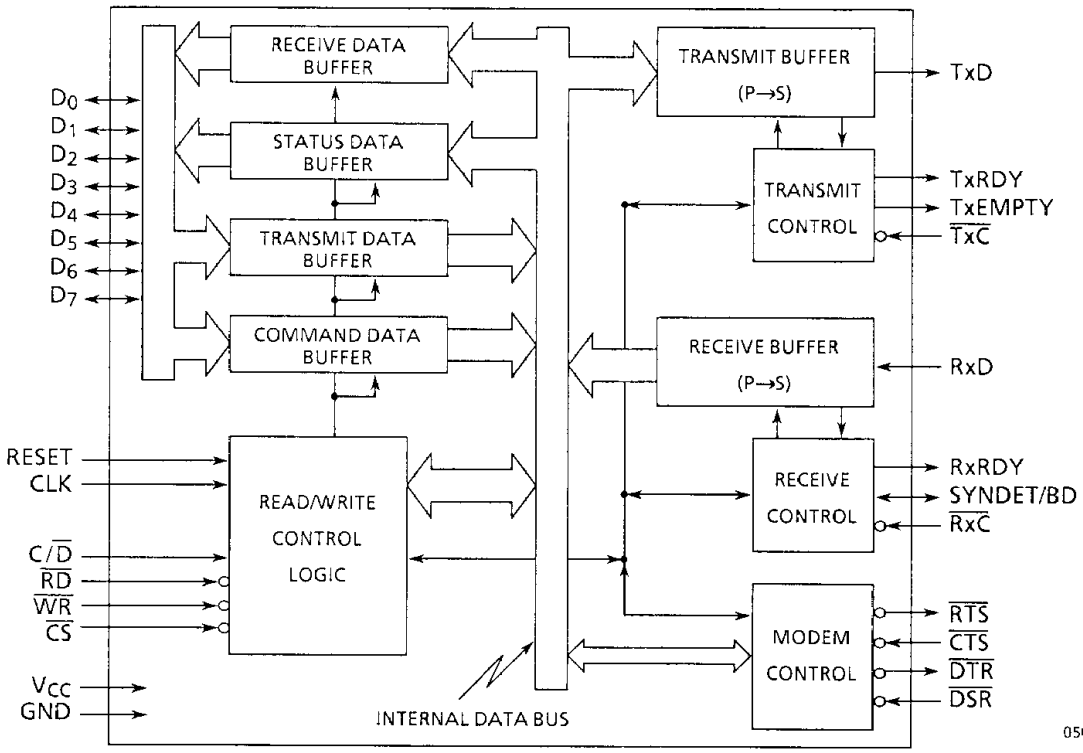
- Full-Duplex, Double-Buffered, Transmitter and Receiver
- Error DetectionParity, Overrun and Framing.
- Single +5V Supply: 5V ±10%

2. PIN CONNECTIONS



050489

3. BLOCK DIAGRAM



050489

4. PIN NAMES AND PIN DESCRIPTIONS

4.1 INTERFACE SIGNALS TO CPU (MAIN SYSTEM)

- D0-D7 (Input/Output)

  This 3-state, bidirectional, 8-bit buffer is used to interface with the system Data Bus. Data is transmitted or received through the buffer upon execution of Input or Output Instructions of the CPU. Control Words, Command Words and Status Information are also transferred through the Data Bus Buffer.

- $\overline{WR}$ (Input)

  A "low" level signal on this input informs the 82C51A that the CPU is Writing Data or Control Words to the 82C51A.

- $\overline{RD}$ (Input)

  A "low" level signal on this input informs the 82C51A that the CPU is Reading Data or Status Information from the 82C51A.

- $\overline{CS}$ (Input)

  A "low" level signal on this input selects the 82C51A. No reading or writing operation will occur unless the device is selected. When $\overline{CS}$ is "high" the Data Bus is in the floating state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.

- C/$\overline{D}$ (Input)

  This input signal, in conjuction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 82C51A that the word on the Data Bus is either a Data Bus Character, Control Word or Status Information. A "high" level signal means Control or Status, a "low" level signal means Data.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	82C51A Receive DATA Buffer → DATA Bus
0	1	0	0	82C51A Transmit DATA Buffer ← DATA Bus
1	0	1	0	82C51A Status DATA Buffer → DATA Bus
X	1	1	0	DATA Bus is in floating state.
X	X	X	1	DATA Bus is in floating state.

- CLK (Input)

  The CLK input is used to generate internal device timing. No external input or output referenced to CLK, but the frequency of CLK must be greater than 30 times the Receiver or Transmitter Data Bit Rates ($\overline{RxC}$ or $\overline{TxC}$) in Synchronous Operation, and greater than 4.5 times the Receiver Data Bit Rates ($\overline{RxC}$ or Trransmiter, $\overline{TxC}$) in Asynchronous operation.

- RESET (Input)

A "high" level signal on this input forces the 82C51A into an "Idle" mode. The device will remain "Idle" until a new set of Control Words is written into the 82C51A to program its functional definition. Minimum RESET pulse width is 6 tcy.

4.2 MODEM CONTROL SIGNALS

- $\overline{DSR}$ (Input)

The $\overline{DSR}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read Operation. The $\overline{DSR}$ input is normally used to test MODEM conditions such as Data Set Ready signal.

- $\overline{DTR}$ (Output)

The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction Words. The $\overline{DTR}$ output signal is normally used for MODEM control such as Data Terminal Ready or Rate Select signal.

- $\overline{RTS}$ (Output)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by pogramming the appropriate bit in the Command Instruction Word. The $\overline{RTS}$ output signal is normally used for MODEM control such as Request to Send signal.

- $\overline{CTS}$ (Input)

A "low" level signal on this input enables the 82C51A to transmit serial data, if the Tx Enable Bit in the Command Byte is set to a "one" (TxEN = 1). If either a Tx Enable off (TxEN = 0) or $\overline{CTS}$ off (CTS = 1) condition occurs while the Tx is in operaion, the Tx will transmit all the data in the USART, written prior to Tx Disable Command before shutting down.

4.3 TRANSMIT CONTROL SIGNALS

- $\overline{TxC}$ (Input)

The transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous Transmission Mode, the Transfer Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous Transmission Mode the transfer rate is a fraction of the actual $\overline{TxC}$ ferquency. A portion of the Mode Instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

If Transfer Rate equals 110 bps,

$\overline{TxC}$ = 110 Hz (1x)

$\overline{TxC}$ = 1.76 kHz (16x)

$\overline{TxC}$ = 7.04 Hz (64x)

The falling edge of $\overline{TxC}$ shifts the serial data out of the 82C51A.

- TxD (Output)

This line is used to transmit serial data. Serial output data on TxD is changed from parallel data to serial data in accordance with the TxD line will be held in the marking state ('1' level) immediately on one of the followings.

- Master Reset
- Tx Disable (TxEN = 0)
- CTS signal is high ($\overline{CTS}$ = 1)
- TxEMPTY signal is high (TxEMPTY = 1)

- TxRDY (Output)

This output informs the CPU that the transmitter is ready to accept a Data Character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disable (TxEN = 0), or, for polled Operation, the CPU can check TxRDY using a Status Read Operation, TxRDY is automatically reset by the trailing edge of $\overline{WR}$ when a Data Character is loaded from the CPU. The TxRDY pin output status (TxRDY (pin)) is different from the TxRDY status bit status register (TxRDY (status bit)) as follows.

TxRDY (status bit) = (Transmit Data Buffer Empty)

TxRDY (pin) = (Transmit Data Buffer Empty) AND ($\overline{CTS}$ = 0) AND (TxEN = 1)

- TxEMPTY (Output)

The TxEMPTY output will go "high" when the 82C51A has no characters to send. It resets upon receiving a character from the CPU if the transmitter is enabled.

In Synchronous Mode, a "high" level signal on this output indicates that a Character has not been loaded and the SYNC Character or Characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go "low" when the SYNC characters are being shifted out.

4.4 RECEIVE CONTROL SIGNALS

- $\overline{RxC}$ (Input)

  The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Transfer Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Transfer Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the Mode Instruction selects this factor; 1, 1/16 or 1/64 the $\overline{RxC}$.

  For Example:

  If Transfere Rate equals 2400 bps,

  $\overline{RxC}$ = 2.4 kHz (1x)

  $\overline{RxC}$ = 38.4 kHz (16x)

  $\overline{RxC}$ = 153.6 kHz (64x)

  Data is sampled into the 82C51A on the rising edge of $\overline{RxC}$.

- RxD (Input)

  This line is used to receive the serial data. Serial input data on this line is changed to parallel data in accordance with the format specified by the Control Words, and then transfered to the Receive Data Buffer.

- RxRDY (Output)

  This output indicates that the 82C51A contains a Data Character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU, or, for Polled Operation, the CPU can check the condition of RxRDY using Status Read Operation.

  Rx Enable off both masks and holds RxRDY in the Reset Condition.

- SYNDET/BD (Input/Output)

  This pin is used for SYNDET in Synchronous Mode and may used as either input or output, programmable through the Control Word. It is reset to output mode "low" upon RESET. When used as an Output (Internal Sync Mode), the SYNDET pin will go "high" to indicate that the 82C51A has located the SYNC Character in the Receive Mode. If the 82C51A is programmed to use Double Sync Characters then SYDET will go "high" in the middle of the last bit of the second SYNC Character. SYNDET is automatically reset upon a Status Read Operation. When used as an Input (External Sync Mode), a positive going signal will cause the 82C51A to start assembling Data Characters on the rising edge of the next $\overline{RxC}$.

In Asynchronous Mode this pin is used BD.

This output will go "high" whenever the receiver remains "low" through two consecutive Stop Bit Sequences (including the Start Bits, Data Bits, and parity bits). Break Detect may also be read as a Status Bit.

It is reset only upon a Master Chip Reset or Rx Data returning to a "one" state.

4.5 POWER SUPPLY

- VCC (Power)

  +5 Volt supply

- GND (Power)

  0 Volt supply

5. ELECTRICAL CHARACTERISTICS

5.1 MAXIMUM RATINGS

Symbol	Item	Rating
V_{CC}	Power Supply Voltage (with respect to GND)	− 0.5V to 7.0V
V_{IN}	Input Voltage (with respect to GND)	− 0.5V to V_{CC} + 0.5
V_{OUT}	Output Voltage (with respect to GND)	− 0.5V to V_{CC} + 0.5
P_D	Power Dissipation	250mW
T_{SOLDER}	Soldering Temperature (10 sec)	260°C
$T_{STG.}$	Storage Temperature	− 65°C to 150°C
$T_{OPR.}$	Operating Temperature	− 40°C to 85°C

050489

5.2 D.C CHARACTERS

Topr = − 40°C to + 85°C, VCC = + 5V ± 10%, GND = 0V, Unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		− 0.5	−	0.8	V
V_{IH}	Input High Voltage		2.2	−	VCC + 0.5	V
V_{OL}	Output Low Voltage	IOL = 2.2mA	−	−	0.45	V
V_{OH1}	Output High Voltage	IOH = − 400μA	2.4	−	−	V
V_{OH2}	Output High Voltage	IOH = − 100μA	Vcc − 0.8	−	−	V
IOFL	Output Leak Current	0.45V ≦ VOUT ≦ VCC	−	−	± 10	μA
IIL	Input Leak Current	0.45V ≦ VOUT ≦ VCC	−	−	± 10	μA
ICC1	Power Supply Current (AP-2/AM-2, 5MHz)	tcyc = 200ns Vin = 4.8V/0.2V	−	1.2	5.0	mA
	Power Supply Current (AP-8/AM-8, 8MHz)	tcyc = 125ns Vin = 4.8V/0.2V	−	2.0	10.0	mA
	Power Supply Current (AP-10/AM-10, 10MHz)	tcyc = 100ns Vin = 4.8V/0.2V	−	2.5	15	mA
ICC2	Power Supply Current (Standby Mode)	STOP All Clocks VCC = 5V, $\overline{CS}$ = 1 Vin = 4.8V/0.2V	−	0.5	10.0	μA

050489

5.3 AC CHARACTERISTICS

Topr = −40°C to 85°C, VCC = 5V ± 10%, GND = 0V, Unless otherwise noted.

5.3.1 Bus Read Cycle Timing Note 1)

Symbol	Parameter	Test Conditions	AP-2 / AM-2		AP-10/AM-10		Units
			Min.	Max.	Min.	Max.	
t_{AR}	$\overline{CS}$, C/$\overline{D}$ Set-up Time for $\overline{RD}$		0	–	0	–	nS
t_{RA}	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{RD}$		0	–	0	–	nS
t_{RR}	$\overline{RD}$ Pulse Width		150	–	120	–	nS
t_{RD}	Data Delay Time for $\overline{RD}$ Note 2)	CL = 150pF Note 3)	–	140	–	100	nS
t_{DF}	Data Hold Time for $\overline{RD}$		10	80	10	50	nS

230589

5.3.2 Bus Write Cycle Timing (Note 1)

Symbol	Parameter	Test Conditions	AP-2 / AM-2		AP-10/AM-10		Units
			Min.	Max.	Min.	Max.	
t_{AW}	$\overline{CS}$, C/$\overline{D}$ Set-up Time for $\overline{WR}$		0	–	0	–	nS
t_{WA}	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{WR}$		0	–	0	–	nS
t_{WW}	$\overline{RD}$ Pulse Width		150	–	120	–	nS
t_{DW}	Data Set-up Time for $\overline{WR}$		100	–	70	–	nS
t_{WD}	Data Hold Time for $\overline{WR}$		0	–	0	–	nS
t_{RV}	Recovery Time Between Write	Note 4)	6	–	6	–	tcyc

230589

5.3.3 Other Timings

Symbol	Parameter	Test Conditions	AP-2 / AM-2		AP-10 / AM-10		Units
			Min.	Max.	Min.	Max.	
tcyc	Clock Period Note 5), 6)		200	–	100	–	nS
tH	Clock High Level Wdith		80	–	40	–	nS
tL	Clock Low Level Wdith		50	–	30	–	nS
tR, tF	Clock Rise, Fall Time		–	20	–	10	nS
tDTx	TxD Delay Time from Falling Edge of TxC		–	1	–	0.5	us
fTx	Transmitter Input Clock Frequency	1xBaud Rate	DC	104	DC	300	kHz
		16xBaud Rate	DC	528	DC	2000	
		64xBaud Rate	DC	832	DC	2000	
tTPH	Transmitter Input Clock Low Level Width	1xBaud Rate	12	–	12	–	tcyc
		16x, 64x, Baud Rate	1	–	1	–	
tTPL	Transmitter Input Clock High Level Width	1xBaud Rate	15	–	15	–	tcyc
		16x, 64x, Baud Rate	3	–	3	–	
fRx	Receiver Input Clock Frequency	1xBaud Rate	DC	104	DC	300	kHz
		16xBaud Rate	DC	528	DC	2000	
		64xBaud Rate	DC	832	DC	2000	
tRPH	Receiver Input Clock High Level Width	1xBaud Rate	12	–	12	–	tcyc
		16x, 64x, Baud Rate	1	–	1	–	
tRPH	Receiver Input Clock Low Level Width	1xBaud Rate	15	–	15	–	tcyc
		16x, 64x, Baud Rate	3	–	3	–	
tTxRDY	TxRDY Pin Delay Time from Center of Last Bit		–	14	–	14	tcyc
tTxRDY CLEAR	TxRDY Clear Delay Time from Leading Edge of $\overline{WR}$		–	400	–	150	ns
tRxRDY	TxRDY Pin Delay Time from Center of Last Bit		–	26	–	26	tcyc
tRxRDY CLEAR	TxRDY Clear Delay Time from Leading Edge of $\overline{WR}$		–	400	–	150	ns
tIS	Internal SYNDET Delay Time from Rising Edge of RxC		–	26	–	26	tcyc
tES	External SYNDET Set-up Time for Falling Edge of $\overline{RxC}$		–	18	–	18	tcyc
tTx EMPTY	TxEMPTY Delay Time from Center of Last Bit		–	20	–	20	tcyc
tWC	Control Delay Time from Rising Edge of $\overline{WR}$ (TxEN, $\overline{DTR}$ $\overline{RTS}$)		–	8	–	8	tcyc
tCR	$\overline{DSR}$, $\overline{CTS}$ Set-up Time for $\overline{RD}$		20	–	20	–	tcyc

230589

Notes:

1) AC Test Condition: Output measuring points VOH = 2.2V, VOL = 0.8V
   Input supply level VIH = 2.4V, VIL = 0.45V

2) Assumes that Address is valid before the falling edge $\overline{RD}$.

3) CL means load capacitance.

4) This recovery time is defind only for Mode Intialization.
   Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 tcyc and for Synchronous Mode is 16 tcyc.

5) The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitations with respect to CLK:
   For 1x Transfer Rate, fTx or fRx < 1 (30 tcyc)
   For 16x and 64x Transfer Rate, fTx or fRx $\leqq$ 1 (4.5 tcyc)

6) Minimum Reset Pulse Width is 6 tcyc. System Clock must running during Reset.

7) Status up data can have a maximum delay of 28 clock periods from the event affecting the status.

6. TIMING WAVEFORMS

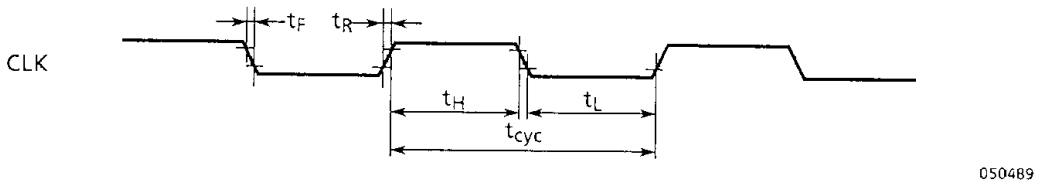


Figure 6.1 System Clock

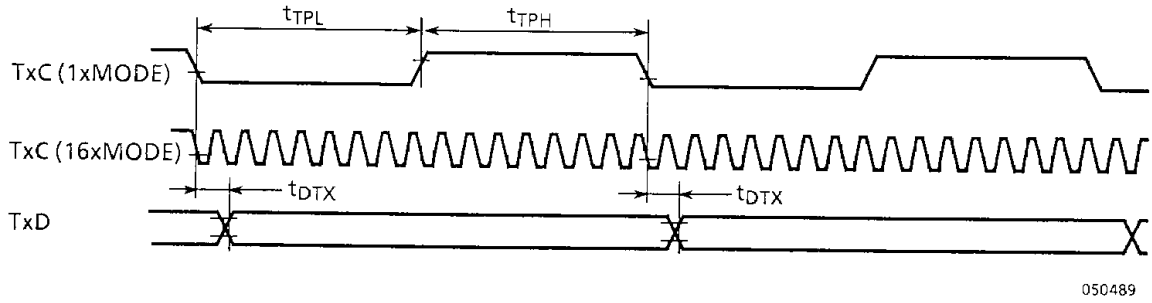


Figure 6.2 Transmitter Clock and Data

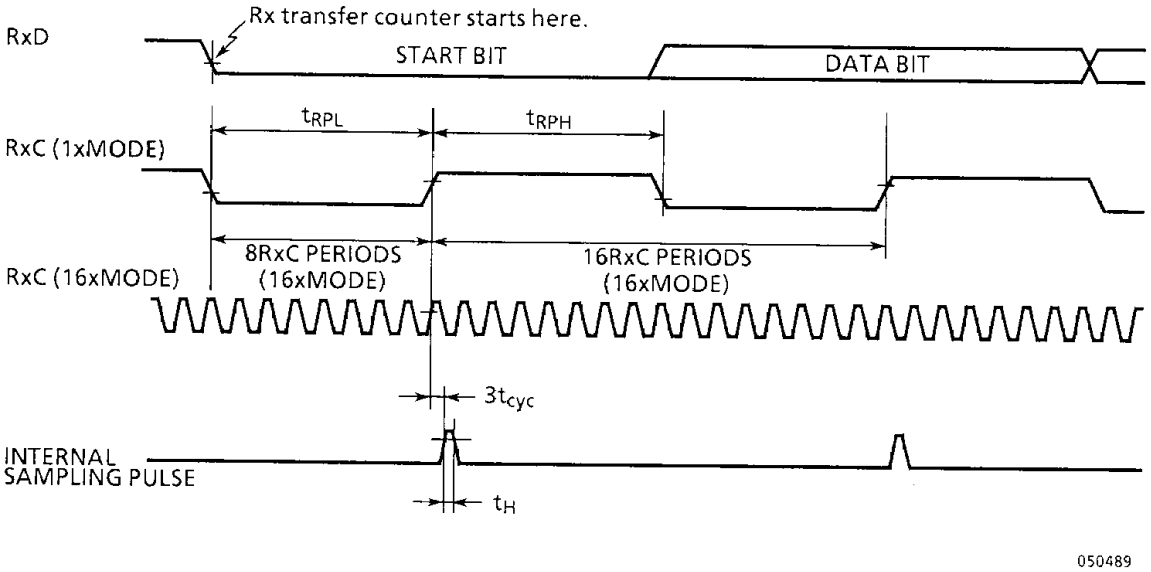


Figure 6.3 Receiver Clock and Data

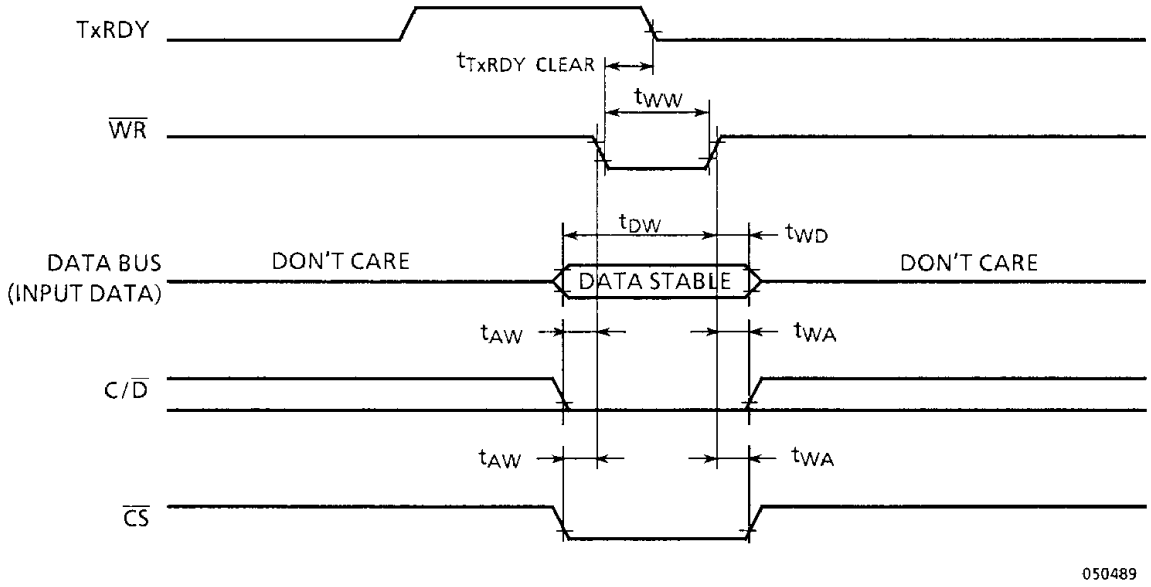


Figure 6.4 Write Data Cycle (MPU → 82C51A)

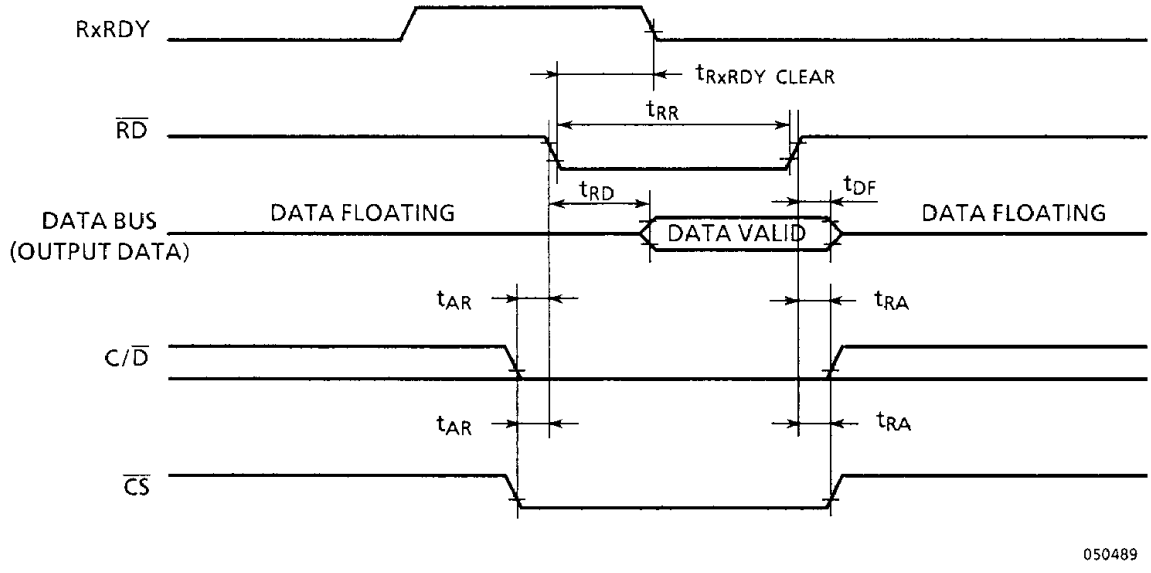


Figure 6.5 Read Data Cycle (82C51A → MPU)

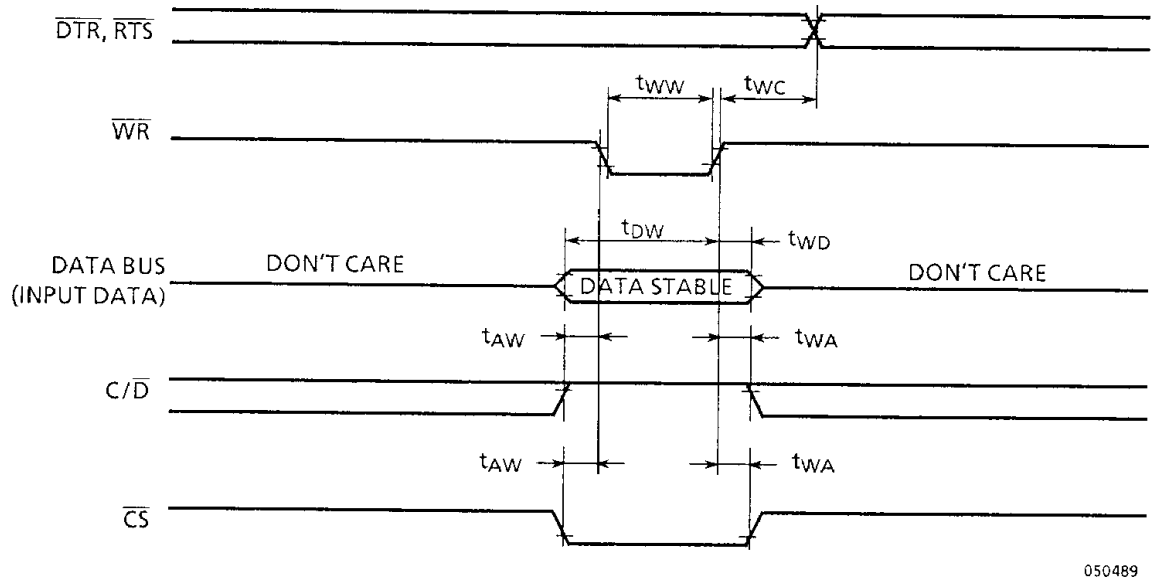


Figure 6.6 Write Control or Output Port Cycle (MPU → 82C51A)

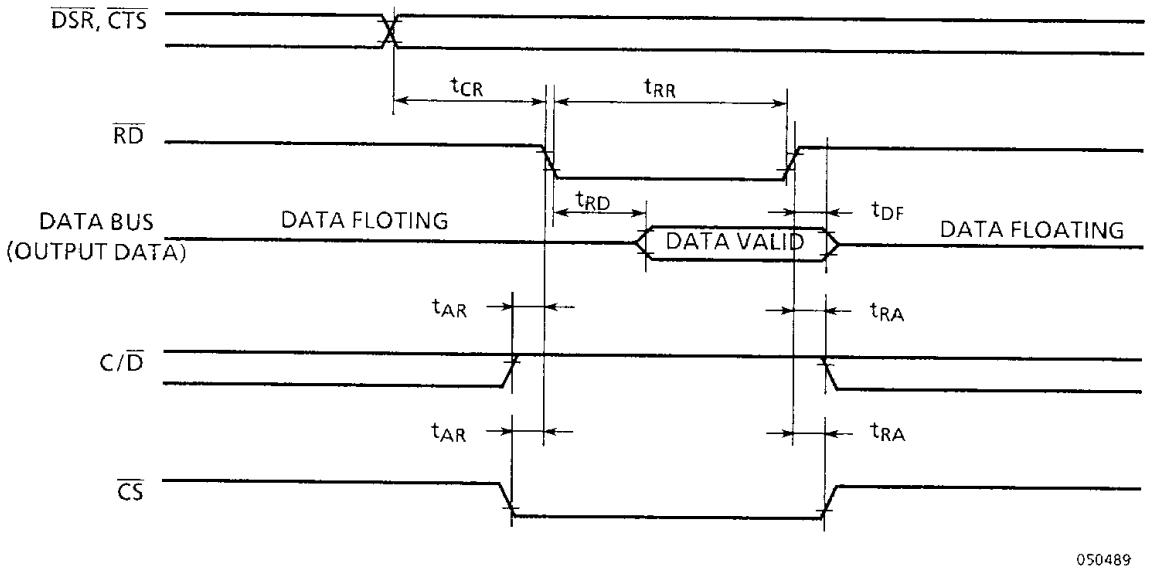


Figure 6.7 Read Control or Input Port Cycle (82C51A → MPU)

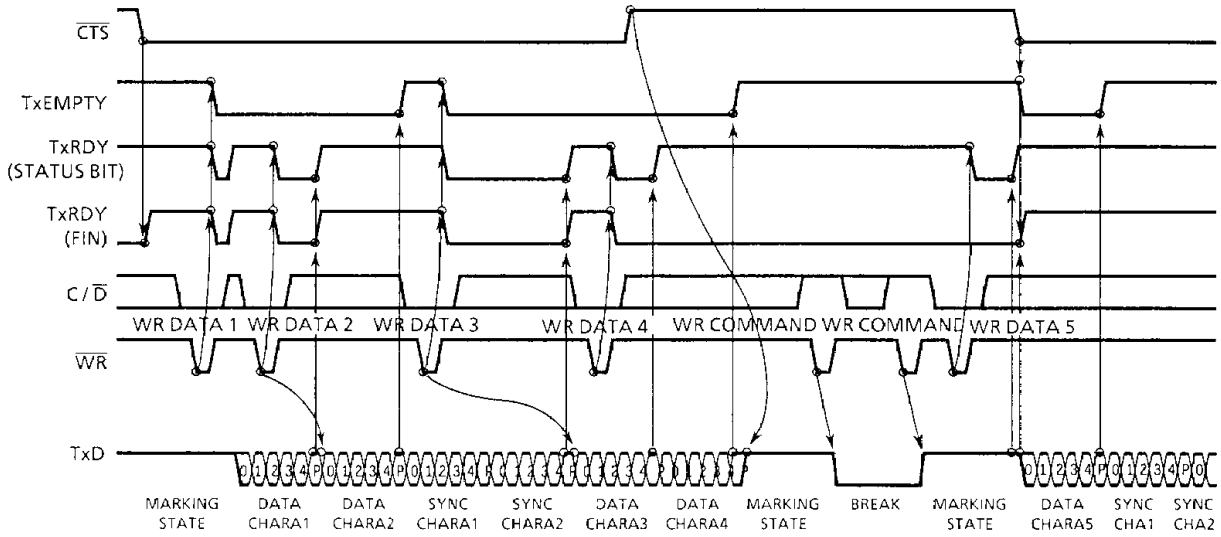


Figure 6.8 Transmitter Control and Flag Timing (SYNC Mode)

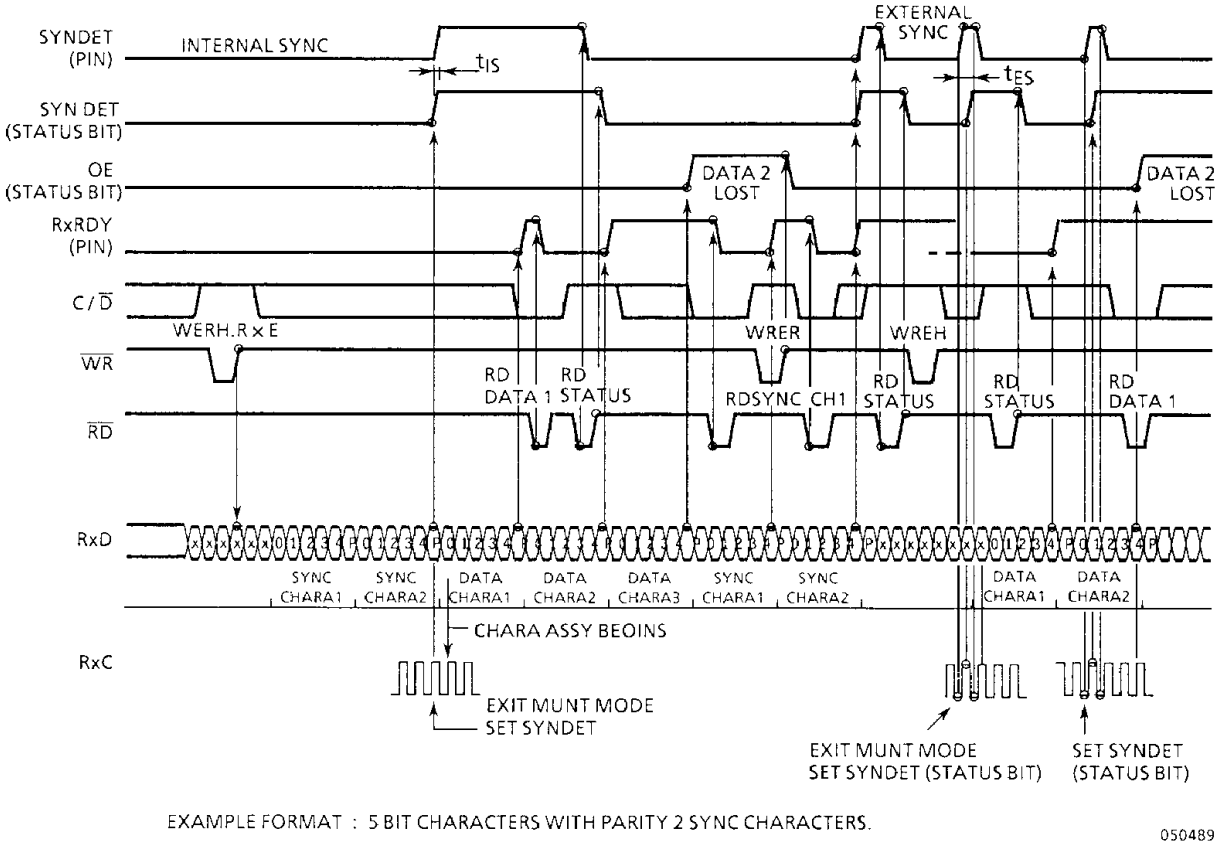
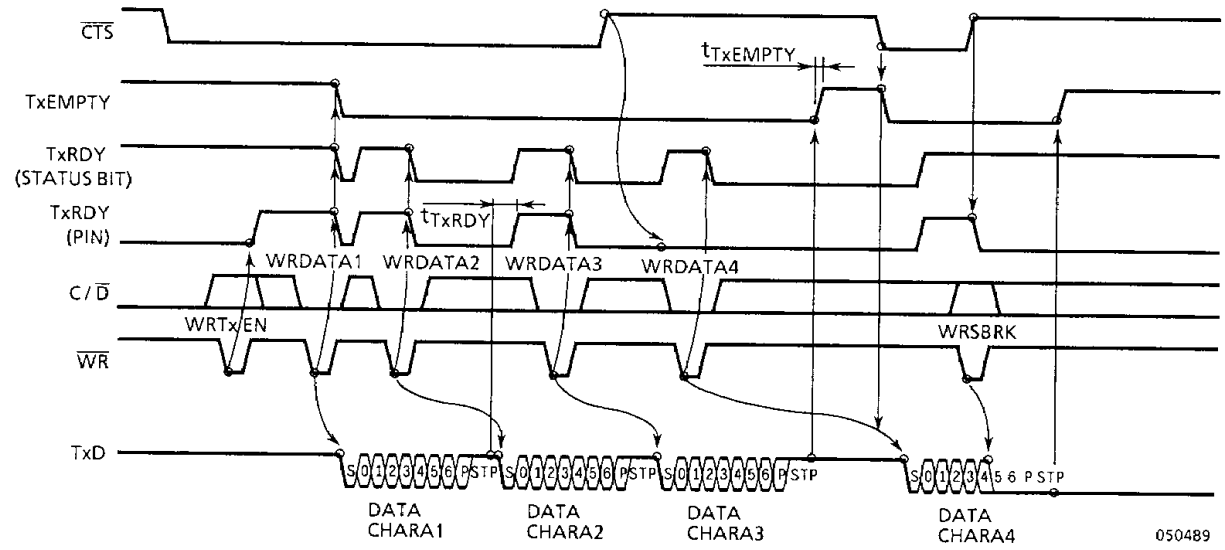


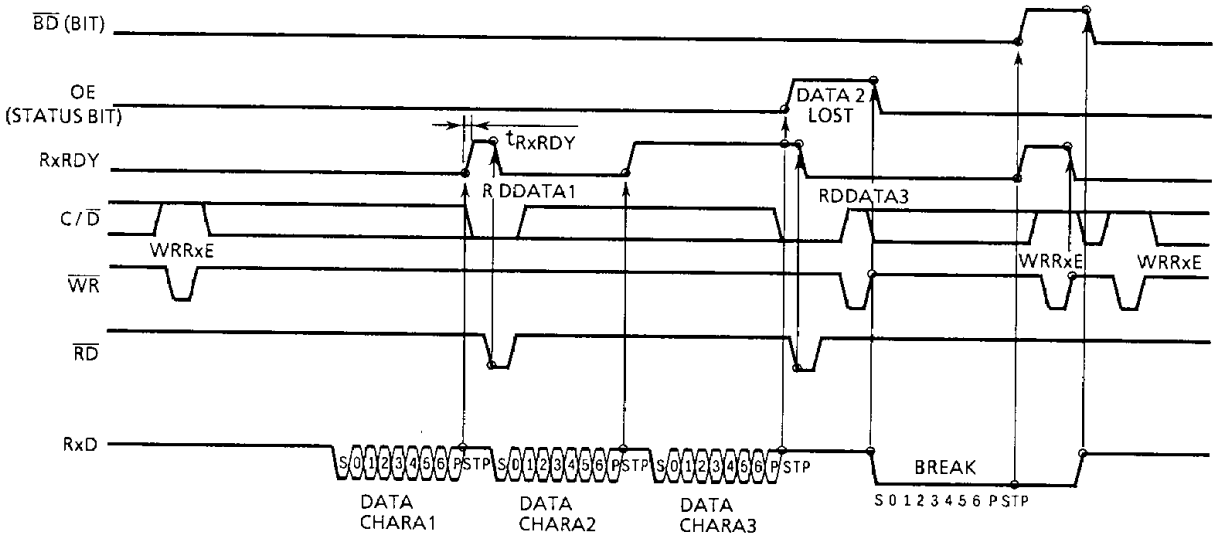
Figure 6.9 Receiver Control and Flag Timimg (SYNC Mode)



EXAMPLE FORMAT : 7 BIT CHARACTER & 2 STOP BITS.

NOTE: { TxRDY (PIN) = (Transmit Data Buffer is empty) . (TxEN = 1) . ($\overline{CTS}$ = 0)
TxRDY (STATUS BIT) = (Transmit Data Buffer is empty)

Figure 6.10 Transmitter Control and Flag Timimg (ASYNC Mode)



EXAMPLE FORMAT : 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

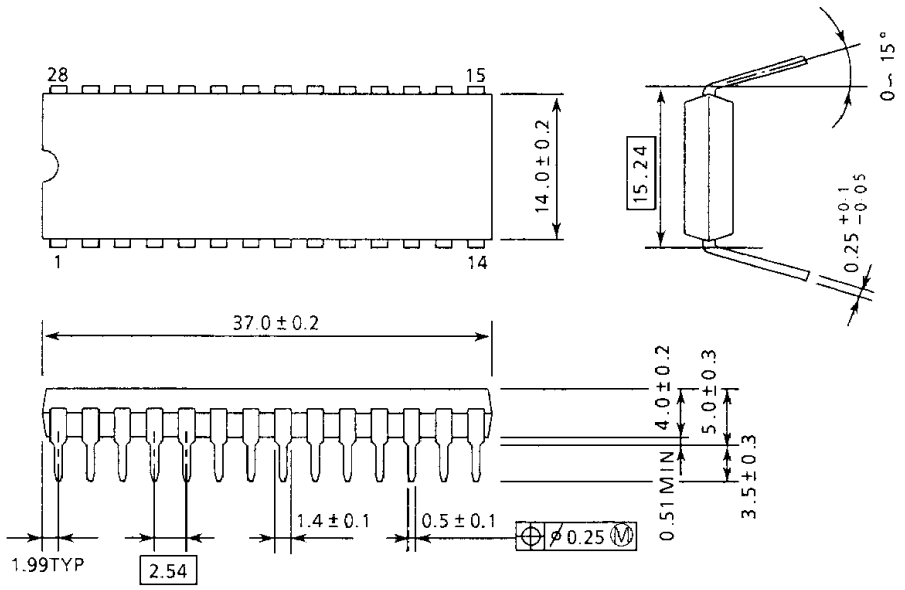
Figure 6.11 Receiver Control and Flag Timing (ASYNC Mode)

7. OUTLINE DRAWING

7.1 DIP

DIP28-P-600

Unit : mm



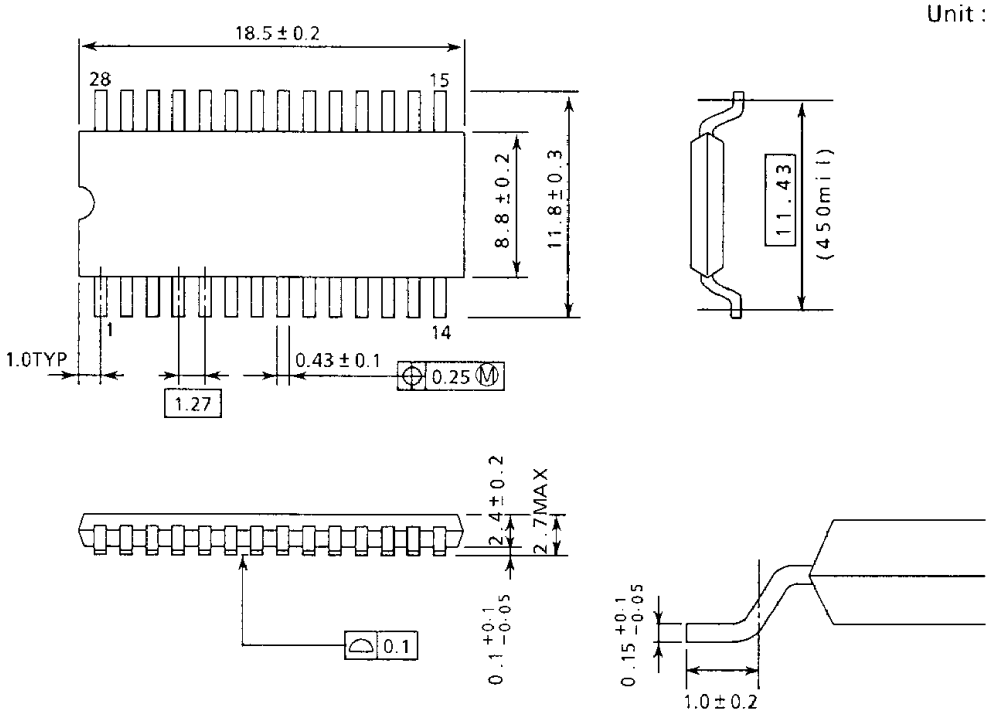
270289

Note : Lead pitch is 2.54mm and to lerance is ±0.25mm against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

7.2 SOP

SOP28-P-450

Unit : mm



270289

Note : Package Width and Length do not include Mold Protrusions.
Allowable Mold Protrusion is 0.15mm.

PROGRAMMABLE COMMUNICATION INTERFACE

TMP8251AP

1. GENERAL DESCRIPTION

The TMP8251AP is the industry standard Universal Synchronous/Asynchoronous Receiver/Transmitter (USART) that is fabricated using N-channel silicon gate MOS technology.

The TMP8251A is mainly used for 8-bit microcomputer extension systems, which require serial data communications.

The TMP8251AP is packaged in the 28pin standard Dual Inline package.

FEATURES

- Synchoronous:

  5-8 Bit Characters
  Internal or External Character Synchronization
  Single or Double Character Synchronization (Internal)
  Automatic Sync Insertion

- Asynchronous:

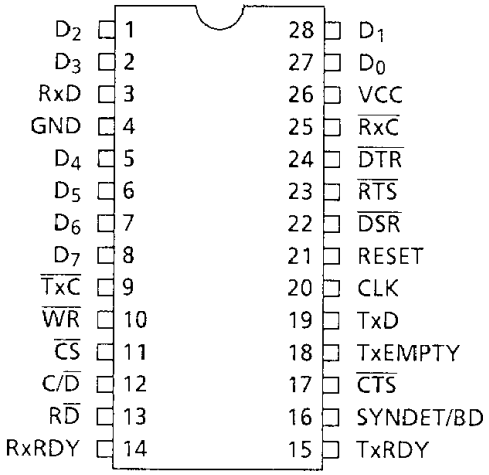
  5-8 Bit Characters
  Clock Rate - 1, 16 or 64 Times Transfer Rate
  Break Character Generation
  1, 1.5, or 2 Stop Bits
  False Start Bit Detection
  Automatic Break Detect and Handling

- Transfer Rate DC to 64K bps (Synchronous)

  DC to 19.6K bps (Asynchronous)

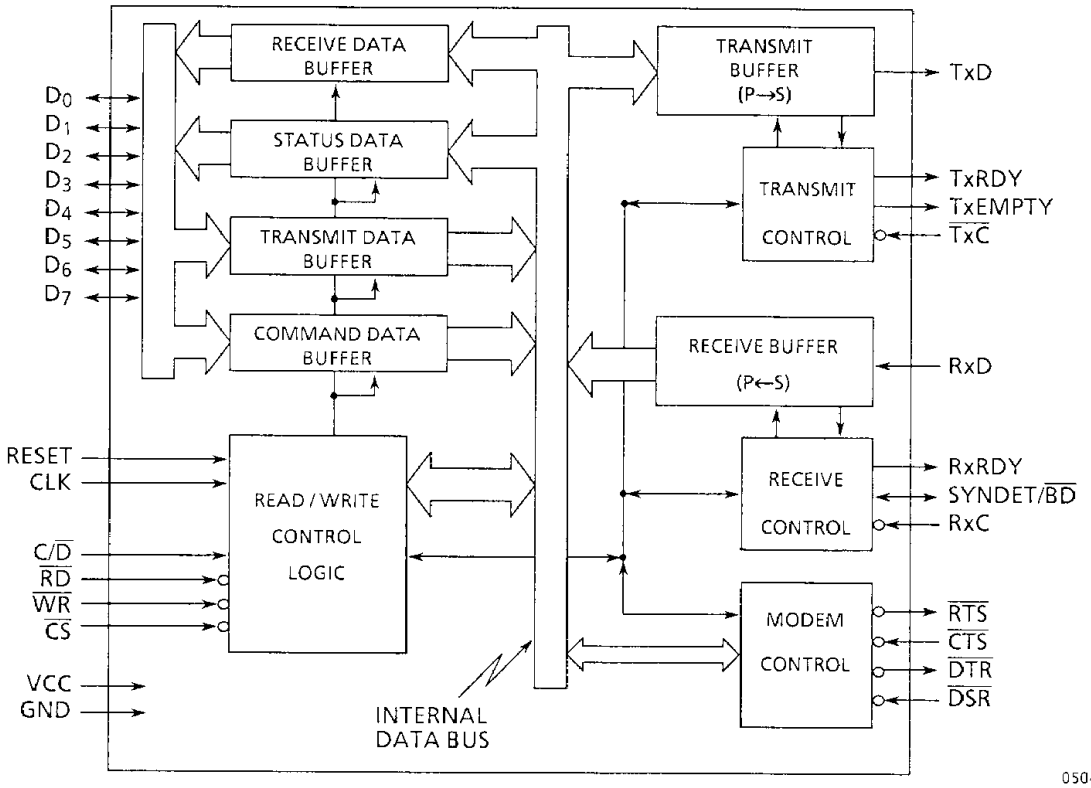
- Full-Duplex, Double-Buffered, Transmitter and Receiver
- Error DetectionParity, Overrun and Framing
- Single +5V Supply
- Compatible with Intel's 8251A/S2657

2. PIN CONNECTIONS (TOP VIEW)



050489

3. BLOCK DIAGRAM



050489

4. PIN NAMES AND PIN DESCRIPTIONS

4.1 INTERFACE SIGNALS TO MPU (MAIN SYSTEM)

- $D_0 \sim D_7$ (Input/Output)

  This 3-state bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received through the buffer upon execution of Input or Output Instructions of the MPU. Control Words, Command Words and Status Information are also transffered through the Data Bus Buffer.

- $\overline{WR}$ (Input)

  A "low" level signal on this input informs the 8251A that the MPU is Writing Data or Control Words to the 8251A.

- $\overline{RD}$ (Input)

  A "low" level signal on this input informs the 8251A that the MPU is Reading Data or Status Information from the 8251A.

- $\overline{CS}$ (Input)

  A "low" level signal on this input selects the 8251A. No reading or writing operation will occur unless the device is selected. When $\overline{CS}$ is "high" the Data Bus is in the floating state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chips.

- $C/\overline{D}$ (Input)

  This input signal, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a Data Character, Control Word or Status Information. A "high" level signal means Control or Status, a "low" level signal means Data.

$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A Recieve DATA Buffer → Data Bus
0	1	0	0	8251A Transmit DATA Buffer ← Data Bus
1	0	1	0	8251A Status DATA Buffer → Data Bus
1	1	0	0	8251A Command DATA Buffer ← Data Bus
×	1	1	0	DATA Bus is in floating state.
×	×	×	1	

- CLK (Input)

  The CLK input is used to generate internal device timing. No external input or output is referenced to CLK, but the frequency of CLK must be greater than 30 times the Receiver or Transmitter Data Bit Rates ($\overline{RxC}$ or $\overline{TxC}$) in Synchronous Operation, and greater than 4.5 times the Receiver Data Bit Rated ($\overline{RxC}$) in Asynchronous Operation.

- RESET (Input)

  A "high" level signal on this input forces the 8251A into an "Idle" mode. The device will remain at "Idel" untill a new set of Control Words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 tcy.

4.2 MODEM CONTROL SIGNALS

- $\overline{DSR}$ (Input)

  The $\overline{DSR}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the MPU using a Status Read Operation. The $\overline{DSR}$ input is normlaly used to test MODEM conditions such as Data Set Ready signal.

- $\overline{DTR}$ (Output)

  The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instsruction Word. The $\overline{DTR}$ output signal is normally used for MODEM control such as Data Terminal Ready or Rate Select signal.

- $\overline{RTS}$ (Output)

  The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction Word. The $\overline{RTS}$ output signal is normally used for MODEM control such as Request to Send signal.

- $\overline{CTS}$ (Input)

  A "low" level signal on this input enables the 8251A to transmit serial data, if the Tx Enable Bit in the Command Byte is set to a "one" (TxEN = 1). If either a Tx Enable off (TxEN = 0) or CTS off ($\overline{CTS}$ = 1) condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable Command before shutting down.

4.3 TRANSMIT CONTROL SIGNALS

- $\overline{TxC}$ (Input)

  The Transmitter Clock Controls the rate at which the character is to be transmitted. In the Synchronous Transmission Mode, the transfer rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous Transmission Mode, the transfer rate is a fraction of the actual $\overline{TxC}$ frequency. A poriton of the Mode Instruction selects this factor; it can be 1, $^1/_{16}$ or $^1/_{64}$ the $\overline{TxC}$.

  For Example:
  If transfer rate equals 110 bps,
  $\overline{TxC}$ = 110 Hz (1x)
  $\overline{TxC}$ = 1.76 KHz (16x)
  $\overline{TxC}$ = 7.04 KHz (64x)

  The falling edge of TxC shifts the serial data out of the 8251A.

- TxD (Output)

  This line is used to transmit the serial data. Serial output data on TxD is changed from paralled data to serial data in accordancae with the format specified by the Control Words.

  TxD line will be held in the marking state ('1' level) immediately on one of the following.s

  - Master Reset
  - CTS signal is high ($\overline{CTS}$ = 1)
  - Tx Disable (TxEN = 0)
  - TxEMPTY signal is high (TxEMPTY = 1)

- TxRDY (Output)

  This output informs the MPU that the transmitter is ready to accept a Data Character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disable (TxEN = 0), or, for polled Operation, the MPU can check TxRDY using a Status Read Operaiton. TxRDY is automatically reset by the trailing edge of $\overline{WR}$ when a Data Character is loaded from the MPU. The Tx RDY pin output status (Tx RDY (pin)) is different from the TxRDY status bit status (TxRDY (status bit)) as follows.

  TXRDY (status bit) = (Transmit Data Buffer Empty)

  TxRDY (pin) = (Transmit Data Buffer Empty) · (CTS = 0) · (TxEN = 1)

- TxEMPTY (Output)

  The TxEMPTY output will go "high" when the 8251A has no characters to send. It resets upon receiving as character from the MPU if the transmitter is enabled.

In Synchronous Mode, a"high" level signal on this output indicates that a Character has not been loaded and the SYNC Character or Characters are about to be or are being transmitted automatically as "fillers". Tx EMPTY does not go "low" when the SYNC characters are being shifted out.

4.4 RECEIVE CONTROL SIGNLAS

- $\overline{\text{RxC}}$ (Input)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Transfer Rate (1x) is equal to the actual frequency of $\overline{\text{RxC}}$. In Asynchronous Mode, the Transfer Rate is a fraction of the actual $\overline{\text{RxC}}$ frequency. A portion of the Mode Instruciton selects this factor; 1, $^1/_{16}$ or $^1/_{64}$ the $\overline{\text{RxC}}$.

For Example:
if Transfer Rate equals 2400 bps,
$\overline{\text{RxC}}$ = 2.4 KHz (1x)
$\overline{\text{RxC}}$ = 38.4 KHz (16x)
$\overline{\text{RxC}}$ = 153.6 KHz (64x)

Data is sampled into the 8251A on the rising edge of $\overline{\text{RxC}}$.

- RxD (Input)

This line is used to receive the serial data. Serial input data on this line is changed to parallel data in accordance with the format specified by the Control Words, and then transfered to the Receive Data Buffer.

- RxRDY (Output)

This output indicates that the 8251A contains a Data Character that is ready to be input to the MPU. RxRDY can be connected to the interrupt structure of the MPU, or, for Polled Operation, the MPU can check the condition of RxRDY using a Status Ready Operaiton.

Rx Enable off both masks and holds RxRDY in the Reset Condition.

- SYNDET/BD (Input/Output)

  This pin is used for SYNDET in Synchronous Mode and may be used as eigher input or ourput, programmable through the Contorl Word. It is reset to output mode "low" upon RESET. When used as an Output (Internal Sync Mode), the SYNDET pin will go "high" to indicate that the 8251A is programmed to use SYNC Character in the Receive Mode. If the 8251A is programmed to use Double Sync Characters then SYNDET will go "high" in the middle of the last bit of the second SYNC Character. SYNDET is automatically reset upon a Status Read Operation. When used as an Input (External Sync Mode), a positive going signal will cause the 8251A to start assembling Data Characters on the rising edge of the next $\overline{RxC}$.

  In Asynchronous Mode this pin is used for BD. This output will go "high" whenever the receiver remains "low" through two consecutive Stop Bit Sequences (including the Start Bits, Data Bits, and Parity Bits). Break Detect may also be read as a Status Bit. It is reset only upon a Master Chip Reset or Rx Data returning to a "one" state. But, if the Rx data returns to a "one" State during the last bit of the next character after the Break, Break detect does not always reset.

4.5 POWER SUPPLY

- V_{CC} (Power)
  +5 Volt supply
- GND (Power)
  0 Volt supply

5. ELECTRICAL CHARACTERISTICS

5.1 MAXIMUM RATINGS

SYMBOL	ITEM	RATING
V_{CC}	Power Supply Voltage (with respect to GND)	−0.5V to 7.0V
V_{IN}	Input Voltage (with respect to GND)	−0.5V to 7.0V
V_{OUT}	Output Voltage (with respect to GND)	−0.5V to 7.0V
P_D	Power Dissipation (Ta = 70°C)	1W
T_{solder}	Soldering Temperature (10 sec)	260°C
T_{stg}	Storage Temperature	−55°C to 150°C
T_{opr}	Operating Temperature	0°C to 70°C

050489

5.2 D.C. CHARACTERISTICS

T_{opr} = 0°C to 70°C, V_{CC} = 5V ± 5%, GND = 0V, Unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage		−0.5	−	0.8	V
V_{IH}	Input High Voltage		2.2	−	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL} = 2.2mA	−	−	0.45	V
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	−	−	V
I_{OFL}	Output Leak Current	$0.45V \leqq V_{OUT} \leqq V_{CC}$	−	−	± 10	μA
I_{IL}	Input Leak Current	$0.45V \leqq V_{IN} \leqq V_{CC}$	−	−	± 10	μA
I_{CC}	Power Supply Current	All Outputs = "High"	−	−	100	mA

050489

5.3 A.C CHARACTERISTICS

T_{opr} = 0°C to 70°C, V_{CC} = 5V ± 5%, GND = 0V, Unless otherwise noted.

5.3.1 Bus Read Cycle Timing Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AR}	$\overline{CS}$, C/$\overline{D}$ Set-up Time for $\overline{RD}$		50	−	−	ns
t_{RA}	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{RD}$		50	−	−	ns
t_{RR}	$\overline{RD}$ Pulse Width		250	−	−	ns
t_{RD}	Data Delay Time for RD Note 2)	C_L = 150pF Note 3)	−	−	250	ns
t_{DF}	$\overline{CS}$, C/$\overline{D}$ Set-up Time for $\overline{RD}$		10	−	100	ns

050489

5.3.2 Bus Write Cycle Timing Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{AW}	$\overline{CS}$, C/$\overline{D}$ Set-up Time for $\overline{WR}$		50	–	–	ns
t_{WA}	$\overline{CS}$, C/$\overline{D}$ Hold Time for $\overline{WR}$		50	–	–	ns
t_{WW}	$\overline{WR}$ Pulse Width		250	–	–	ns
t_{DW}	Data Set Up Time for $\overline{WR}$		150	–	–	ns
t_{WD}	Data Hold Time for $\overline{WR}$		50	–	–	ns
t_{RV}	Recovery Time between WRITES	Note 4)	6	–	–	t_{cyc}

050489

5.3.3 Other Timing

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT	
t_{cyc}	Clock PeriodNote 5), 6)		320	–	1350	ns	
t_H	Clock HIgh Level Width		140	–	t_{cyc} – 90	ns	
t_L	Clock Low Level Width		90	–	–	ns	
t_R, t_F	Clock Rise and Fall Time		–	–	20	ns	
t_{DTx}	TxD Delay Time from Falling Edge of $\overline{TxC}$		–	–	1	μs	
f_{Tx}	Transmitter Input Clock Frequency	1x, 64x Baud Rate	DC	–	64	kHz	
		16x Baud Rate	DC	–	310		
		64x Baud Rate	DC	–	615		
t_{TPH}	Transmitter Input Clock High Level Width	1x Baud Rate	12	–	–	t_{cyc}	
		16, 64x Baud Rate	1	–	–		
t_{TPL}	Transmitter Input Clock Low Level Width	1x Baud Rate	15	–	–	t_{cyc}	
		64x Baud Rate	3	–	–		
f_{Rx}	Transmitter Input Clock Frequency	1x Baud Rate	DC	–	64	kHz	
		16, 64x Baud Rate	DC	–	310		
		64x Baud Rate	DC	–	615		
t_{RPH}	Transmitter Input Clock High Level Width	1x Baud Rate	12	–	–	t_{cyc}	
		64x Baud Rate	1	–	–		
t_{RPL}	Transmitter Input Clock Low Level Width	1x Baud Rate	15	–	–	t_{cyc}	
		64x Baud Rate	3	–	–		
t_{TxRDY}	TxRDY Pin Delay Time from Center of Last Bit		–	–	8	t_{cyc}	Note 7
$t_{RxRDY\ CLEAR}$	TxRDY Clear Delay Time from Trailing Edge of $\overline{WR}$		–	–	6	t_{cyc}	Note 7
t_{RxRDY}	RxRDY Pin Delay Time from Center of Last Bit		–	–	24	t_{cyc}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY Clear Delay Time from Leading Edge of $\overline{RD}$		–	–	6	t_{cyc}	Note 7
t_{IS}	Internal SYNDET Delaya Time from Rising Edge of $\overline{RxC}$		–	–	24	t_{cyc}	Note 7
t_{ES}	External SYNDET Set-Up Time fore Falling Edge of $\overline{RxC}$		16	–	–	t_{cyc}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay Time from Center of Last Bit		20	–	–	t_{cyc}	Note 7
t_{WC}	Control Delay Time from Rising Edge of $\overline{WR}$ (TxEN, $\overline{DTR}$, $\overline{RTS}$)		8	–	–	t_{cyc}	Note 7
t_{CR}	$\overline{DSR}$, $\overline{CTS}$ Set-Up Time for $\overline{RD}$		20	–	–	t_{cyc}	Note 7

050489

Note :

1) AC Test Conditions : Output measuring Point $V_{OH}=2.0V$, $V_{OL}=0.8V$
   Input supply level $V_{IH}=2.4V$, $V_{IL}=0.45V$
2) Assumes that Address is valid before the falling edge of $\overline{RD}$.
3) C_L means load capacitance.
4) This recovery time is defined only for Mode Intialization.
   Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 tcy and for Synchronous Mode is 16 tcy.
5) The TxC and RxC frequencies have the following limitations with respect to CLK:
   For 1x Transfer Rate, f_{Tx} or $f_{Rx} \leqq 1/(30tcy)$
   For 16x and 64x Transfer Rate, f_{Tx} or $f_{Rx} \leqq 1/(4.5tcy)$
6) Minimum Reset Pulse Width is 6 tcy. System Clock must be running during Reset.
7) Status up data can have a maximum delay of 28 clock periods from the event affecting the status.

6. TIMING WAVEFORMS

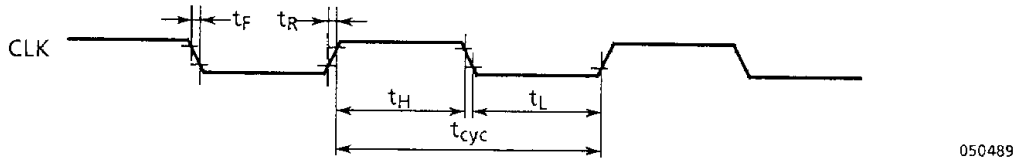


Figure 6.1 System Clock

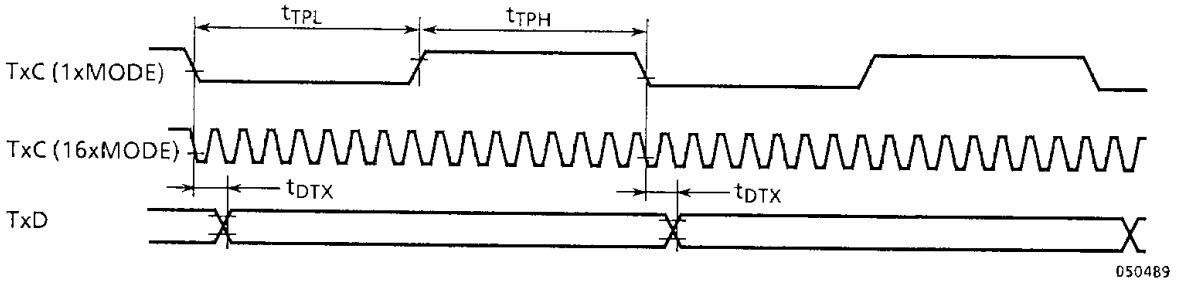


Figure 6.2 Transmitter Clock and Data

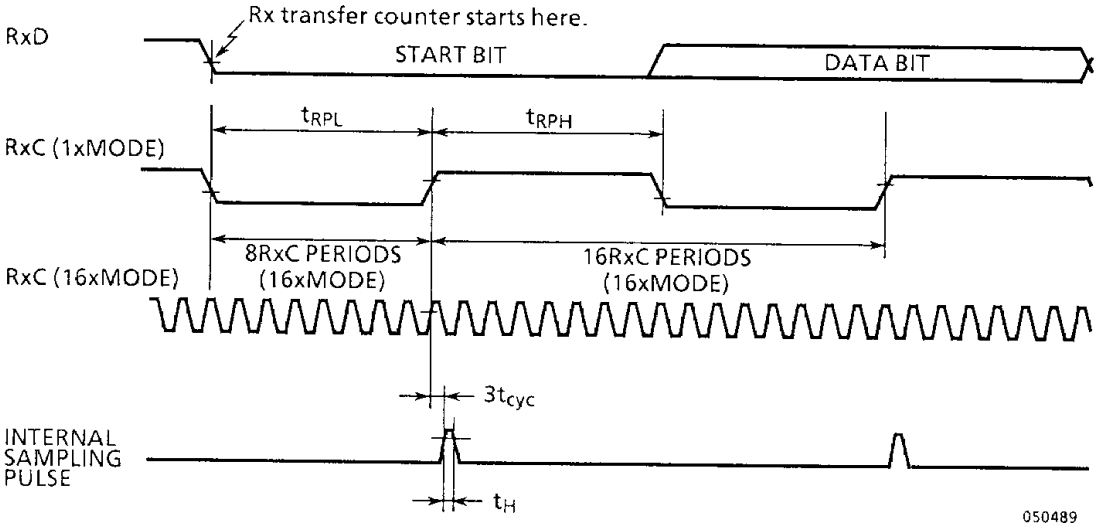


Figure 6.3 Receiver Clock and Data

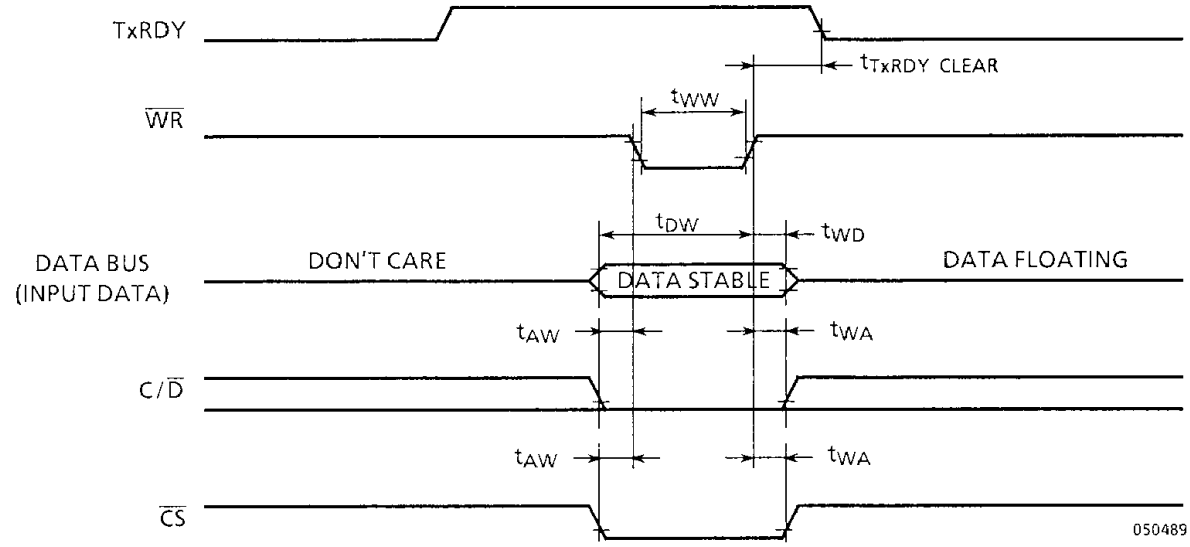


Figure 6.4 Write Data Cycle (MPU→8251A)

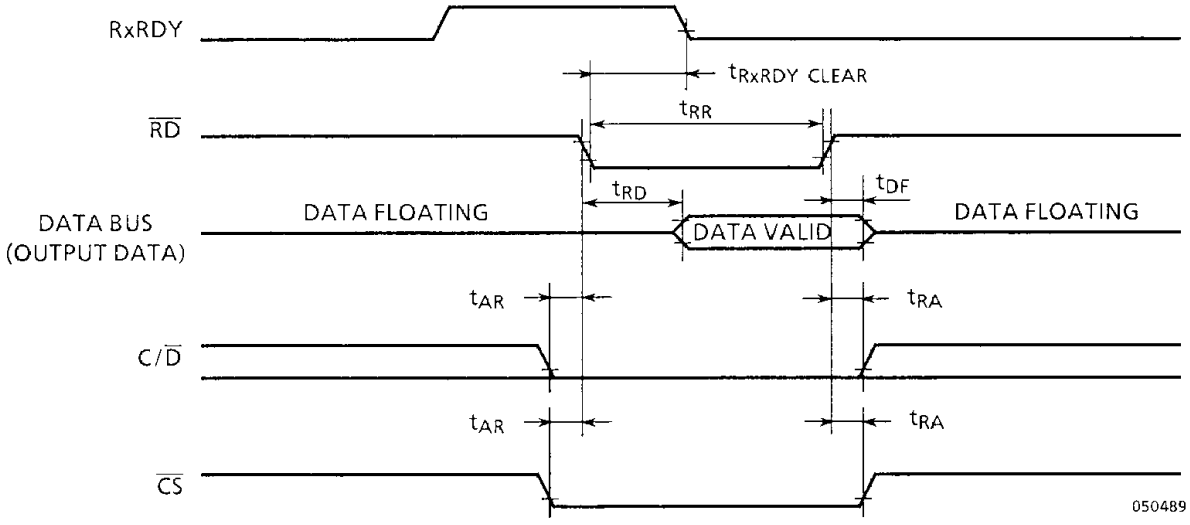


Figure 6.5 Read Data Cycle (8251A→MPU)

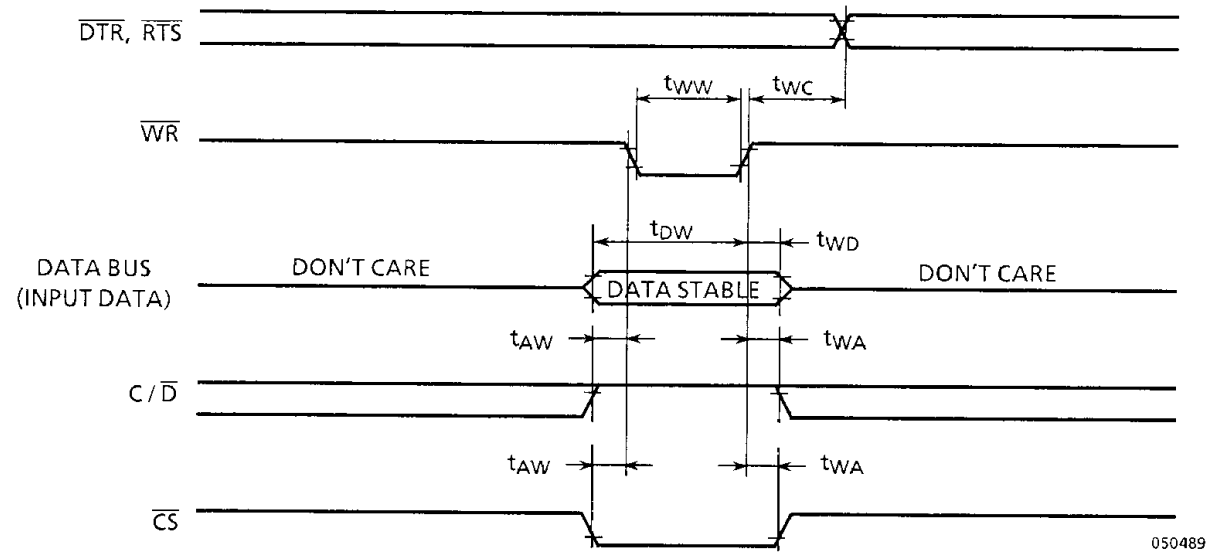


Figure 6.6 Write Contorl or Output Port Cycle (MPU→82251A)

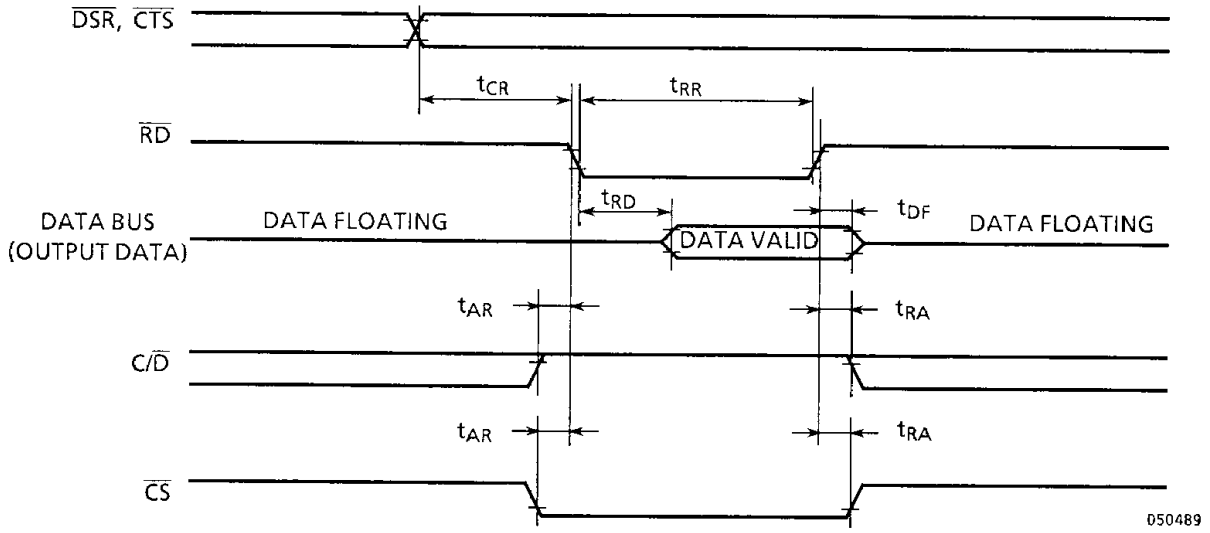
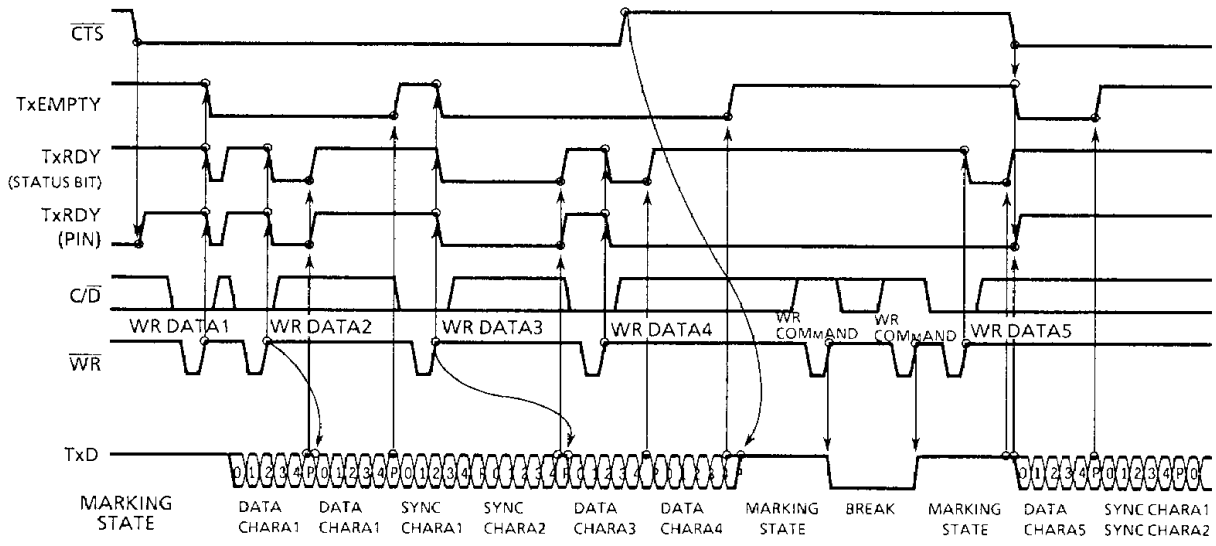


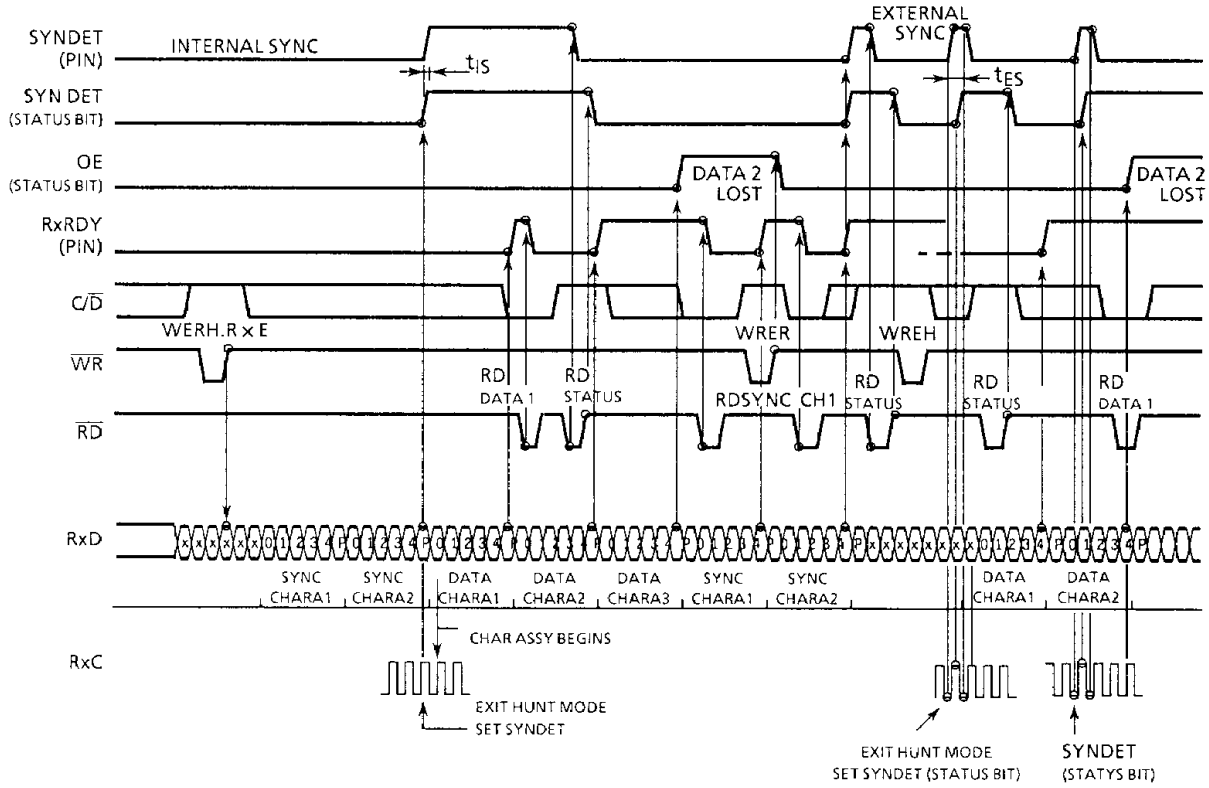
Figure 6.7 Read Control or Input Port Cycle (8251A→MPU)



EXAMPLE FORMAT : 5 BIT CHARACTER WITH PARITY 2 SYNC CHARACTERS.

050489

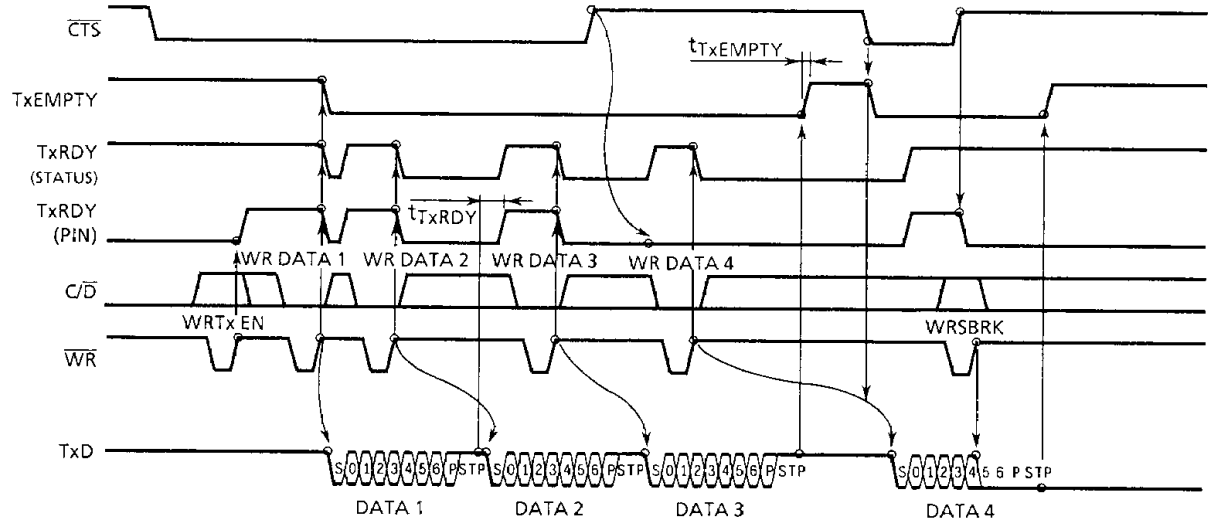
Figure 6.8 Transmitter Control and Flag Timing (SYNC Mode)



EXAMPLE FORMAT : 5 BIT CHARACTER WITH PARITY 2 SYNC CHARACTERS.

050489

Figure 6.9 Receiver Controla nd Flag Timing (SYNC Mode)

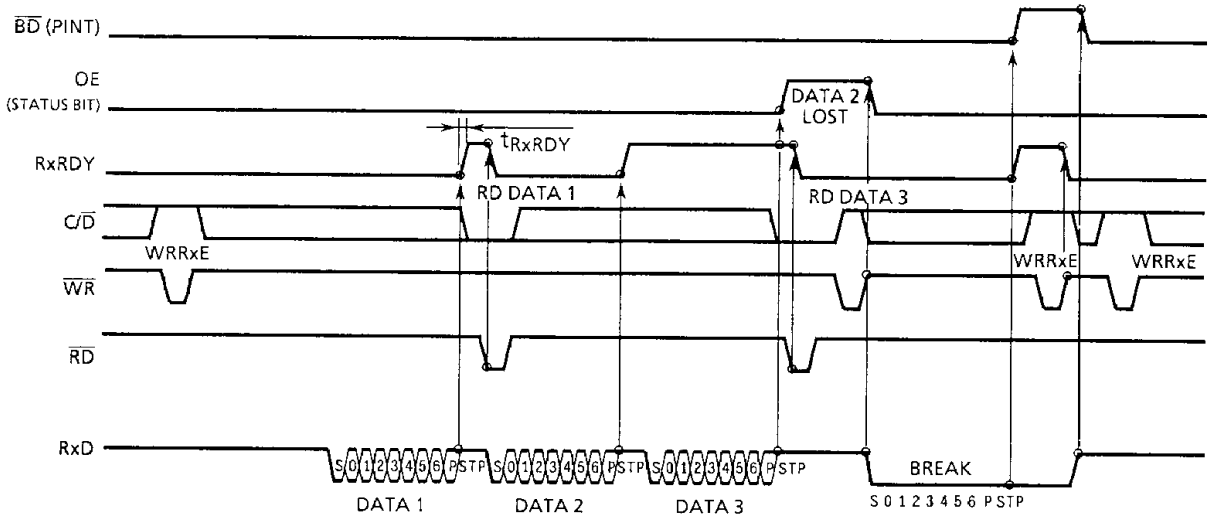


EXAMPLE FORMAT : 7 BIT CHARACTER & 2 STOP BITS.

050489

Note : TxRDY (PIN) – (Transmit Data Buffer is empty) · (TxEN = 1) · (CTS – 0)
TxRDY (STATUS BIT) – (Transmit Data Buffer is empty)

Figure 6.10 Transmitter Control and Flag Timing (SYNC Mode)



EXAMPLE FORMAT : 7 BIT CHARACTER & 2 STOP BITS.

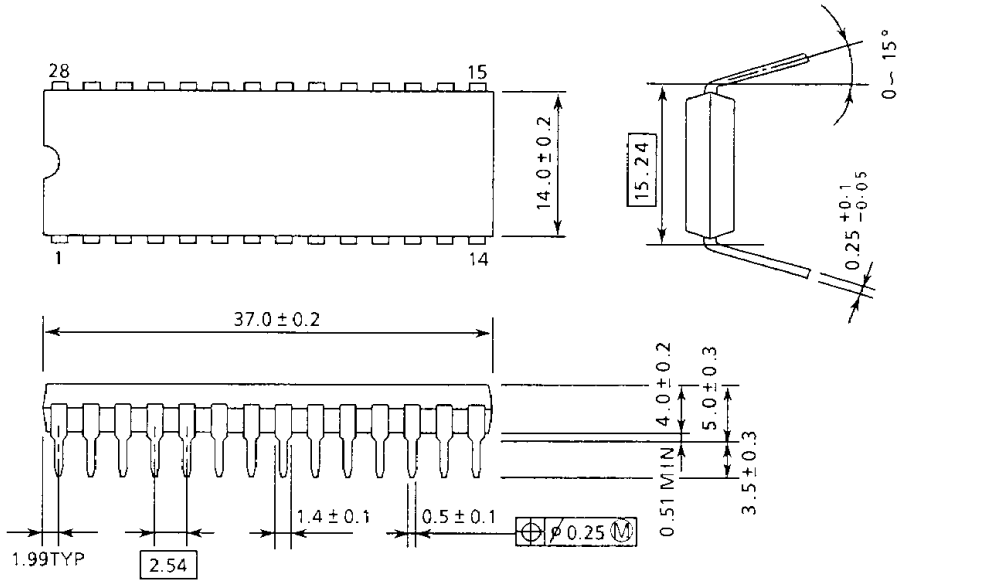
050489

Figure 6.11 Receiver Control and Flag Timing (ASYNC Mode)

7. OUTLINE DRAWING (Dual Inline Package)

DIP28-P-600

Unit : mm



270289

Note : Lead pitch is 2.54m and to lerance is ±25mm against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.