

General Description

The AO4627 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This complementary N and P channel MOSFET configuration is ideal for low Input Voltage inverter applications.

Product Summary

N-Channel

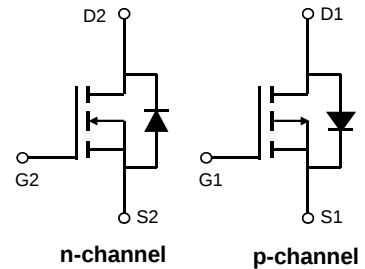
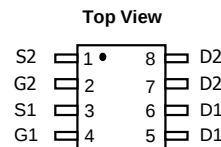
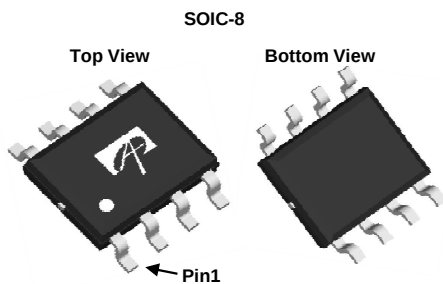
$V_{DS} = 30V$
 $I_D = 4.5A$ ($V_{GS} = 10V$)
 $R_{DS(ON)} < 50m\Omega$ ($V_{GS} = 10V$)
 $< 68m\Omega$ ($V_{GS} = 4.5V$)

100% UIS Tested
100% R_g Tested

P-Channel

$-30V$
 $-3.5A$ ($V_{GS} = -10V$)
 $R_{DS(ON)} < 100m\Omega$ ($V_{GS} = -10V$)
 $< 165m\Omega$ ($V_{GS} = -4.5V$)

100% UIS Tested
100% R_g Tested



Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current	I_D	4.5	-3.5	A
$T_A = 25^\circ C$				
Current	I_D	3.5	-2.5	A
$T_A = 70^\circ C$				
Pulsed Drain Current ^C	I_{DM}	25	-20	
Avalanche Current ^C	I_{AS}, I_{AR}	8	-8	A
Avalanche energy $L = 0.1mH$ ^C	E_{AS}, E_{AR}	3	3	mJ
Power Dissipation ^B	P_D	2	2	W
		1.3	1.3	
$T_A = 25^\circ C$				
$T_A = 70^\circ C$				
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	48	62.5	$^\circ C/W$
$t \leq 10s$				
Maximum Junction-to-Ambient ^{A,B}	$R_{\theta JA}$	74	90	$^\circ C/W$
Steady-State				
Maximum Junction-to-Lead	$R_{\theta JL}$	32	40	$^\circ C/W$
Steady-State				

N-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.5	2	2.5	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =4.5A T _J =125°C		39 63	50 78	mΩ
		V _{GS} =4.5V, I _D =3A		50	68	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =4.5A		10		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.79	1	V
I _S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, f=1MHz	135	170	210	pF
C _{oss}	Output Capacitance		25	35	45	pF
C _{rss}	Reverse Transfer Capacitance		13	23	33	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.7	3.5	5.3	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =15V, I _D =4.5A		4.05	5	nC
Q _{g(4.5V)}	Total Gate Charge			2	3	nC
Q _{gs}	Gate Source Charge			0.55		nC
Q _{gd}	Gate Drain Charge			1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =15V, R _L =3.3Ω, R _{GEN} =3Ω		4.5		ns
t _r	Turn-On Rise Time			1.5		ns
t _{D(off)}	Turn-Off DelayTime			18.5		ns
t _f	Turn-Off Fall Time			15.5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =4.5A, dI/dt=100A/μs		7.5	10	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =4.5A, dI/dt=100A/μs		2.5		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

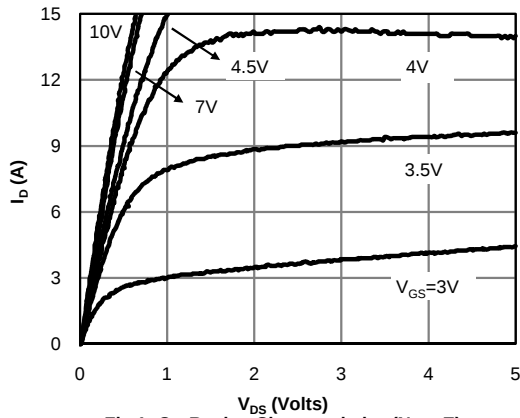


Fig 1: On-Region Characteristics (Note E)

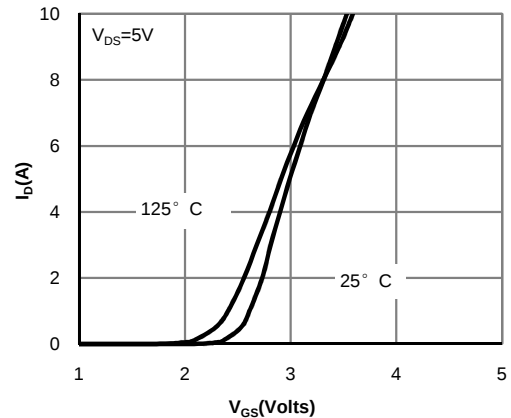


Figure 2: Transfer Characteristics (Note E)

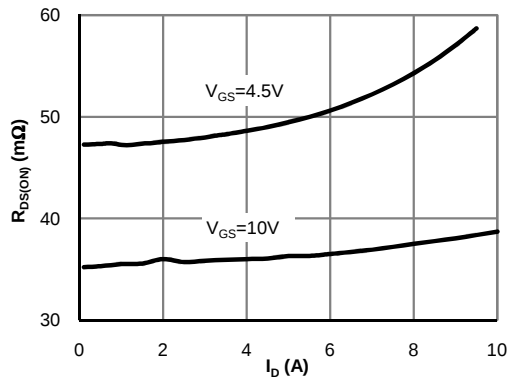


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

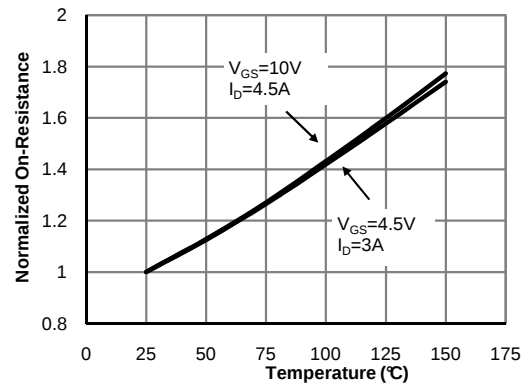


Figure 4: On-Resistance vs. Junction Temperature (Note E)

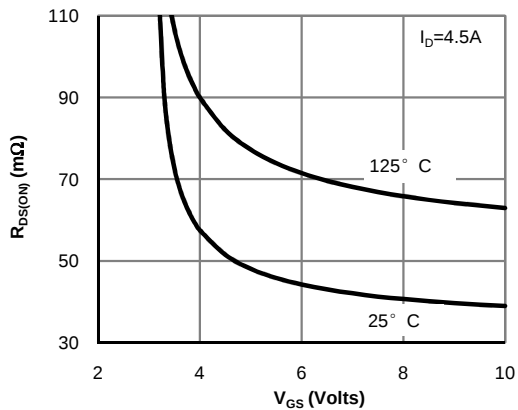


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

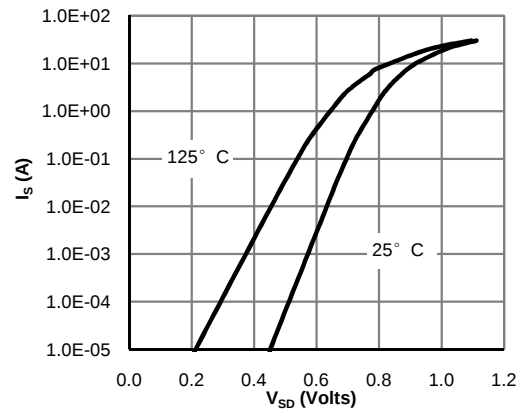
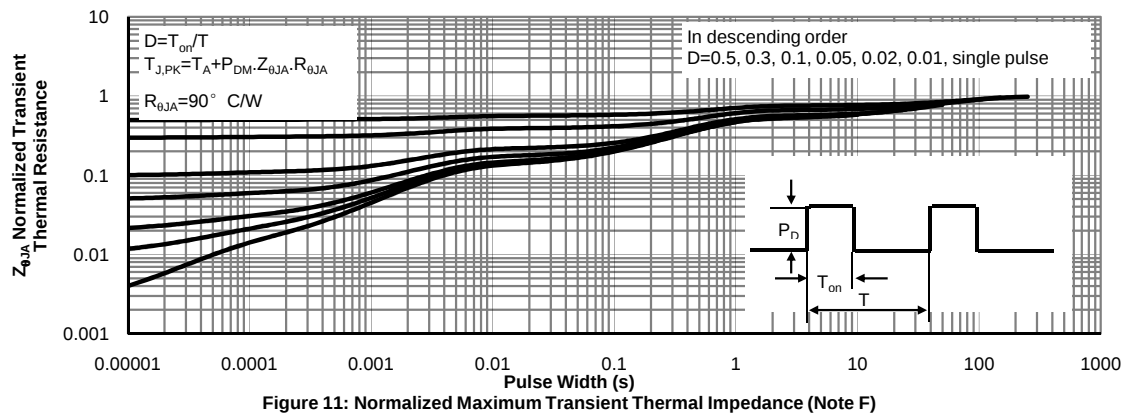
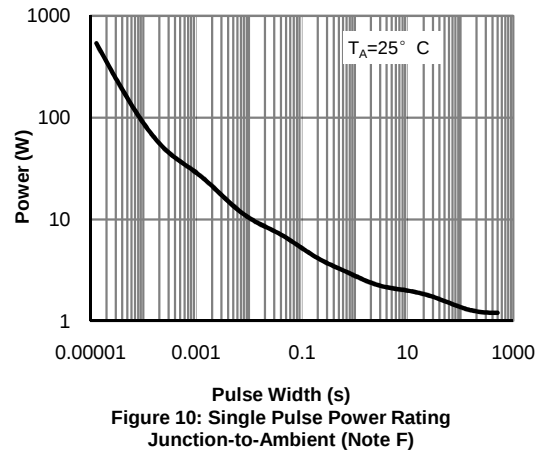
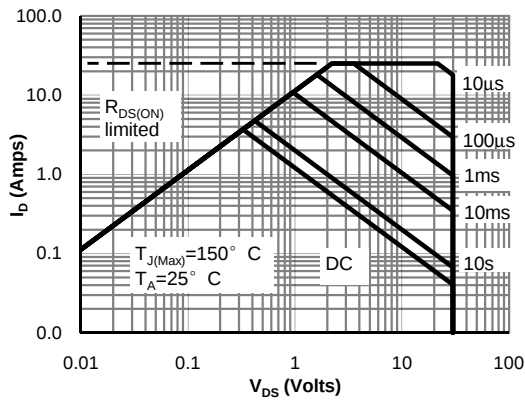
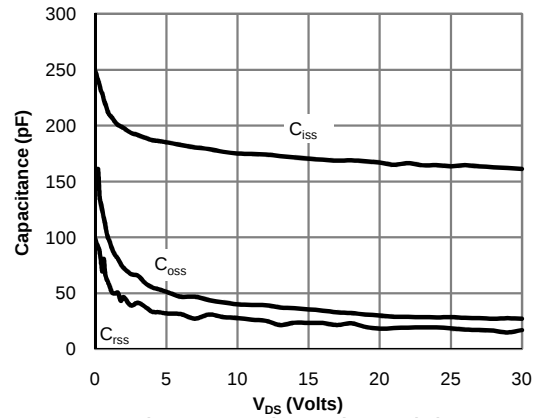
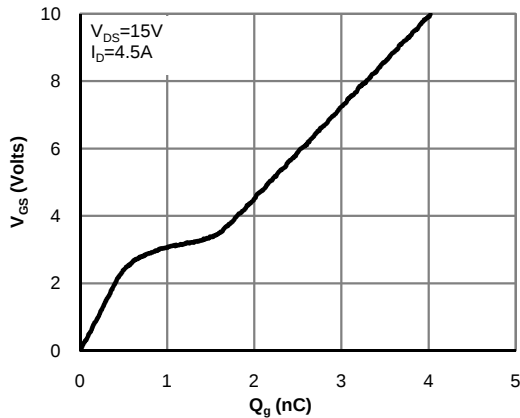
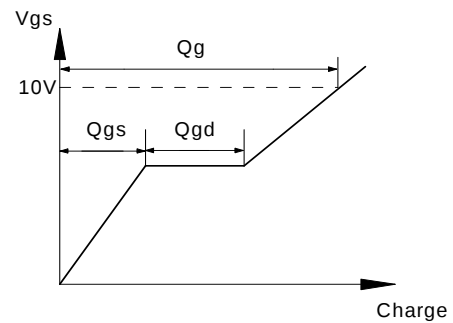
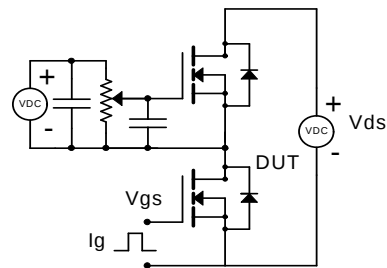


Figure 6: Body-Diode Characteristics (Note E)

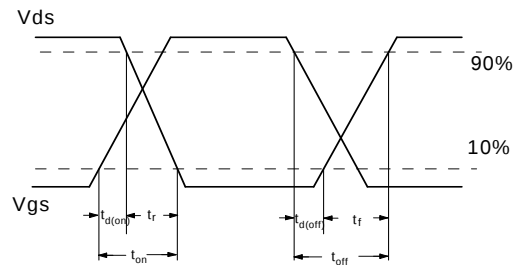
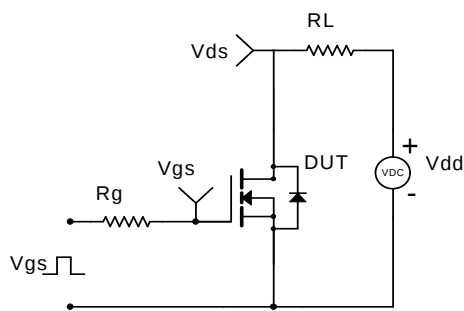
N-Channel: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



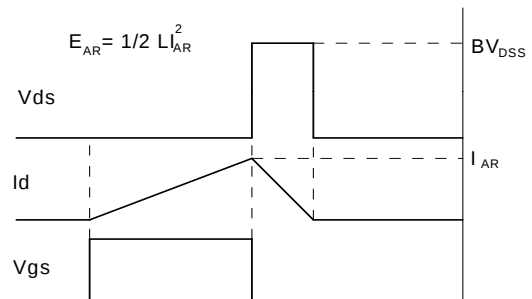
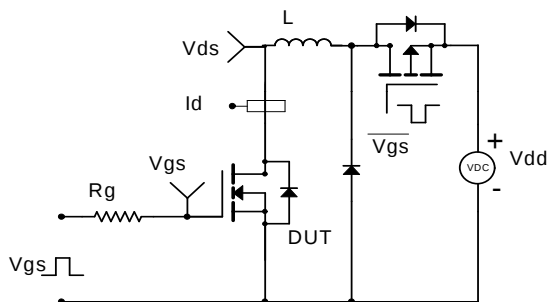
Gate Charge Test Circuit & Waveform



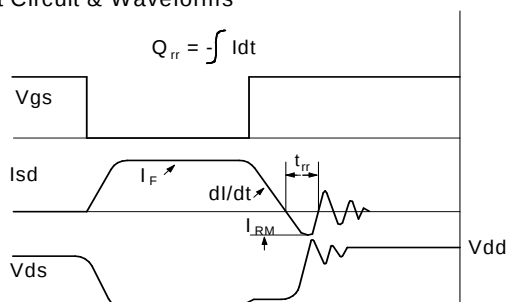
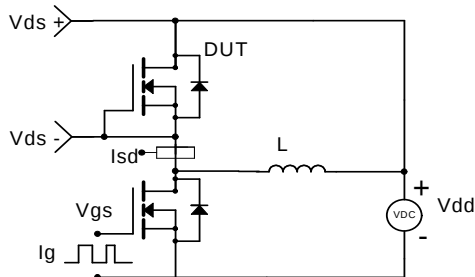
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.4	-1.9	-2.4	V
I _{D(ON)}	On state drain current	V _{GS} =-10V, V _{DS} =-5V	-20			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-3.5A T _J =125°C		78 111	100 140	mΩ
		V _{GS} =-4.5V, I _D =-2A		120	165	
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-3.5A		6		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.8	-1	V
I _S	Maximum Body-Diode Continuous Current				-2.5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz	155	197	240	pF
C _{oss}	Output Capacitance		28	42	55	pF
C _{rss}	Reverse Transfer Capacitance		15	26	37	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	3.5	7.2	11	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =-15V, I _D =-3.5A		4.3	5.2	nC
Q _{g(4.5V)}	Total Gate Charge			2.2	3	nC
Q _{gs}	Gate Source Charge			0.7		nC
Q _{gd}	Gate Drain Charge			1.1		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =-15V, R _L =4Ω, R _{GEN} =3Ω		7.5		ns
t _r	Turn-On Rise Time			4.1		ns
t _{D(off)}	Turn-Off DelayTime			11.8		ns
t _f	Turn-Off Fall Time			3.8		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-3.5A, dI/dt=100A/μs		11.3	14	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-3.5A, dI/dt=100A/μs		4.4		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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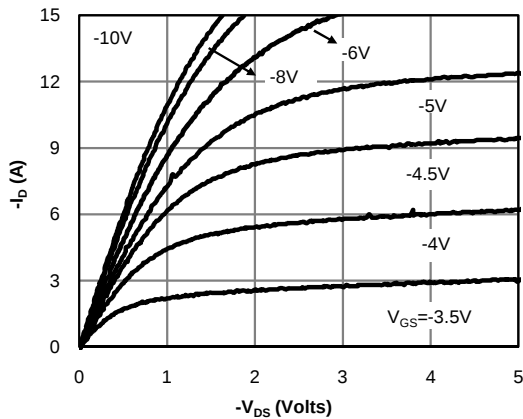


Fig 1: On-Region Characteristics (Note E)

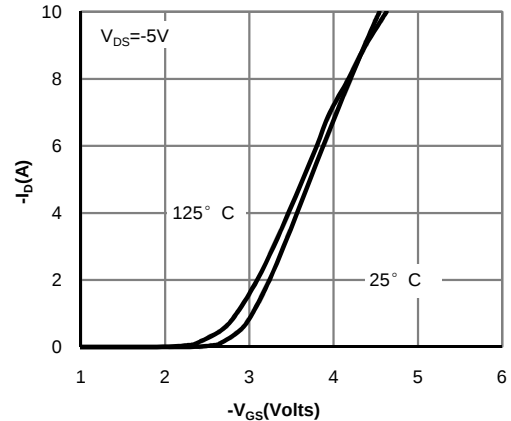


Figure 2: Transfer Characteristics (Note E)

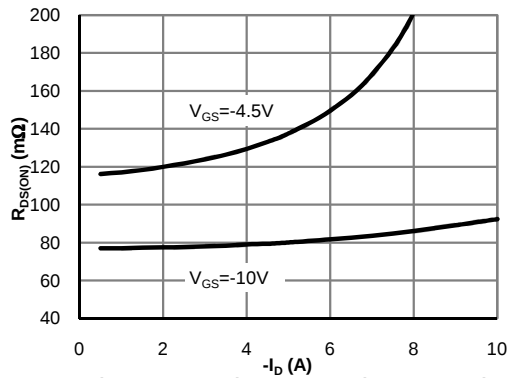


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

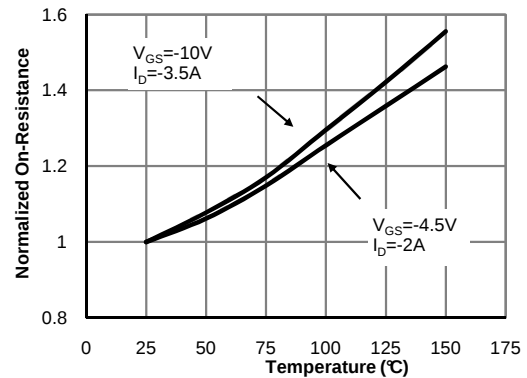


Figure 4: On-Resistance vs. Junction Temperature (Note E)

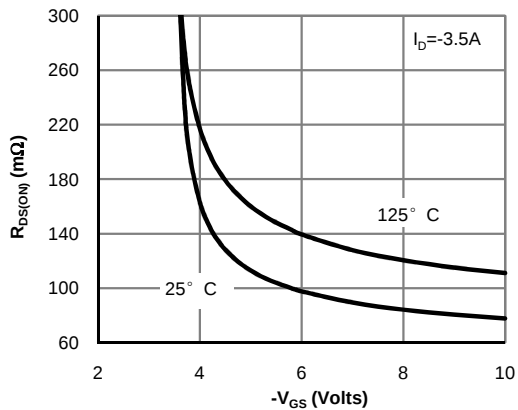


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

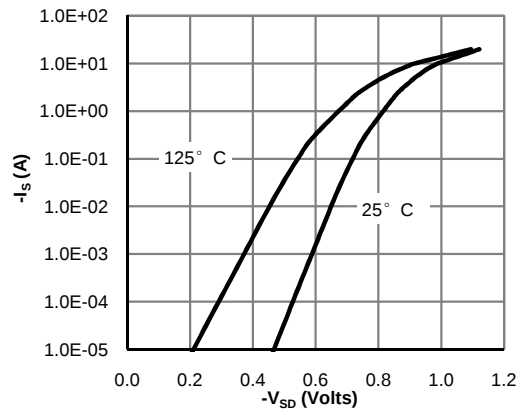
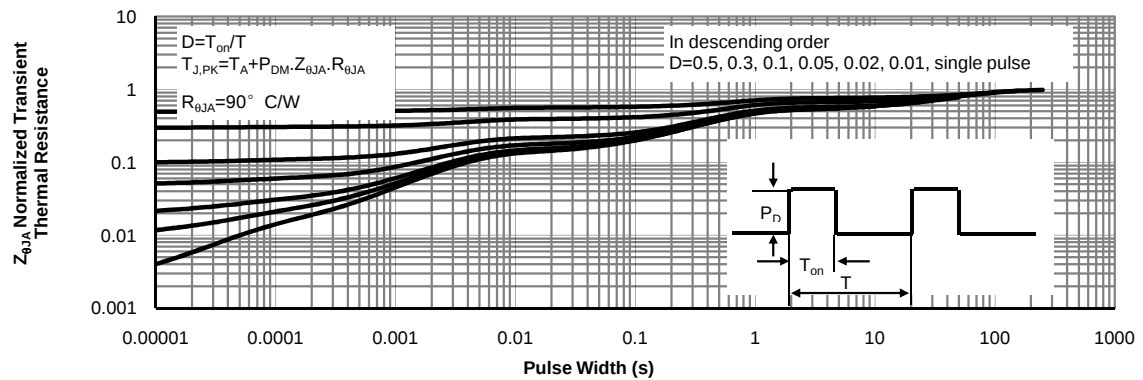
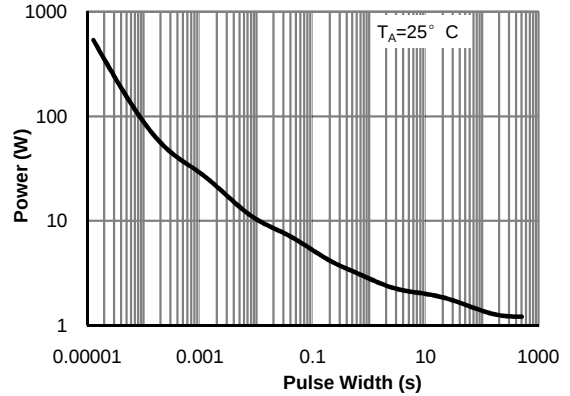
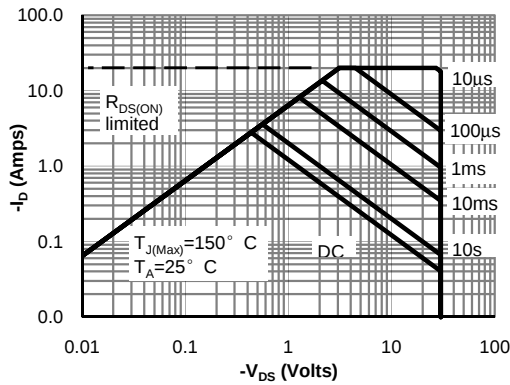
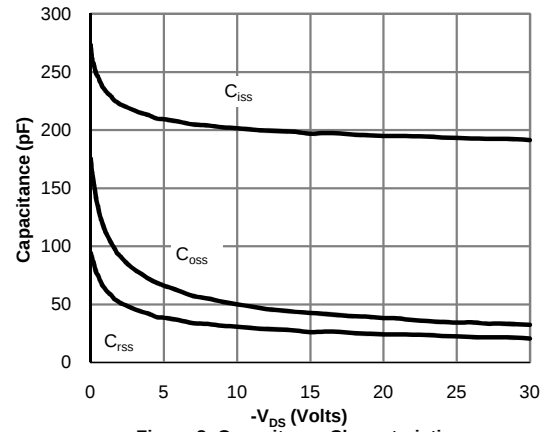
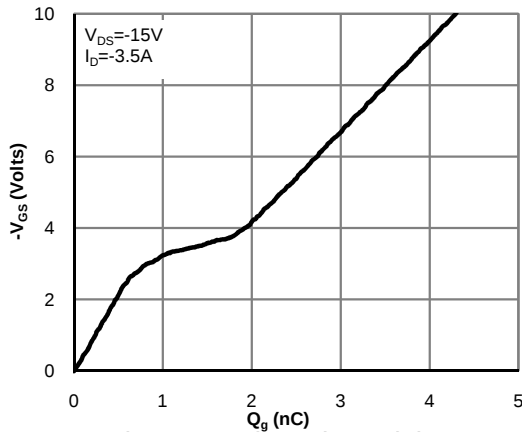
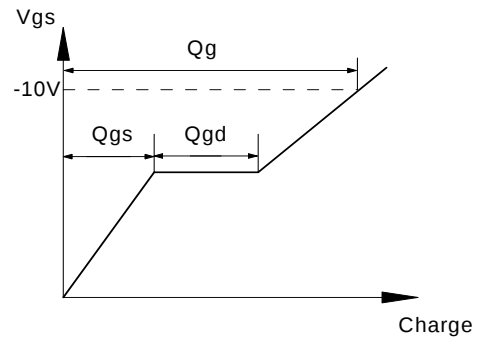
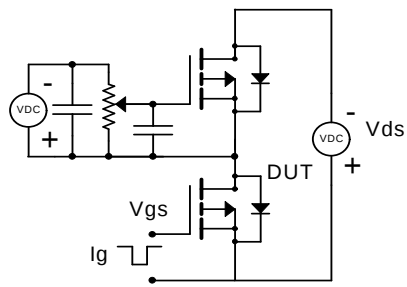


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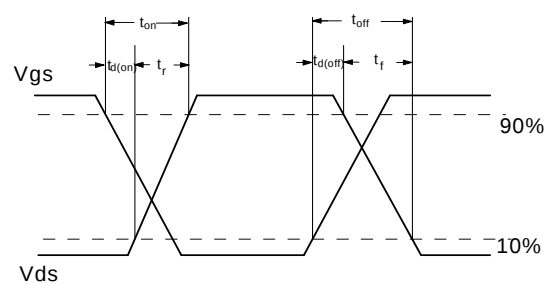
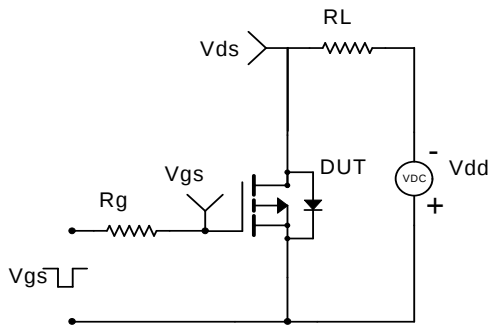
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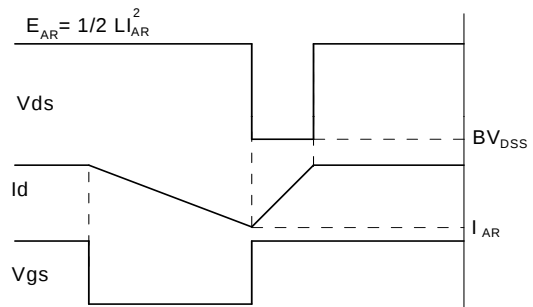
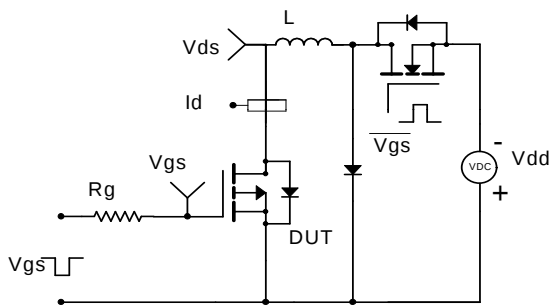
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

