National Semiconductor

LM49101

Boomer® Audio Power Amplifier Series

March 23, 2009

Mono Class AB Audio Subsystem with a True Ground Headphone Amplifier and Earpiece Switch

General Description

The LM49101 is a fully integrated audio subsystem with a mono power amplifier capable of delivering 540mW of continuous average power into an 8Ω BTL speaker load with 1% THD+N using a 3.3V supply. The LM49101 includes a separate stereo headphone amplifier that can deliver 44mW per channel into 32Ω loads using a 2.75V supply.

The LM49101 has four input channels. A pair of single-ended inputs and a fully differential input channel with volume control and amplification stages. Additionally, a bypass differential input is available that connects directly to the mono speaker outputs through an analog switch without any amplification or volume control stages. The LM49101 features a 32–step digital volume control on the input stage and an 8–step digital volume control on the headphone output stage.

The digital volume control and output modes, programmed through a two-wire I²C compatible interface, allows flexibility in routing and mixing audio channels.

The LM49101 is designed for cellular phones, PDAs, and other portable handheld applications. The high level of integration minimizes external components. The True Ground headphone amplifier eliminates the physically large DC blocking output capacitors reducing required board space and reducing cost.

Key Specifications

- Supply Voltage ($V_{DD}LS$) — $2.7V \leq V_{DD}LS \leq 5.5V$
- Supply Voltage ($V_{DD}HP$) — $1.8V \leq V_{DD}HP \leq 2.9V$
- I²C Supply Voltage — $1.7V \leq I^2CV_{DD} \leq 5.5V$
- Output power

  $V_{DD}LS = 5V$, $V_{DD}HP = 2.75V$
  1% THD+N

$R_L = 8\Omega$ speaker	1.3W (typ)
$R_L = 32\Omega$ headphone	45mW (typ)

- Output Power

  $V_{DD}LS = 3.3V$, $V_{DD}HP = 2.75V$
  1% THD+N

$R_L = 8\Omega$ speaker	540W (typ)
$R_L = 32\Omega$ headphone	40mW (typ)

- PSRR:

  $V_{DD} = 3.3V$, 217Hz ripple, Mono In — 90dB (typ)
- Shutdown power supply current — 0.01µA (typ)

Features

- Differential mono input and stereo single-ended input
- Separate earpiece (receiver) differential input
- Analog switch for a separate earpiece path
- 32-step digital volume control (-80 to +18dB)
- Three independent volume channels (Left, Right, Mono)
- Separate headphone volume control
- Flexible output for speaker and headphone output
- True Ground headphone amplifier eliminates large DC blocking capacitors reducing PCB space and cost.
- Hardware reset function
- RF immunity topology
- “Click and Pop” suppression circuitry
- Thermal shutdown protection
- Micro-power shutdown
- I²C control interface
- Available in space-saving microSMD package

Applications

- Portable electronic devices
- Mobile Phones
- PDAs

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Typical Application

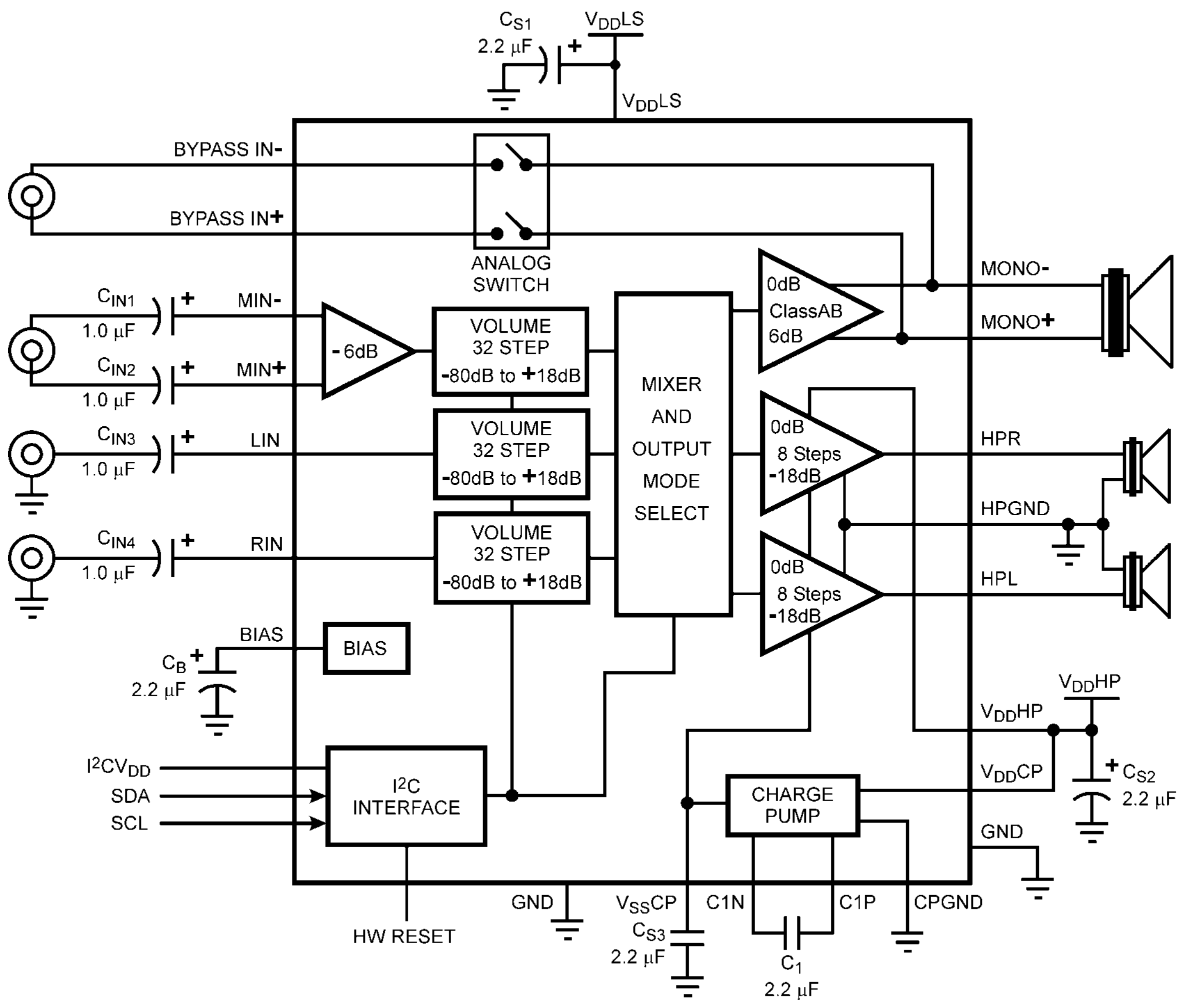
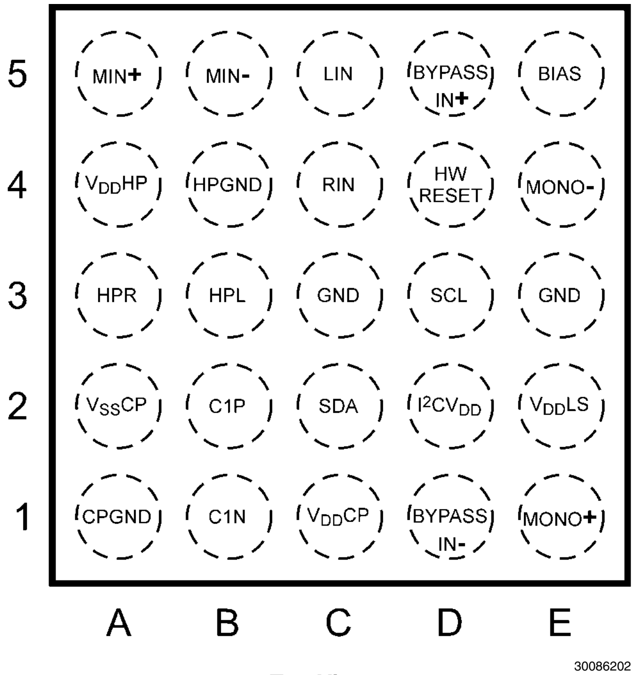


FIGURE 1. Typical Audio Application Circuit

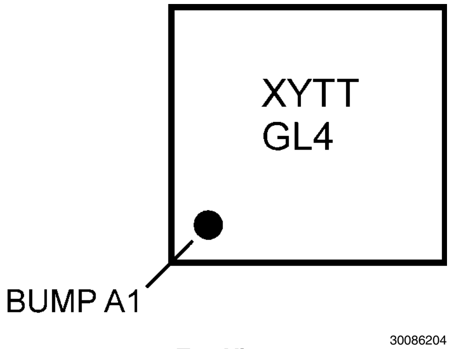
Connection Diagrams

25 Bump micro SMD Package



Top View
(Bump Side Down)
Order Number LM49101TM, LM49101TMX
See NS Package Number TMD25BCA

micro SMD Markings



Top View
XY - Date Code
TT - Die Traceability
G- Boomer Family
L4 - LM49101TM

Ordering Information

Order Number	Package	Package DWG #	Transport Media	MSL Level	Green Status	Features
LM49101TM	25 Bump micro SMD	TMD25BCA	250 units on tape and reel	1	RoHS and no Sb/Br	
LM49101TMX	25 Bump micro SMD	TMD25BCA	3000 units on tape and reel	1	RoHS and no Sb/Br	

Bump Descriptions

Bump	Name	Pin Function	Type
A1	CPGND	Charge pump ground terminal	Ground
A2	V_{SS}CP	Negative charge pump power supply	Power Output
A3	HPR	Right headphone output	Analog Output
A4	V_{DD}HP	Headphone amplifier power supply	Power Input
A5	MIN+	Positive input pin for the mono, differential input	Analog Input
B1	C1N	Negative terminal of the charge pump flying capacitor	Analog Output
B2	C1P	Positive terminal of the charge pump flying capacitor	Analog Output
B3	HPL	Left headphone output	Analog Output
B4	HPGND	Headphone signal ground	Ground
B5	MIN-	Negative input pin for the mono, differential input	Analog Input
C1	V_{DD}CP	Charge pump power supply	Power Input
C2	SDA	I^2C data	Digital Input
C3	GND	Ground	Ground
C4	RIN	Single-ended input for the right channel	Analog Input
C5	LIN	Single-ended input for the left channel	Analog Input
D1	BYPASS_IN-	Earpiece negative input, bypass volume control and amplifier	Analog Input
D2	I^2CV_{DD}	I^2C power supply	Power Input
D3	SCL	I^2C clock	Digital Input
D4	HW RESET	Hardware reset function, active low. When pin is low (<0.6V) the LM49101 goes into shutdown mode and will remain in shutdown mode until pin goes to logic high (>1.6V) and is activated by I^2C control. When reset all registers are set to the default value of 0.	Digital Input
D5	BYPASS_IN+	Earpiece positive input, bypass volume control and amplifier	Analog Input
E1	MONO+	Positive loudspeaker output	Analog Output
E2	V_{DD}LS	Main power supply	Power Input
E3	GND	Ground	Ground
E4	MONO-	Negative loudspeaker output	Analog Output
E5	BIAS	Half-supply bias, capacitor bypassed	Analog Output

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Loudspeaker, $V_{DD}LS$)	6.0V
Supply Voltage (Headphone, $V_{DD}HP$)	3.0V
Storage Temperature	−65°C to +150°C
Voltage at Any Input Pin	GND − 0.3 to $V_{DD}LS$ + 0.3
Power Dissipation (Note 3)	Internally Limited
ESD Rating (Note 4)	2000V
ESD Rating (Note 5)	200V
Junction Temperature (T_{JMAX})	150°C
Soldering Information	
Vapor Phase (60sec.)	215°C
Infrared (15sec.)	220°C
See AN-1112 “Micro SMD Wafer Level Chip Scale Package”	
Thermal Resistance	
θ_{JA} (Note 8)	51°C/W

Operating Ratings

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-40°C \leq T_A \leq 85°C$
Supply Voltage ($V_{DD}LS$)	$2.7V \leq V_{DD}LS \leq 5.5V$
Supply Voltage ($V_{DD}HP$)	$1.8V \leq V_{DD}HP \leq 2.9V$ $V_{DD}HP \leq V_{DD}LS$
Supply Voltage ($V_{DD}CP$)	$V_{DD}CP = V_{DD}HP$
Supply Voltage (I^2CV_{DD})	$1.7V \leq I^2CV_{DD} \leq 5.5V$ $I^2CV_{DD} \leq V_{DD}LS$

Electrical Characteristics $V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 2.75V (Notes 1, 2)

The following specifications apply for $V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 2.75V, T_A = 25°C, all volume controls set to 0dB, unless otherwise specified. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

Symbol	Parameter	Conditions	LM49101		Units (Limits)
			Typical (Note 6)	Limits (Note 7)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0, No Load			
		EP Receiver (Output Mode Bit EP Bypass = 1)	0.03	0.045	mA (max)
		LS only (Mode 1), GAMP_SD = 0 VDDLS VDDHP	 2.5 0	 4.2 	 mA (max) mA
		LS only (Mode 1), GAMP_SD = 1 VDDLS VDDHP	 2 0		 mA mA
		HP only (Mode 8), GAMP_SD = 0 VDDLS VDDHP VDDLS +VDDHP	 1.6 3.1 	 2.0 4.5 6.45	 mA (max) mA (max) mA (max)
		HP only (Mode 8), GAMP_SD = 1 VDDLS VDDHP	 2.8 3.3		 mA mA
		LS+HP (Mode 10), GAMP_SD = 0 VDDLS VDDHP VDDLS +VDDHP	 2.8 3.1 	 3.8 4.5 8	 mA (max) mA (max) mA (max)
I_{SD}	Shutdown Current	Power_On = 0	0.01	2	µA (max)
V_{OS}	Output Offset Voltage	V_{IN} = 0V, Mode 10 LS output, R_L = 8Ω BTL HP output, R_L = 32Ω SE	 2.5 0.5	 22 5	 mV (max) mV (max)
P_O	Output Power	LS output, Mode 1, R_L = 8Ω BTL THD+N = 1%, f = 1kHz, LS_Gain = 6dB	540	480	mW (min)
		HP output, Mode 8, R_L = 32Ω SE THD+N = 1%, f = 1kHz	44	40	mW (min)

Symbol	Parameter	Conditions	LM49101 Typical (Note 6)	LM49101 Limits (Note 7)	Units (Limits)
THD+N	Total Harmonic Distortion + Noise	LS output, f = 1kHz, R_L = 8Ω BTL P_O = 250mW, Mode 1, LS_Gain = 6dB	0.065		%
		HP output, f = 1kHz, R_L = 32Ω SE P_O = 20mW, Mode 8	0.015		%
SNR	Signal-to-Noise Ratio	LS output, f = 1kHz, Mode 1 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain & LS_GAIN = 0dB A-Wtg, LIN & RIN AC terminated	105		dB
		HP output, f = 1kHz, Mode 8 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain = 0dB, A-weighted LIN & RIN AC terminated	100		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} on $V_{DD}LS$ = 200mV_{PP}, f_{RIPPLE} = 217Hz, C_B = 2.2µF All inputs AC terminated to GND, output referred			
		LS: Mode 1, 5, 9, 13, R_L = 8Ω BTL	90		dB (max)
		LS: Mode 2, 6, 10 ,14, R_L = 8Ω BTL	75		dB (max)
		HP: Mode 4, 5, 6, 7, R_L = 32Ω SE	85		dB (max)
		HP: Mode 8, 9, 10, 11, R_L = 32Ω SE	81		dB (max)
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = 1V_{P-P} LS: R_L = 8Ω BTL, Mode 1 HP: R_L = 32Ω SE, Mode 4	60 60		dB dB
X_{TALK}	Crosstalk	HP P_O = 20mW f = 1kHz, Mode 8	72		dB
Z_{IN}	MIN, LIN, and RIN Input Impedance	Maximum Gain setting	12.5	10 15	KΩ (min) KΩ (max)
		Maximum Attenuation setting	110	90 130	KΩ (min) KΩ (max)
R_{ON}	On Resistance	Analog Switch On	3.4		Ω
VOL	Digital Volume Control Range	Maximum Gain Maximum Attenuation	18 –80		dB dB
VOL	Volume Control Step Size Error		±0.02		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, HP, Normal Turn-On Mode	30		ms
		C_B = 2.2µF, HP, Fast Turn-On Mode	15		ms

Electrical Characteristics $V_{DD}LS = 5.0V$, $V_{DD}HP = 2.75V$ (Notes 1, 2)

The following specifications apply for $V_{DD}LS = 5.0V$, $V_{DD}HP = 2.75V$, $T_A = 25°C$, all volume controls set to 0dB, unless otherwise specified. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

Symbol	Parameter	Conditions	LM49101 Typical (Note 6)	LM49101 Limits (Note 7)	Units (Limits)
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0$, No Load			
		EP Receiver (Output Mode Bit EP Bypass = 1)	0.05	0.07	mA (max)
		LS only (Mode 1), GAMP_SD = 0 VDDLS VDDHP	 2.9 0	 4.4 	 mA (max) mA
		LS only (Mode 1), GAMP_SD = 1 VDDLS VDDHP	 2.1 0		 mA mA
		HP only (Mode 8), GAMP_SD = 0 VDDLS VDDHP VDDLS+VDDHP	 1.8 3.1 	 2.15 4.5 6.6	 mA (max) mA (max) mA (max)
		HP only (Mode 8), GAMP_SD = 1 VDDLS VDDHP	 1.3 3.1		 mA mA
		LS+HP only (Mode 10), GAMP_SD = 0 VDDLS VDDHP VDDLS+VDDHP	 3 3.1 	 4.1 4.5 8.35	 mA (max) mA (max) mA (max)
I_{SD}	Shutdown Current	Power_On = 0	0.01	2	μA (max)
V_{OS}	Output Offset Voltage	$V_{IN} = 0V$, Mode 10 LS output, $R_L = 8\Omega$ BTL HP output, $R_L = 32\Omega$ SE	 2.5 0.5	 22 5	 mV (max) mV (max)
P_O	Output Power	LS output, Mode 1, $R_L = 8\Omega$ BTL THD+N = 1%, f = 1kHz, LS_Gain = 6dB	1.3		W
		HP output, Mode 8, $R_L = 32\Omega$ SE THD+N = 1%, f = 1kHz	45		mW
THD+N	Total Harmonic Distortion + Noise	LS output, f = 1kHz, $R_L = 8\Omega$ BTL P_O = 600mW, Mode 1, LS_Gain = 6dB	0.055		%
		HP output, f = 1kHz, $R_L = 32\Omega$ SE P_O = 20mW, Mode 8	0.015		%
SNR	Signal-to-Noise Ratio	LS output, f = 1kHz, Mode 1 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain & LS_GAIN = 0dB A-Wtg, LIN & RIN AC terminated	108		dB
		HP output, f = 1kHz, Mode 8 $V_{REF} = V_{OUT}$ (1%THD+N) Vol. Gain = 0dB, A-weighted LIN & RIN AC terminated	100		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} on $V_{DD}LS = 200mV_{PP}$, $f_{RIPPLE} = 217Hz$, $C_B = 2.2\mu F$ All inputs AC terminated to GND, output referred			
		LS: Mode 1, 5, 9, 13, $R_L = 8\Omega$ BTL	90		dB
		LS: Mode 2, 6, 10, 14, $R_L = 8\Omega$ BTL	74		dB
		HP: Mode 4, 5, 6, 7, $R_L = 32\Omega$ SE	84		dB
		HP: Mode 8, 9, 10, 11, $R_L = 32\Omega$ SE	79		dB

Symbol	Parameter	Conditions	LM49101		Units (Limits)
			Typical (Note 6)	**Limits** (Note 7)	
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V_{CM} = $1V_{P-P}$ LS: R_L = 8Ω BTL, Mode 1 HP: R_L = 32Ω SE, Mode 4	 60 60		 dB dB
X_{TALK}	Crosstalk	HP P_O = 20mW f = 1kHz, Mode 8	72		dB
Z_{IN}	MIN, LIN, and RIN Input Impedance	Maximum Gain setting	12.5	10 15	KΩ (min) KΩ (max)
		Maximum Attenuation setting	110	90 130	KΩ (min) KΩ (max)
R_{ON}	On Resistance	Analog Switch On	2		Ω
VOL	Digital Volume Control Range	Maximum Gain Maximum Attenuation	18 –80		dB dB
VOL	Volume Control Step Size Error		±0.02		dB
T_{WU}	Wake-Up Time from Shutdown	C_B = 2.2µF, HP, Normal Turn-On Mode	30		ms
		C_B = 2.2µF, HP, Fast Turn-On Mode	15		ms

I²C Interface 2.2V ≤ I²C_V_{DD} ≤ 5.5V, (Notes 1, 2)

The following specifications apply for V_{DD}LS = 5.0V and 3.3V, 2.2V ≤ I²C_V_{DD} ≤ 5.5V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	LM49101 Typical (Note 4)	LM49101 Limits (Notes 7, 9)	Units (Limits)
t_1	I²C Clock Period			2.5	μs (min)
t_2	I²C Data Setup Time			100	ns (min)
t_3	I²C Data Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
t_6	I²C Data Hold Time			100	ns (min)
V_{IH}	I²C Input Voltage High			0.7xI²CV_{DD}	V (min)
V_{IL}	I²C Input Voltage Low			0.3xI²CV_{DD}	V (max)

I²C Interface 1.7V ≤ I²C_V_{DD} ≤ 2.2V, (Notes 1, 2)

The following specifications apply for V_{DD}LS = 5.0V and 3.3V, T_A = 25°C, 1.7V ≤ I²C_V_{DD} ≤ 2.2V, unless otherwise specified.

Symbol	Parameter	Conditions	LM49101 Typical (Note 6)	LM49101 Limits (Notes 7, 9)	Units (Limits)
t_1	I²C Clock Period			2.5	μs (min)
t_2	I²C Data Setup Time			250	ns (min)
t_3	I²C Data Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	I²C Data Hold Time			250	ns (min)
V_{IH}	I²C Input Voltage High			0.7xI²CV_{DD}	V (min)
V_{IL}	I²C Input Voltage Low			0.3xI²CV_{DD}	V (max)

Note 1: *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

Note 2: The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Typical values represent most likely parametric norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

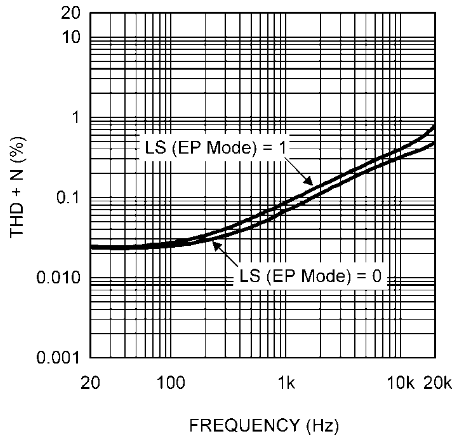
Note 7: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Note 8: The given θ_{JA} is for an LM49101 mounted on a demonstration board.

Note 9: Refer to the I²C timing diagram, Figure 2.

Typical Performance Characteristics

THD+N vs Frequency
$V_{DD}LS = 3.3V$, $R_L = 8\Omega$ BTL, $P_O = 250mW$
Mode 1 (Mono), 80kHz BW



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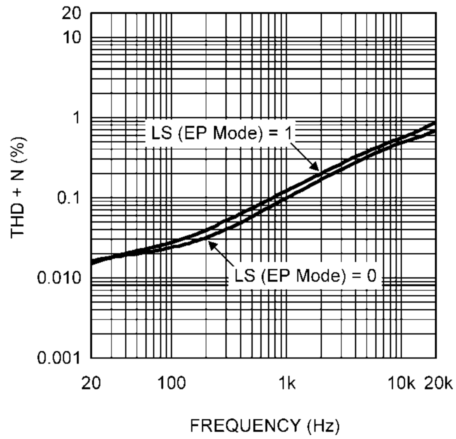
THD+N vs Frequency
$V_{DD}LS = 3.3V$, $R_L = 8\Omega$ BTL, $P_O = 250mW$
Mode 2 (Left + Right), 80kHz BW



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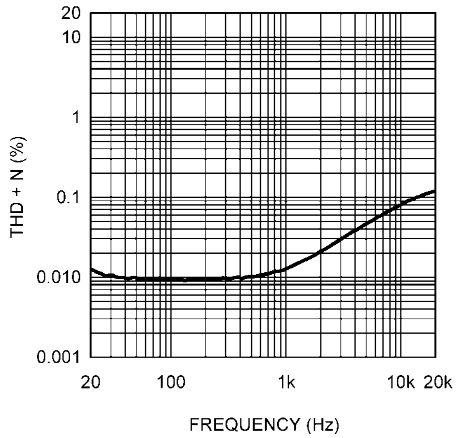
THD+N vs Frequency
$V_{DD}LS = 3.3V$, $V_{DD}HP = 1.8V$, $R_L = 32\Omega$ SE,
$P_O = 5mW/Ch$, Mode 4 (Mono), 80kHz BW



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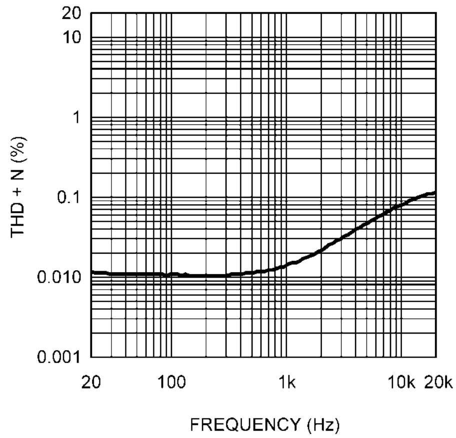
THD+N vs Frequency
$V_{DD}LS = 3.3V$, $V_{DD}HP = 1.8V$, $R_L = 32\Omega$ SE,
$P_O = 5mW/Ch$, Mode 8 (Left/Right), 80kHz BW



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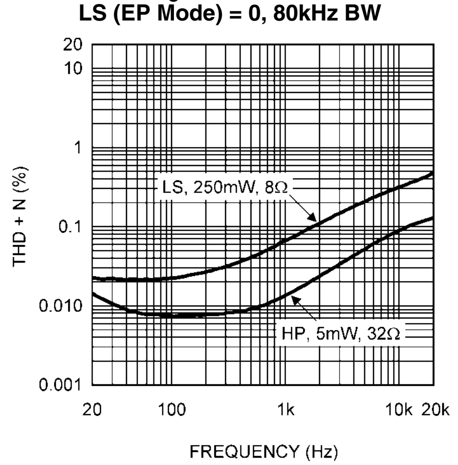
THD+N vs Frequency
$V_{DD}LS = 3.3V$, $V_{DD}HP = 1.8V$, $R_L = 8\Omega$ BTL, $R_L = 32\Omega$ SE,
$P_O = 250mW$ BTL, $P_O = 5mW/Ch$ SE, Mode 5 (Mono)
LS (EP Mode) = 0, 80kHz BW



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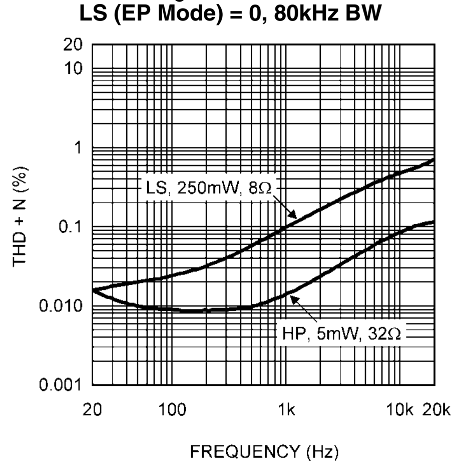
THD+N vs Frequency
$V_{DD}LS = 3.3V$, $V_{DD}HP = 1.8V$, $R_L = 8\Omega$ BTL, $R_L = 32\Omega$ SE,
$P_O = 250mW$ BTL, $P_O = 5mW/Ch$ SE, Mode 10 (L/R)
LS (EP Mode) = 0, 80kHz BW



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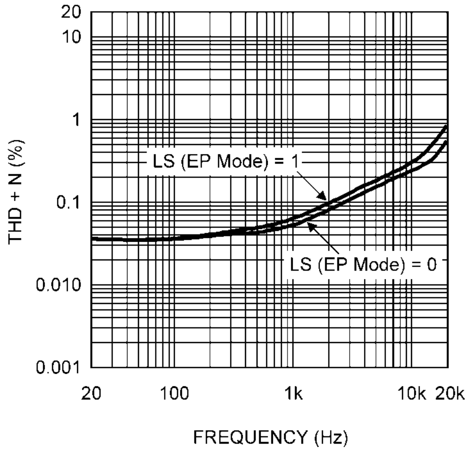
THD+N vs Frequency
$V_{DD}LS$ = 5V, R_L = 8Ω BTL, P_O = 600mW, Mode 1 (Mono), 80kHz BW



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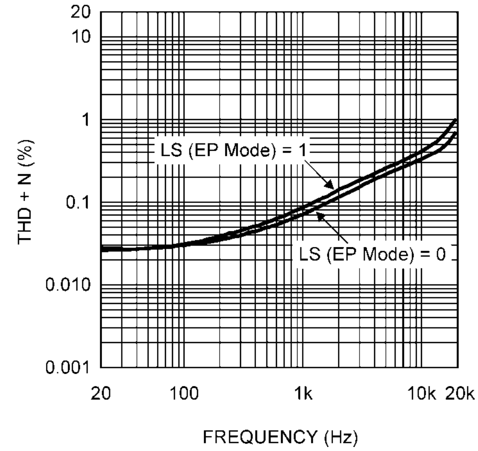
THD+N vs Frequency
$V_{DD}LS$ = 5V, R_L = 8Ω BTL, P_O = 600mW, Mode 2 (Let + Right), 80kHz BW



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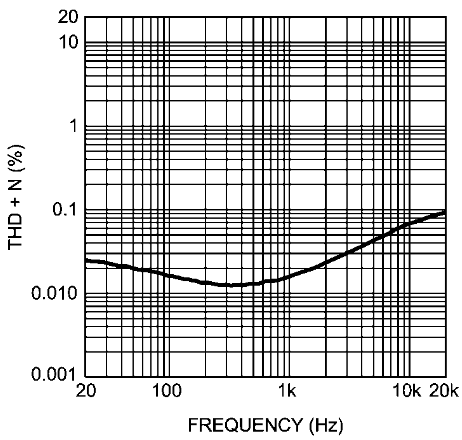
THD+N vs Frequency
$V_{DD}LS$ = 5V, $V_{DD}HP$ = 2.75V, R_L = 32Ω SE, P_O = 20mW/Ch, Mode 4 (Mono), 80kHz BW



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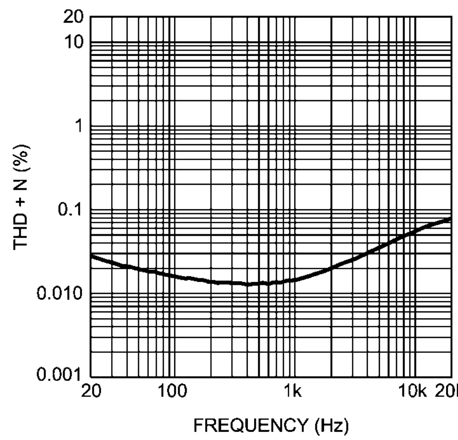
THD+N vs Frequency
$V_{DD}LS$ = 5V, $V_{DD}HP$ = 2.75V, R_L = 32Ω SE, P_O = 20mW/Ch, Mode 8 (Left/Right), 80kHz BW



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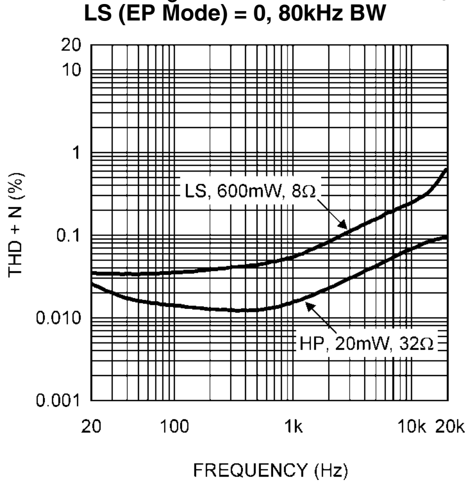
THD+N vs Frequency
$V_{DD}LS$ = 5V, $V_{DD}HP$ = 2.75V, R_L = 8Ω BTL, R_L = 32Ω SE, P_O = 600mW BTL, P_O = 20mW/Ch SE, Mode 5 (Mono) LS (EP Mode) = 0, 80kHz BW



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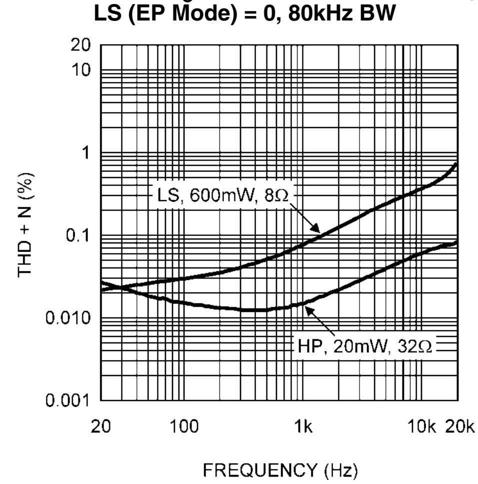
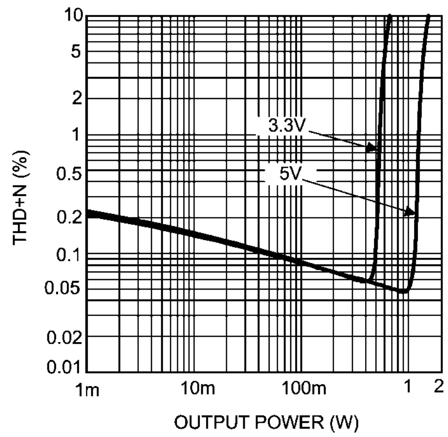
THD+N vs Frequency
$V_{DD}LS$ = 5V, $V_{DD}HP$ = 2.75V, R_L = 8Ω BTL, R_L = 32Ω SE, P_O = 600mW BTL, P_O = 20mW/Ch SE, Mode 10 (L/R) LS (EP Mode) = 0, 80kHz BW



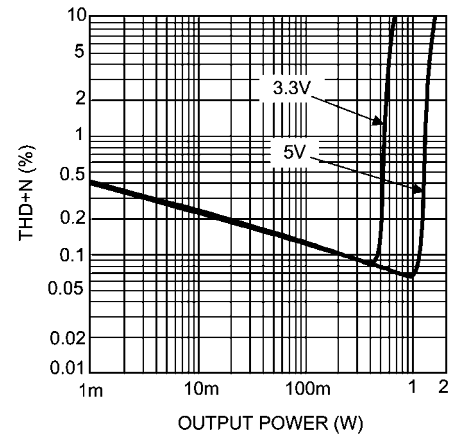
30086230

THD+N vs Output Power
$V_{DD}LS$ = 3.3V & 5V, f = 1kHz, R_L = 8Ω BTL
Mode 1 (Mono), 80kHz BW



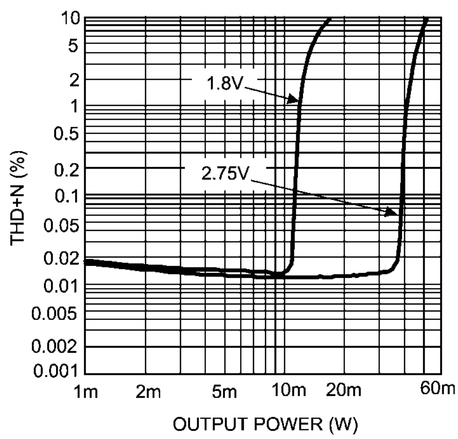
30086243

THD+N vs Output Power
$V_{DD}LS$ = 3.3V & 5V, f = 1kHz, R_L = 8Ω BTL
Mode 2 (Left + Right), 80kHz BW



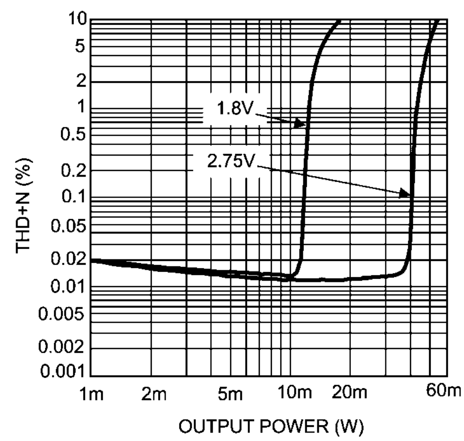
30086244

THD+N vs Output Power
$V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 1.8V & 2.75V, f = 1kHz,
R_L = 32Ω SE, Mode 4 (Mono), 80kHz BW



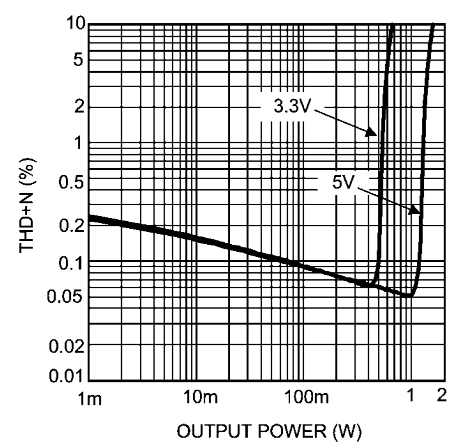
30086245

THD+N vs Output Power
$V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 1.8V & 2.75V, f = 1kHz,
R_L = 32Ω SE, Mode 8 (Left/Right), 80kHz BW



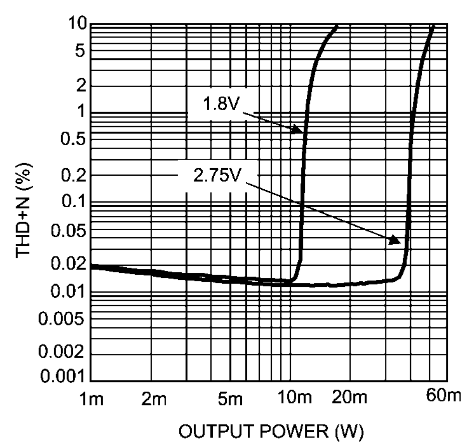
30086246

THD+N vs Output Power
$V_{DD}LS$ = 3.3V & 5V, $V_{DD}HP$ = 2.75V, f = 1kHz,
R_L = 8Ω BTL, Mode 5 (Mono), 80kHz BW



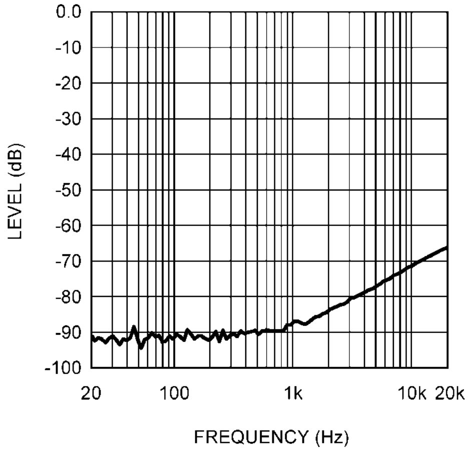
30086242

THD+N vs Output Power
$V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 1.8V & 2.75V, f = 1kHz,
R_L = 32Ω SE, Mode 10 (Left/Right), 80kHz BW



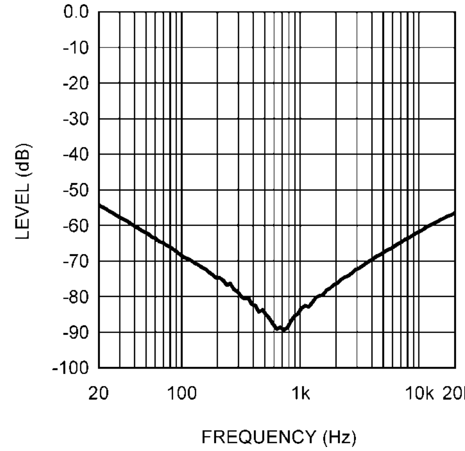
30086247

PSRR vs Frequency
$V_{DD}LS = 3.3V$, $V_{RIPPLE}LS = 200mV_{PP}$, $R_L = 8\Omega$ BTL, Mode 1 (Mono), 80kHz BW



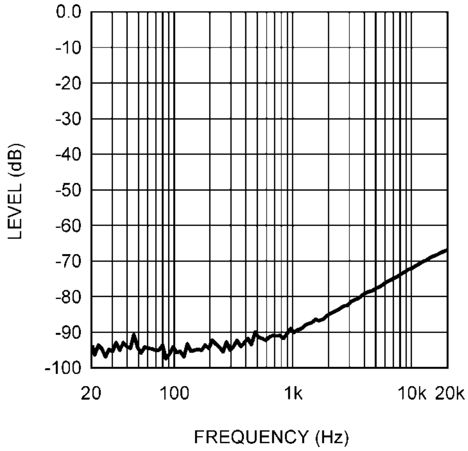
30086211

PSRR vs Frequency
$V_{DD}LS = 3.3V$, $V_{RIPPLE}LS = 200mV_{PP}$, $R_L = 8\Omega$ BTL, Mode 2 (Left + Right), 80kHz BW



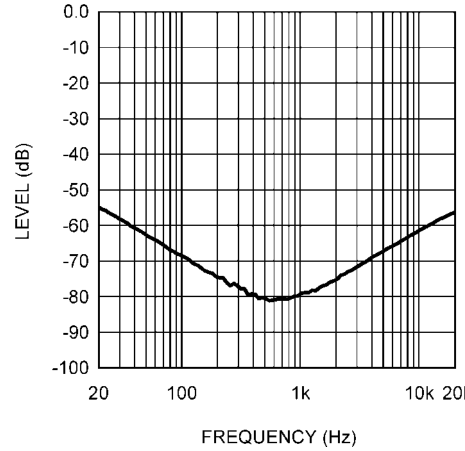
30086213

PSRR vs Frequency
$V_{DD}LS = 5V$, $V_{RIPPLE}LS = 200mV_{PP}$, $R_L = 8\Omega$ BTL, Mode 1 (Mono), 80kHz BW



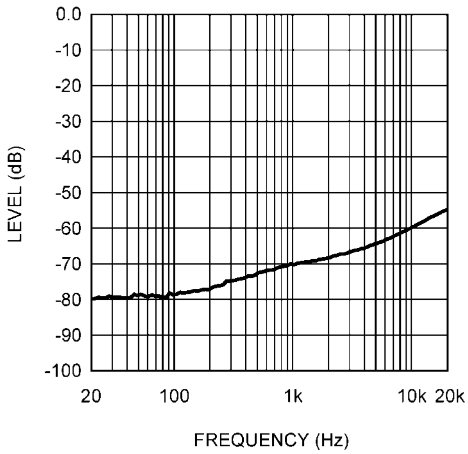
30086212

PSRR vs Frequency
$V_{DD}LS = 5V$, $V_{RIPPLE}LS = 200mV_{PP}$, $R_L = 8\Omega$ BTL, Mode 2 (Left + Right), 80kHz BW



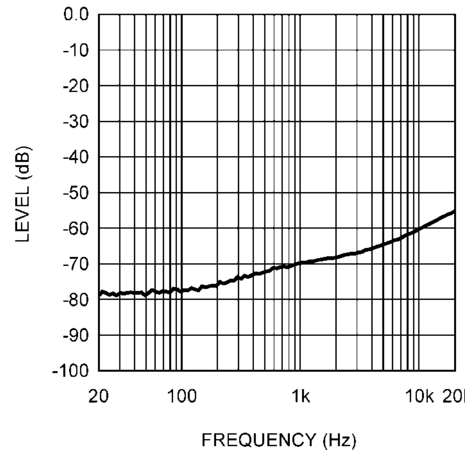
30086214

PSRR vs Frequency
$V_{DD}LS = 3.3V$, $V_{DD}HP = 1.8V$, $V_{RIPPLE}HP = 200mV_{PP}$, $R_L = 32\Omega$ SE, Mode 4 (Mono), 80kHz BW



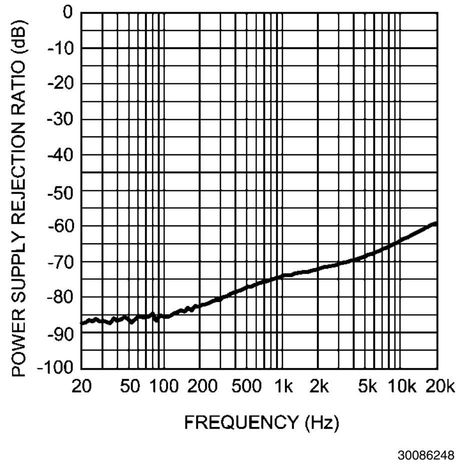
30086215

PSRR vs Frequency
$V_{DD}LS = 3.3V$, $V_{DD}HP = 1.8V$, $V_{RIPPLE}HP = 200mV_{PP}$, $R_L = 32\Omega$ SE, Mode 8 (Left/Right), 80kHz BW

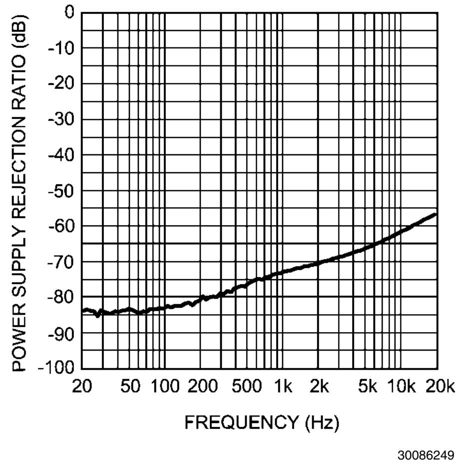


30086217

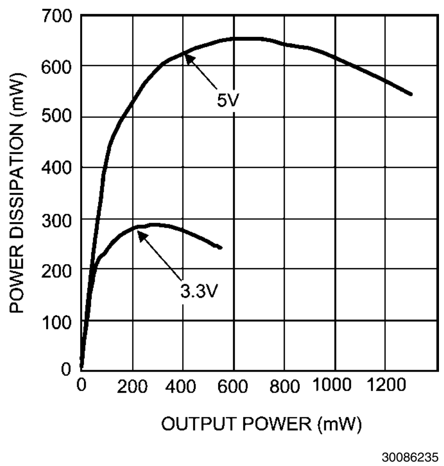
PSRR vs Frequency
$V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 2.75V, $V_{RIPPLE}HP$ = 200mV_{PP},
R_L = 32Ω SE, Mode 4 (Mono), 80kHz BW



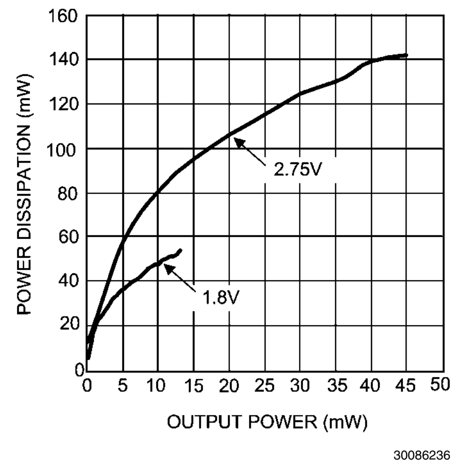
PSRR vs Frequency
$V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 2.75V, $V_{RIPPLE}HP$ = 200mV_{PP},
R_L = 32Ω SE, Mode 8 (Left/Right), 80kHz BW



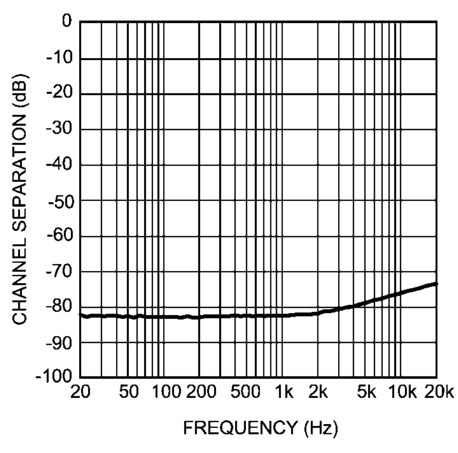
Power Dissipation vs Output Power
$V_{DD}LS$ = 3.3V & 5V, $V_{DD}HP$ = 2.75V, R_L = 8Ω BTL,
Mode 3 (Mono + Left + Right), 80kHz BW



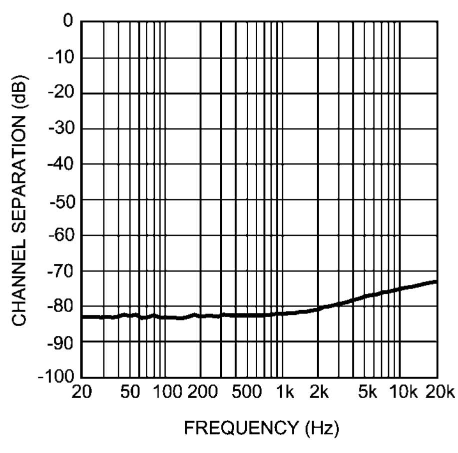
Power Dissipation vs Output Power
$V_{DD}LS$ = 5V, $V_{DD}HP$ = 1.8V & 2.75V, R_L = 32Ω SE,
Mode 12 (Mono + Left/ Right), 80kHz BW



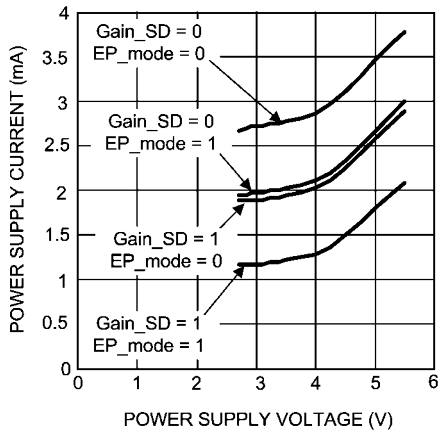
Crosstalk vs Frequency
$V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 1.8V, V_{IN} = 1V_{PP},
R_L = 32Ω SE, Mode 8 (Left/Right), 80kHz BW



Crosstalk vs Frequency
$V_{DD}LS$ = 3.3V, $V_{DD}HP$ = 2.75V, V_{IN} = 1V_{PP},
R_L = 32Ω SE, Mode 8 (Left/Right), 80kHz BW

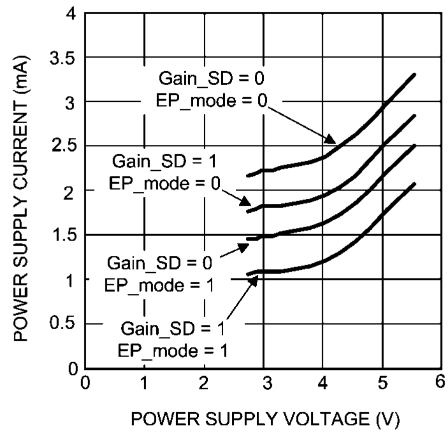


Supply Current vs Supply Voltage (V_{DD}LS)
V_{DD}HP = 2.75V, No Load, Gain_SD = 0 & 1
LS (EP_Mode) = 0 & 1, Mode 1



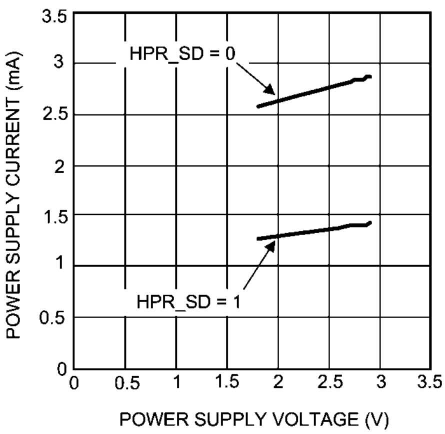
30086237

Supply Current vs Supply Voltage (V_{DD}LS)
V_{DD}HP = 2.75V, No Load, Gain_SD = 0 & 1
LS (EP_Mode) = 0 & 1, Mode 2



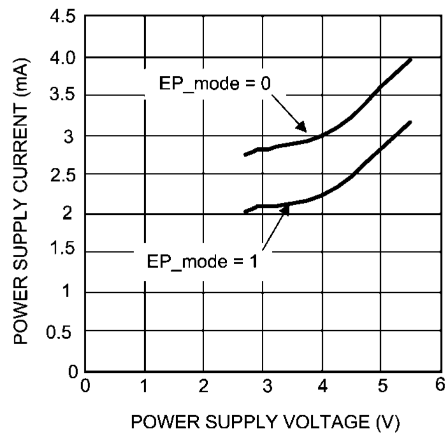
30086239

Supply Current vs Supply Voltage (V_{DD}HP)
V_{DD}LS = 3.3V, No Load, Gain_SD = 0 or 1
HPR_SD = 0 & 1, Modes 4, 8, 15



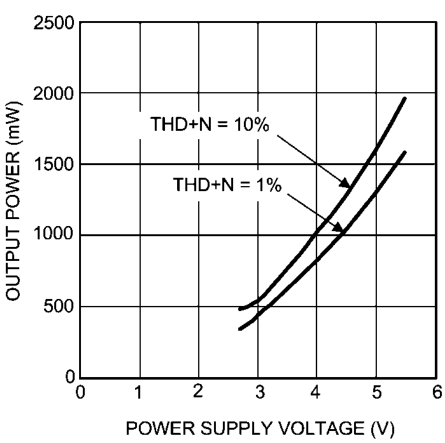
30086238

Supply Current vs Supply Voltage (V_{DD}LS)
V_{DD}HP = 2.75V, No Load, Gain_SD = 0 or 1
LS (EP_Mode) = 0 & 1, Mode 15



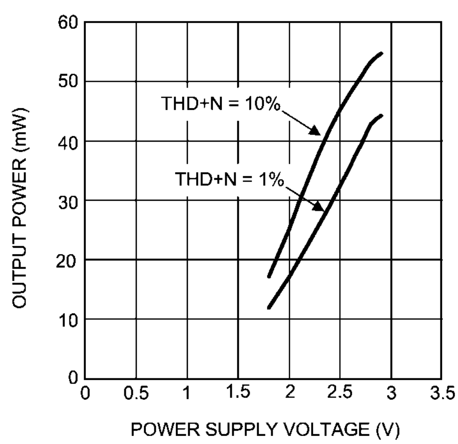
30086240

Output Power vs Supply Voltage (V_{DD}LS)
V_{DD}HP = 2.75V, R_L = 8Ω BTL,
Mode 1



30086234

Output Power vs Supply Voltage (V_{DD}HP)
V_{DD}LS = 3.3V, R_L = 32Ω SE,
Mode 4



30086233

Application Information

I²C COMPATIBLE INTERFACE

The LM49101 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM49101 and the master can communicate at clock rates up to 400kHz. Figure 2 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49101 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 3). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 4). The LM49101 device address is 11111000.

I²C INTERFACE POWER SUPPLY PIN (I²CV_{DD})

The LM49101's I²C interface is powered up through the I²CV_{DD} pin. The LM49101's I²C interface operates at a voltage level set by the I²CV_{DD} pin which can be set independent to that of the main power supply pin $V_{DD}LS$. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the $V_{DD}LS$ voltage.

I²C BUS FORMAT

The I²C bus format is shown in Figure 4. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit. R/$\overline{W}$ = 0 indicates the master is writing to the slave device, R/$\overline{W}$ = 1 indicates the master wants to read data from the slave device. Set R/$\overline{W}$ = 0; the LM49101 is a WRITE-ONLY device and will not respond to the R/$\overline{W}$ = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM49101 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM49101 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

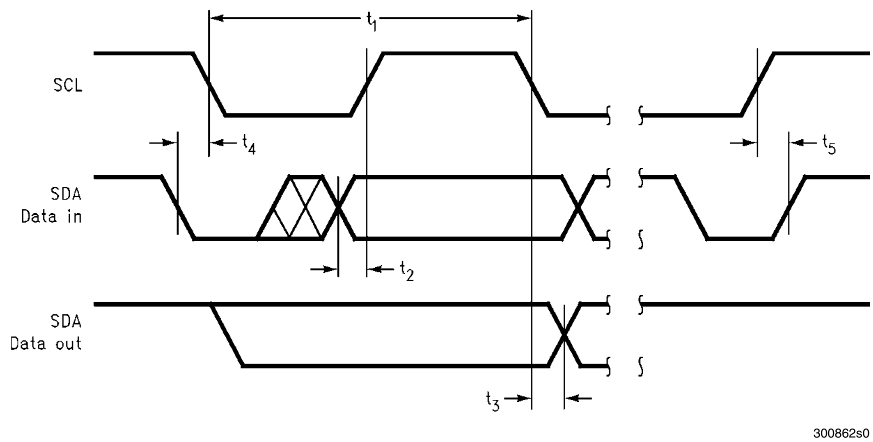


FIGURE 2. I²C Timing Diagram

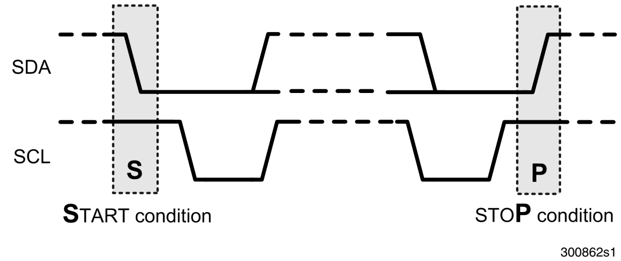


FIGURE 3. Start and Stop Diagram

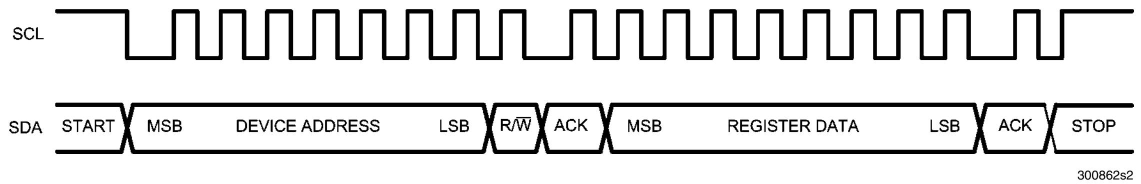


FIGURE 4. Start and Stop Diagram

TABLE 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	0	0

TABLE 2. Control Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
General Control	0	0	1	GAMP_SD (1)	LS (EP_Mode) (2)	0	Turn_On _Time (3)	Power_On (4)
Output Mode Control	0	1	EP Bypass (5)	HPR_SD (6)	Mode_ Control (7)			
Output Gain Control	1	0	0	Input_Mute (8)	LS_Gain (9)	HP_Gain (10)		
Mono Input Volume Control	1	0	1	Mono_Vol (11)				
Left Input Volume Control	1	1	0	Left_Vol (11)				
Right Input Volume Control	1	1	1	Right_Vol (11)				

Notes: All registers default to 0 on initial power-up.

1. GAMP_SD: Is used to shut down gain amplifiers not in use and reduce current consumption. See Table 3.

2. LS (EP_Mode): Loudspeaker power amplifier bias current reduction. See Table 3.

3. Turn_On_Time: Reduces the turn on time for faster activation. See Table 3.

4. Power_On: Master Power on bit. See Table 3.

5. EP Bypass: Earpiece bypass mode to allow BYPASS inputs to drive speaker outputs. See Table 4

6. HPR_SD: Will shutdown one channel of the headphone amplifier. See Table 4.

7. Mode_Control: Sets the output mode. See Table 4.

8. Input Mute: Controls muting of the inputs except the BYPASS inputs. See Table 5.

9. LS_Gain: Sets the gain of the loudspeaker amplifier to 0dB or 6dB. See Table 5.

10. HP_Gain: Sets the headphone amplifier output gain. See Table 5.

11. Mono_Vol/Left_Vol/Right_Vol: Sets the input volume for Mono, Left and Right inputs. See Table 6.

TABLE 3. General Control Register

<table>
<tr><th>Bit</th><th>Name</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="4">0</td><td rowspan="4">Power_On</td><td colspan="2">This bit is a master shutdown control bit and sets the device to be on or off.</td></tr>
<tr><td>Value</td><td>Status</td></tr>
<tr><td>0</td><td>Master power off, device disable.</td></tr>
<tr><td>1</td><td>Master power on, device enable.</td></tr>
<tr><td rowspan="4">1</td><td rowspan="4">Turn_On_Time</td><td colspan="2">This bit sets the turn on time of the device.</td></tr>
<tr><td>Value</td><td>Status</td></tr>
<tr><td>0</td><td>Normal Turn-on time</td></tr>
<tr><td>1</td><td>Fast Turn-on time</td></tr>
<tr><td rowspan="4">3</td><td rowspan="4">LS (EP Mode)</td><td colspan="2">This bit enables EP Mode reducing loudspeaker output stage bias current by 500µA.</td></tr>
<tr><td>Value</td><td>Status</td></tr>
<tr><td>0</td><td>Normal loudspeaker power amplifier operation.</td></tr>
<tr><td>1</td><td>Enables EP Mode reducing loudspeaker output stage bias current by 500µA.</td></tr>
<tr><td rowspan="3">4</td><td rowspan="3">GAMP_SD</td><td colspan="2">This bit is used to reduce I_{DD} by shutting down gain amplifiers not in use.</td></tr>
<tr><td>0</td><td>Normal operation of all gain amplifiers.</td></tr>
<tr><td>1</td><td>Disables the input gain amplifiers that are not in use to reduce current from V_{DD}LS. Recommended for Output Modes 1, 2, 4, 5, 8, 10.</td></tr>
</table>

TABLE 4. Output Mode Control Register (see key below table)

<table>
<tr><th>Bits</th><th>Field</th><th colspan="6">Description</th></tr>
<tr><td rowspan="20">3:0</td><td rowspan="20">Mode_Control</td><td colspan="6">These bits determine how the input signals are mixed and routed to the outputs.</td></tr>
<tr><td colspan="2"></td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td colspan="2"></td><td colspan="2">Headphone</td><td colspan="2">Loudspeaker</td></tr>
<tr><td>$D_3D_2D_1D_0$</td><td>Mode</td><td>Left Headphone</td><td>Right Headphone</td><td colspan="2"></td></tr>
<tr><td>0000</td><td>0</td><td>SD</td><td>SD</td><td colspan="2">SD</td></tr>
<tr><td>0001</td><td>1</td><td>SD</td><td>SD</td><td colspan="2">G_M x M</td></tr>
<tr><td>0010</td><td>2</td><td>SD</td><td>SD</td><td colspan="2">2 x (G_L x L + G_R x R)</td></tr>
<tr><td>0011</td><td>3</td><td>SD</td><td>SD</td><td colspan="2">2 x (G_L x L + G_R x R)
+ G_M x M</td></tr>
<tr><td>0100</td><td>4</td><td>G_M x M/2</td><td>G_M x M/2</td><td colspan="2">SD</td></tr>
<tr><td>0101</td><td>5</td><td>G_M x M/2</td><td>G_M x M/2</td><td colspan="2">G_M x M</td></tr>
<tr><td>0110</td><td>6</td><td>G_M x M/2</td><td>G_M x M/2</td><td colspan="2">2 x (G_L x L + G_R x R)</td></tr>
<tr><td>0111</td><td>7</td><td>G_M x M/2</td><td>G_M x M/2</td><td colspan="2">2 x (G_L x L + G_R x R)
+ G_M x M</td></tr>
<tr><td>1000</td><td>8</td><td>G_L x L</td><td>G_R x R</td><td colspan="2">SD</td></tr>
<tr><td>1001</td><td>9</td><td>G_L x L</td><td>G_R x R</td><td colspan="2">G_M x M</td></tr>
<tr><td>1010</td><td>10</td><td>G_L x L</td><td>G_R x R</td><td colspan="2">2 x (G_L x L + G_R x R)</td></tr>
<tr><td>1011</td><td>11</td><td>G_L x L</td><td>G_R x R</td><td colspan="2">2 x (G_L x L + G_R x R)
+ G_M x M</td></tr>
<tr><td>1100</td><td>12</td><td>G_L x L + G_M x M/2</td><td>G_R x R + G_M x M/2</td><td colspan="2">SD</td></tr>
<tr><td>1101</td><td>13</td><td>G_L x L + G_M x M/2</td><td>G_R x R + G_M x M/2</td><td colspan="2">G_M x M</td></tr>
<tr><td>1110</td><td>14</td><td>G_L x L + G_M x M/2</td><td>G_R x R + G_M x M/2</td><td colspan="2">2 x (G_L x L + G_R x R)</td></tr>
<tr><td>1111</td><td>15</td><td>G_L x L + G_M x M/2</td><td>G_R x R + G_M x M/2</td><td colspan="2">2 x (G_L x L + G_R x R)
+ G_M x M</td></tr>
<tr><td rowspan="4">4</td><td rowspan="4">HPR_SD</td><td colspan="6">This bit sets the headphone amplifiers to normal mode or mono mode.</td></tr>
<tr><td>Value</td><td colspan="5">Status</td></tr>
<tr><td>0</td><td colspan="5">Normal stereo headphone operation.</td></tr>
<tr><td>1</td><td colspan="5">Disable right headphone output.</td></tr>
<tr><td rowspan="4">5</td><td rowspan="4">EP Bypass</td><td colspan="6">This bit is used to control the analog switch to have the BYPASS inputs drive the loudspeaker outputs.</td></tr>
<tr><td>Value</td><td colspan="5">Status</td></tr>
<tr><td>0</td><td colspan="5">Normal output mode operation with analog switch off.</td></tr>
<tr><td>1</td><td colspan="5">Loudspeaker and headphone amplifiers go into shutdown mode and Bypass (Receiver) path enable with the analog switch on.</td></tr>
</table>

M : MIN, Mono differential input
L : LIN, Left single-ended input
R : RIN, Right single-ended input
SD : Shutdown
G_M : Mono_Vol setting determined by the Mono Input Volume Control register, See Table 6.
G_L : Left_Vol setting determined by the Left Input Volume Control register, See Table 6.
G_R : Right_Vol setting determined by the Right Input Volume Control register, See Table 6.

TABLE 5. Output Gain Control Register

<table>
<tr><th>Bits</th><th>Field</th><th colspan="2">Description</th></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">HP_GAIN</td><td colspan="2">These bits set the gain of the headphone output amplifiers.</td></tr>
<tr><td>Value</td><td>Gain (dB)</td></tr>
<tr><td>000</td><td>0</td></tr>
<tr><td>001</td><td>–1.2</td></tr>
<tr><td>010</td><td>–2.5</td></tr>
<tr><td>011</td><td>–4.0</td></tr>
<tr><td>100</td><td>–6.0</td></tr>
<tr><td>101</td><td>–8.5</td></tr>
<tr><td>110</td><td>–12</td></tr>
<tr><td>111</td><td>–18</td></tr>
<tr><td rowspan="4">3</td><td rowspan="4">LS_GAIN</td><td colspan="2">This bit sets the loudspeaker output amplifier gain.</td></tr>
<tr><td>Value</td><td>Status</td></tr>
<tr><td>0</td><td>Loudspeaker output amplifier gain is set to 0dB.</td></tr>
<tr><td>1</td><td>Loudspeaker output amplifier gain is set to 6dB.</td></tr>
<tr><td rowspan="4">4</td><td rowspan="4">INPUT MUTE</td><td colspan="2">This bit will set all the inputs except the BYPASS inputs to be in Mute mode.</td></tr>
<tr><td>Value</td><td>Status</td></tr>
<tr><td>0</td><td>Normal operation of all inputs.</td></tr>
<tr><td>1</td><td>Mutes all inputs except BYPASS with over 80dB of attenuation with out adjusting the volume settings. This bit can be used to mute the inputs to eliminate noise or transients from other systems and ICs. See the section Input Mute Bit in the Application Information section for a detailed explanation.</td></tr>
</table>

TABLE 6. Input Volume Control Registers

Bits	Fields	Description		
4:0	Mono_Vol Right_Vol Left_Vol	These bits set the input volume for each input volume register listed.		
		Volume Step	Value	Gain (dB)
		1	00000	–80.0
		2	00001	–46.5
		3	00010	–40.5
		4	00011	–34.5
		5	00100	–30.0
		6	00101	–27.0
		7	00110	–24.0
		8	00111	–21.0
		9	01000	–18.0
		10	01001	–15.0
		11	01010	–13.5
		12	01011	–12.0
		13	01100	–10.5
		14	01101	–9.0
		15	01110	–7.5
		16	01111	–6.0
		17	10000	–4.5
		18	10001	–3.0
		19	10010	–1.5
		20	10011	0.0
		21	10100	1.5
		22	10101	3.0
		23	10110	4.5
		24	10111	6.0
		25	11000	7.5
		26	11001	9.0
		27	11010	10.5
		28	11011	12.0
		29	11100	13.5
		30	11101	15.0
		31	11110	16.5
		32	11111	18.0

HW RESET FUNCTION

The LM49101 can be globally reset without using the I²C controls. When the HW RESET pin is set to a logic low the LM49101 will enter into shutdown, the mode control bits of the Output Mode Control register, volume control registers and Power_On bits will be set to the default value of zero. The other bits will retain their values. The LM49101 cannot be activated until the HW RESET pin is set to a logic high voltage. When the HW RESET is set to a logic high then the I²C controls can activate and set the register control bits.

GAMP_SD BIT

The GAMP_SD bit allows for reduced power consumption. When set to '1' the gain amplifiers on unused inputs will be shutdown saving approximately 0.4mA per input in shutdown. For example, in Mode 1 only the mono inputs are in use. Setting GAMP_SD to '1' will shut down the gain amplifiers for the left and right inputs reducing current draw from the $V_{DD}LS$ supply by approximately 0.8mA. The GAMP_SD bit does not need to be set each time when changing modes as the LM49101 will automatically activate and deactivate the needed inputs based on the mode selected.

When operating with GAMP_SD set to '1', a transient may be observed on the outputs when changing modes. During power up, the LM49101 uses a start up sequence to eliminate any pops and clicks on the outputs. The volume control circuitry is powered up first followed by the other internal circuitry with the output amplifiers being powered up last. If a mode change requires a gain amplifier to turn on then a potential transient may be created that is amplified on the already active outputs. To eliminate unwanted noise on the outputs the Power_On bit should be used to turn off the LM49101 before changing modes, perform a mode change, then turn the LM49101 back on. This procedure will cause the LM49101 to follow the start up sequence.

LS (EP_MODE) BIT

The LS (EP_Mode) bit selects the amount of bias current in the loudspeaker amplifier. Setting the LS (EP_Mode) bit to a '1' will reduce the amount of current from the $V_{DD}LS$ supply by approximately 0.5mA. The THD performance of the loudspeaker amplifier will be reduced as a result of lower bias current. See the performance graphs in the Typical Performance Characteristics section above.

TURN_ON_TIME BIT

The Turn_On_Time bit determines the delay time from the Power_On bit set to '1' and the internal circuits ready. For input capacitor values up to 0.47µF the Turn_On_Time bit can be set to fast mode by setting the bit to a '1'. When the input capacitor values are larger than 0.47µF then the Turn_On_Time bit should be set to '0' for normal turn-on time and higher delay. This allows sufficient time to charge the input capacitors to the ½ $V_{DD}LS$ bias voltage.

POWER_ON BIT

The Power_On bit is the master control bit to activate or deactivate the LM49101. All registers can be loaded independent of the Power_On bit setting as long as the IC is powered correctly. Cycling the Power_On bit does not change the values of any registers nor return all bits to the default power on value of zero. The Power_On bit only determines whether the IC is on or off.

EP BYPASS BIT

The EP Bypass bit is used to set the LM49101 to earpiece mode. When this bit is set the analog switch is activated and the rest of the IC blocks except for the I²C circuitry will go into shutdown for minimal current consumption.

HPR_SD BIT

The HPR_SD bit will deactivate the right headphone output amplifier. This bit is provided to reduce power consumption when only one headphone output is needed.

MODE_CONTROL BITS

The LM49101 includes a comprehensive mixer multiplexer controlled through the I²C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49101. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. Table 4 shows how the input signals are mixed together for each possible input selection.

INPUT MUTE BIT

The Input Mute bit will mute all inputs except the Bypass inputs when set to a '1'. This allows complete and quick mute of the Mono, Left, and Right inputs without changing the Volume Control registers or HP_Gain bits. The volume and HP_Gain bits retain their values when the Input Mute is enabled or disabled.

The Input Mute bit can be used to mute all the inputs when other chips in a system, such as the baseband IC, create transients causing unwanted noise on the outputs of the LM49101. This added feature eliminates the need for power cycling the LM49101.

LS_GAIN BIT

The loudspeaker amplifier can have an additional gain of 0dB or 6dB by using the LS_Gain bit. The Mono input has 6dB of attenuation before the volume control (see Figure 1) while the Left and Right inputs do not. The LS_Gain bit is used to account for the different attenuation levels for each input and to achieve maximum output power. To obtain maximum output power on the loudspeaker outputs, the LS_Gain bit should be se to '1' for Modes 1, 5, 9, 13.

HP_GAIN BITS

The headphone outputs have an additional, single volume control set by the three HP_Gain bits in the Output Gain Control register. The HP_Gain volume setting controls the output level for both the left and the right headphone outputs.

VOLUME CONTROL BITS

The LM49101 has three independent 32-step volume controls, one for each of the inputs. The five bits of the Volume Control registers sets the volume for the specified input channel.

SHUTDOWN FUNCTION

The LM49101 features the following shutdown controls.

Bit D4 (GAMP_SD) of the GENERAL CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the I_{DD} to be minimized.

Bit D0 (Power_On) of the GENERAL CONTROL register is the global shutdown control for the entire device. Set Power_On = 0 for normal operation. Power_On = 1 overrides any other shutdown control bit.

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49101 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49101 can be used without input coupling capacitors when configured with a differential input signal.

BRIDGE CONFIGURATION EXPLAINED

By driving the load differentially through the MONO outputs, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped.

A bridge configuration, such as the one used in LM49101, also creates a second advantage over single-ended amplifiers. Since the differential outputs are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. The power dissipation of the LM49101 varies with the mode selected. The maximum power dissipation occurs in modes where all inputs and outputs are active (Modes 6, 7, 8, 9, 10, 11, 13, 14, 15). The power dissipation is dominated by the Class AB amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4^*(V_{DD})^2/(2\pi^2 R_L) \qquad (1)$$

It is critical that the maximum junction temperature (T_{JMAX}) of 150°C is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced from the free air value, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the LM49101. It is especially effective when connected to V_{DD}, GND, and the output pins. Refer to the application information on the LM49101 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM49101. The selection of a bypass capacitor, especially C_B, is dependent upon PSRR requirements, click and pop performance, system cost, and size constraints.

GROUND REFERENCED HEADPHONE AMPLIFIER

The LM49101 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor from a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49101 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49101 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

HEADPHONE & CHARGE PUMP SUPPLY VOLTAGE (V_{DD}HP & V_{DD}CP)

The headphone outputs are centered at ground by using dual supply voltages for the headphone amplifier. The positive power supply is set by the voltage on the V_{DD}HP pin while the negative supply is created with an internal charge pump. The negative supply voltage is equal in magnitude but opposite in voltage to the voltage on the V_{DD}CP pin.

INPUT CAPACITOR SELECTION

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49101. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high-pass filter is found using Equation (2) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad \text{(Hz)} \qquad (2)$$

Where the value of R_{IN} is given in the Electrical Characteristics Table as Z_{IN}.

When the LM49101 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output.

Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

CHARGE PUMP FLYING CAPACITOR (C_1)

The flying capacitor (C_1), see Figure 1, affects the load regulation and output impedance of the charge pump. A C_1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C_1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C_1 and C_{s3} dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

CHARGE PUMP HOLD CAPACITOR (C_{S3})

The value and ESR of the hold capacitor C_{s3} directly affects the ripple on V_{SS}CP. Increasing the value of C_{s3} reduces output ripple. Decreasing the ESR of C_{s3} reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

SELECTION OF INPUT RESISTORS

The Bypass_In inputs connect to the loudspeaker output through an FET switch when EP Bypass is active (see Figure 5). Because THD through this path is mainly dominated by the switch impedance variation, adding input resistors (R_3 and R_4 in Figure 5) will help reduce impedance effects resulting in improved THD. For example, a change in the switch impedance from 2Ω to 3Ω is a 67% change in impedance. If 10Ω input resistors are used then the impedance change is from 12Ω to 13Ω, only 7.7% impedance variation. The analog switch impedance is typically 2Ω to 3.4Ω. The switch impedance change is a result of heating and the increase in $R_{DS(ON)}$ of the FETs.

The value of the input resistors must be balanced against the amount of output current and the load impedance on the loudspeaker outputs. A higher value input resistor reduces the effects of switch impedance variation but also causes voltage drop and reduced power to the load on the loudspeaker outputs.

The current through the FET switch should not exceed 500mA or die heating may cause thermal shut down activation and potential IC damage.

MINIMUM POWER OPERATION

The LM49101 has several options to reduce power consumption and is designed to conserve power when possible. When a speaker only mode is selected the headphone sections are shutdown and the current drawn from the V_{DD}HP/V_{DD}CP power supply will be zero. When a headphone mode is selected the current drawn from the V_{DD}LS supply is also reduced by shutting down unused circuitry. See the various Supply Current vs Supply Voltage graphs in the Typical Performance Characteristics section.

To reduce power consumption further, the additional control bits GAMP_SD, LS (EP Mode), and HPR_SD are provided. When low power consumption is more important than the THD performance of the loudspeaker the LS (EP_mode) bit should be set to '1' saving approximately 0.5mA from the V_{DD}LS supply. The GAMP_SD bit should be set on to save approximately 0.4mA for each input shut down. For modes where only the mono input is used, up to 0.8mA can be saved from the V_{DD}LS supply. Also, the HPR_SD bit can be used to shut down the right headphone channel reducing power consumption when only one amplifier headphone output is needed.

Additionally, the supply voltages for the different V_{DD} pins (V_{DD}LS, V_{DD}HP, and V_{DD}CP) can be set to the minimum needed values to obtain the output power levels required by the design. By reducing the supply voltage the total power consumption will be reduced.

For best system efficiency, a DC-DC converter (buck) can be used to power the V_{DD}HP and V_{DD}CP voltages from the V_{DD}LS supply instead of a linear regulator. DC-DC converters achieve much higher efficiency (> 90%) than even a low dropout regulator (LDO).

Demo Board Circuit

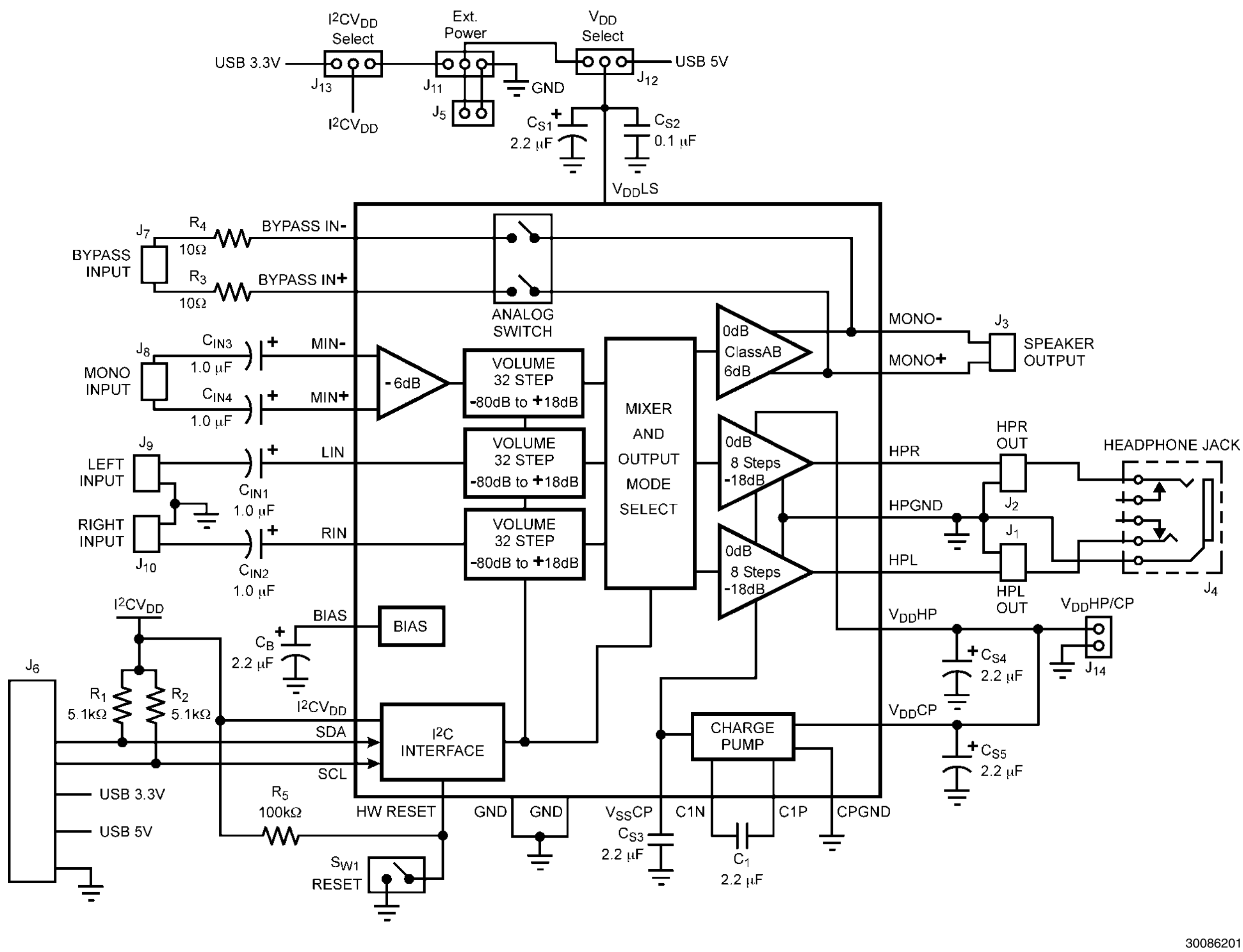


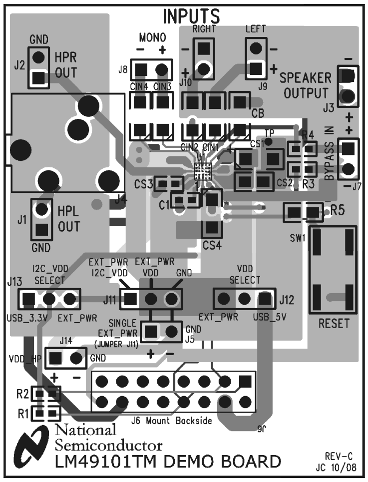
FIGURE 5. Demo Board Circuit

Demonstration Board

The demonstration board (see Figure 5) has connection and jumper options to be powered partially from the USB bus or from external power supplies. Additional options are to power the I²C logic and loudspeaker amplifier (V_{DD}LS) from a single power supply or separate power supplies. The headphone amplifier and charge pump can also be powered from the same supply as long as the voltage limits for each power supply are not exceeded, although the option is not built into the board. See the *Operating Ratings* for each supply's range limit. When powered from the USB bus the I^2CV_{DD} will be set to 3.3V and the V_{DD}LS will be set to 5V. Jumper headers J_{13} and J_{12} must be set accordingly. If a single power supply for I^2CV_{DD} and V_{DD}LS is desired then header J_5 should be used with a jumper added to header J_{11} to connect I^2CV_{DD} to the external supply voltage connected to J_5 (see Figure 5).

Connection headers J_1 and J_2 are provided along with the stereo headphone jack J_4 for easily connection and monitoring of the headphone outputs.

LM49101 microSMD Demo Board Views



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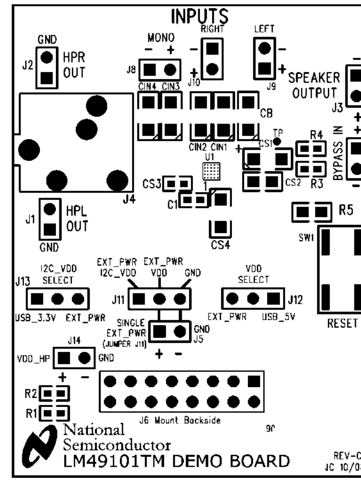
Composite View



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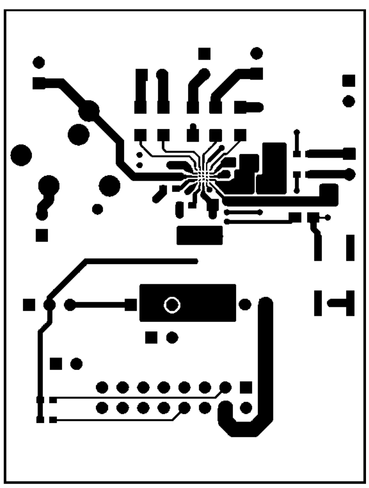
Silk Screen



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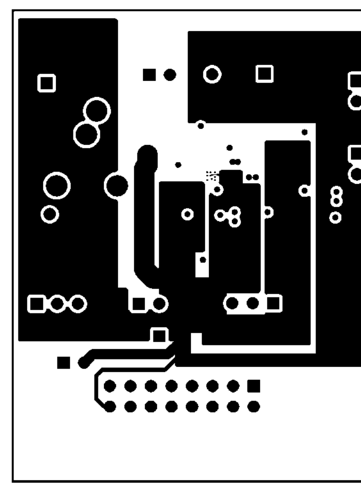
Top Layer



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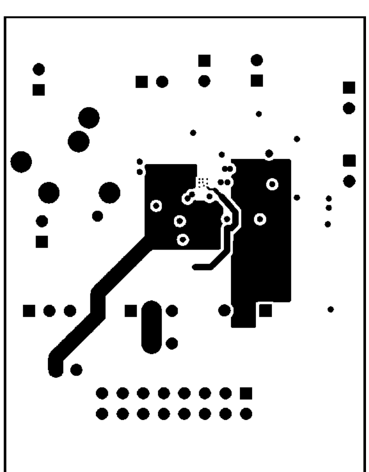
Internal Layer 1



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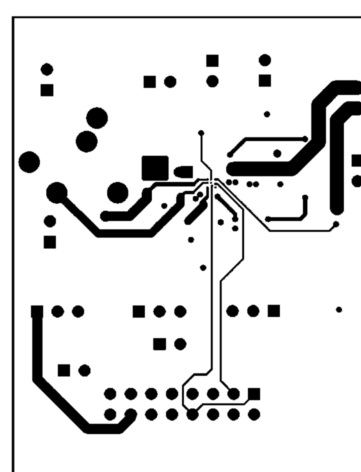
Internal Layer 2



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Bottom Layer

LM49101 Reference Demo Board Bill Of Materials

TABLE 7. Bill Of Materials

Designator	Vlaue	Tolerance	Part Description	Comment
R_1, R_2	5.1kΩ	5%	1/10W, 0603 Resistors	
R_3, R_4	10Ω	1%	1/10W, 0603 Resistors	
R_5	100kΩ	5%	1/10W, 0805 Resistor	
C_{IN1}, C_{IN2} C_{IN3}, C_{IN4}	1µF	10%	1206, X7R Ceramic Capacitor	
C_{S1}, C_{S4} C_{S5}, C_B	2.2µF	10%	Size A, Tantalum Capacitor	
C_{S2}	0.1µF	10%	0805, 16V, X7R Ceramic Capacitor	
C_{S3}, C_1	2.2µF	10%	0603, 10V, X7R Ceramic Capacitor	
U_1			LM49101TM	
J_1, J_2, J_3 J_5, J_7, J_8 J_9, J_{10}, J_{14}			0.100" 1x2 header, vertical mount	Input, Output, V_{DD}, GND
J_{11}, J_{12}, J_{13}			0.100" 1x3 header, vertical mount	V_{DD} Selects, V_{DD}, I^2CV_{DD}, GND
J_6			16 pin header	I^2C Connector
J_4			Headphone Jack	
S_{W1}			Momentary Push Switch	RESET function

PCB Layout Guidelines

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

General Mixed Signal Layout Recommendations

SINGLE-POINT POWER AND GROUND CONNECTIONS

The analog power traces should be connected to the digital traces through a single point (link). A "Pi-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. It is further recommended to put digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

PLACEMENT OF DIGITAL AND ANALOG COMPONENTS

All digital components and high-speed digital signals traces should be located as far away as possible from analog components and circuit traces.

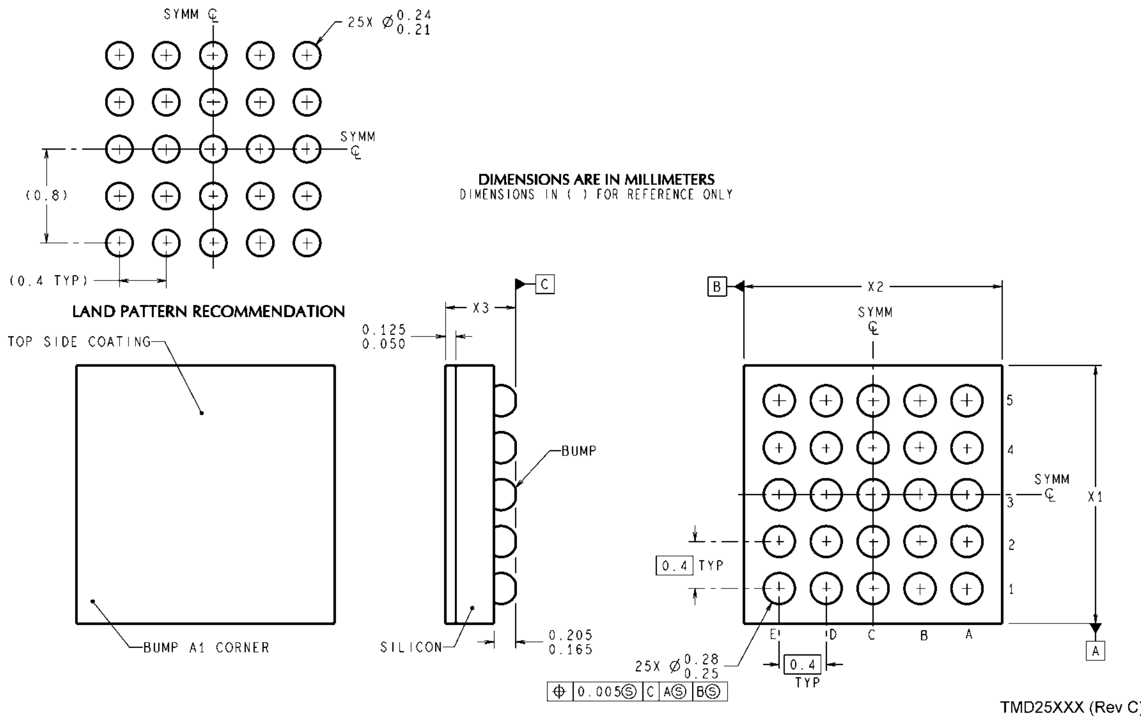
AVOIDING TYPICAL DESIGN AND LAYOUT PROBLEMS

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Revision History

Rev	Date	Description
0.01	10/18/08	Initial released.

Physical Dimensions inches (millimeters) unless otherwise noted



25 Bump micro SMD Package
NS Package Number TMD25BCA
X_1 = 2.040±0.030mm X_2 = 2.066±0.030mm, X_3 = 0.600±0.075mm

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
Wireless (PLL/VCO)	www.national.com/wireless	Analog University®	www.national.com/AU

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