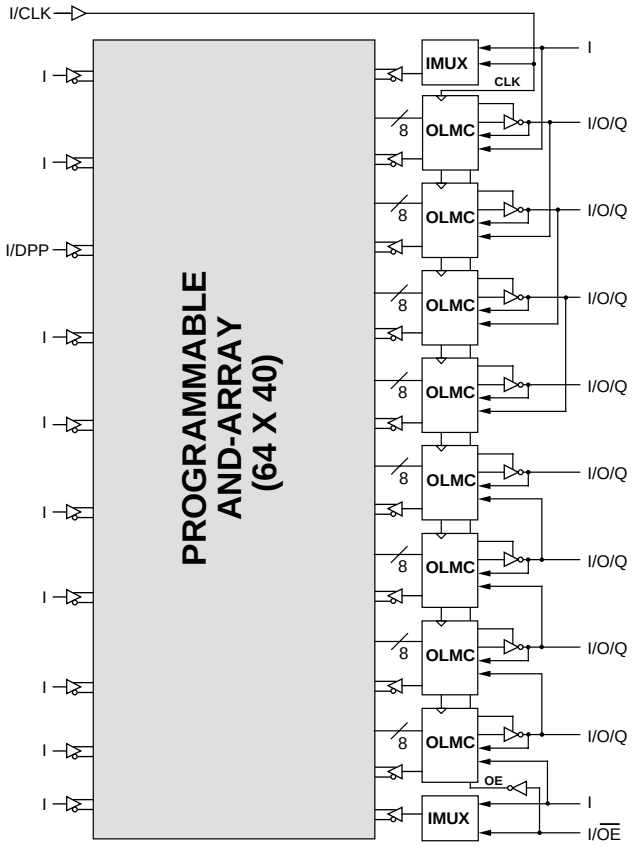
GAL20V8Z
GAL20V8ZD

Zero Power E²CMOS PLD

Features

- **ZERO POWER E²CMOS TECHNOLOGY**
  - **— 100μA Standby Current**
  - **— Input Transition Detection on GAL20V8Z**
  - **— Dedicated Power-down Pin on GAL20V8ZD**
  - **— Input and Output Latching During Power Down**
- **HIGH PERFORMANCE E²CMOS TECHNOLOGY**
  - **— 12 ns Maximum Propagation Delay**
  - **— Fmax = 83.3 MHz**
  - **— 8 ns Maximum from Clock Input to Data Output**
  - **— TTL Compatible 16 mA Output Drive**
  - **— UltraMOS® Advanced CMOS Technology**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Architecturally Similar to Standard GAL20V8**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Battery Powered Systems**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

Functional Block Diagram



Description

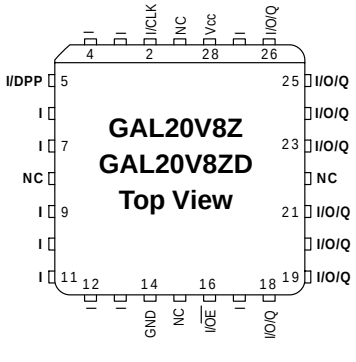
The GAL20V8Z and GAL20V8ZD, at 100 μA standby current and 12ns propagation delay provides the highest speed and lowest power combination PLD available in the market. The GAL20V8Z/ZD is manufactured using Lattice Semiconductor's advanced zero power E²CMOS process, which combines CMOS with Electrically Erasable (E²) floating gate technology.

The GAL20V8Z uses Input Transition Detection (ITD) to put the device in standby mode and is capable of emulating the full functionality of the standard GAL20V8. The GAL20V8ZD utilizes a dedicated power-down pin (DPP) to put the device in standby mode. It has 19 inputs available to the AND array.

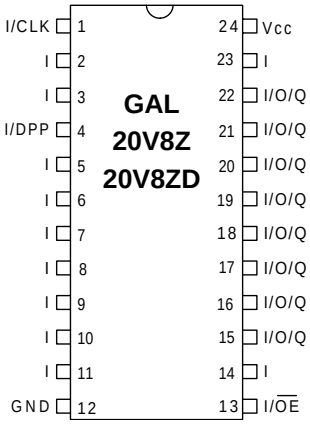
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



DIP



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GAL20V8Z/ZD Ordering Information

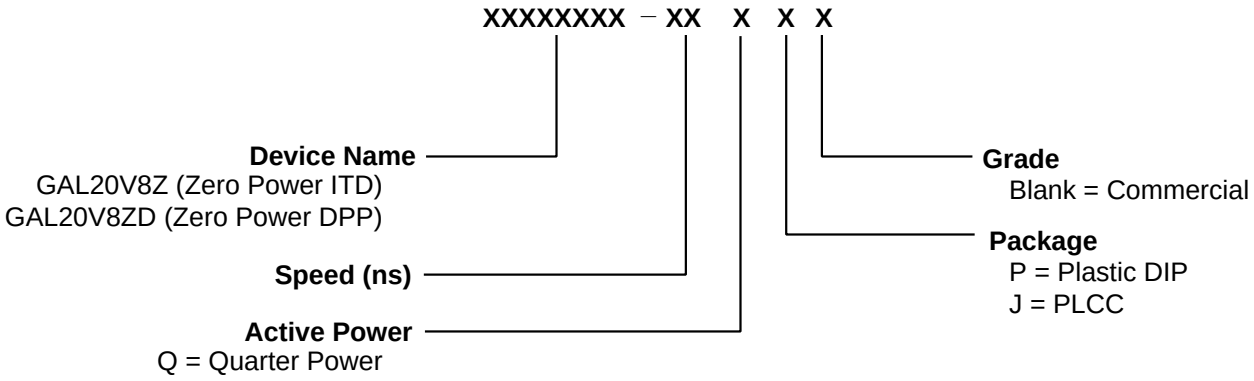
GAL20V8Z: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	ISB (μA)	Ordering #	Package
12	10	8	55	100	GAL20V8Z-12QP	24-Pin Plastic DIP
			55	100	GAL20V8Z-12QJ	28-Lead PLCC
15	15	10	55	100	GAL20V8Z-15QP	24-Pin Plastic DIP
			55	100	GAL20V8Z-15QJ	28-Lead PLCC

GAL20V8ZD: Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	ISB (μA)	Ordering #	Package
12	10	8	55	100	GAL20V8ZD-12QP	24-Pin Plastic DIP
			55	100	GAL20V8ZD-12QJ	28-Lead PLCC
15	15	10	55	100	GAL20V8ZD-15QP	24-Pin Plastic DIP
			55	100	GAL20V8ZD-15QJ	28-Lead PLCC

Part Number Description



Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL20V8Z/ZD. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode.

In **registered mode** pin 1(2) and pin 13(16) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1(2) and pin 13(16) become dedicated inputs and use the feedback paths of pin 22(26) and pin 15(18) respectively. Because of this feedback path usage, pin 22(26) and pin 15(18) do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 18(21) and 19(23)) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

When using the standard GAL20V8 JEDEC fuse pattern generated by the logic compilers for the GAL20V8ZD, special attention must be given to pin 4(5) (DPP) to make sure that it is not used as one of the functional inputs.

Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

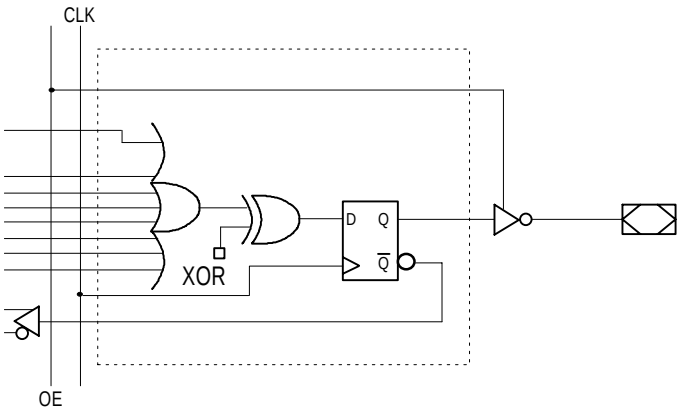
Architecture configurations available in this mode are similar to the common 20R8 and 20RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

Registered outputs have eight product terms per output. I/Os have seven product terms per output.

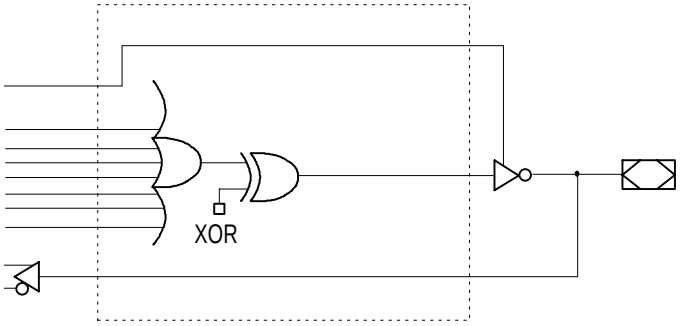
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1(2) controls common CLK for the registered outputs.
- Pin 13(16) controls common $\overline{OE}$ for the registered outputs.
- Pin 1(2) & Pin 13(16) are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



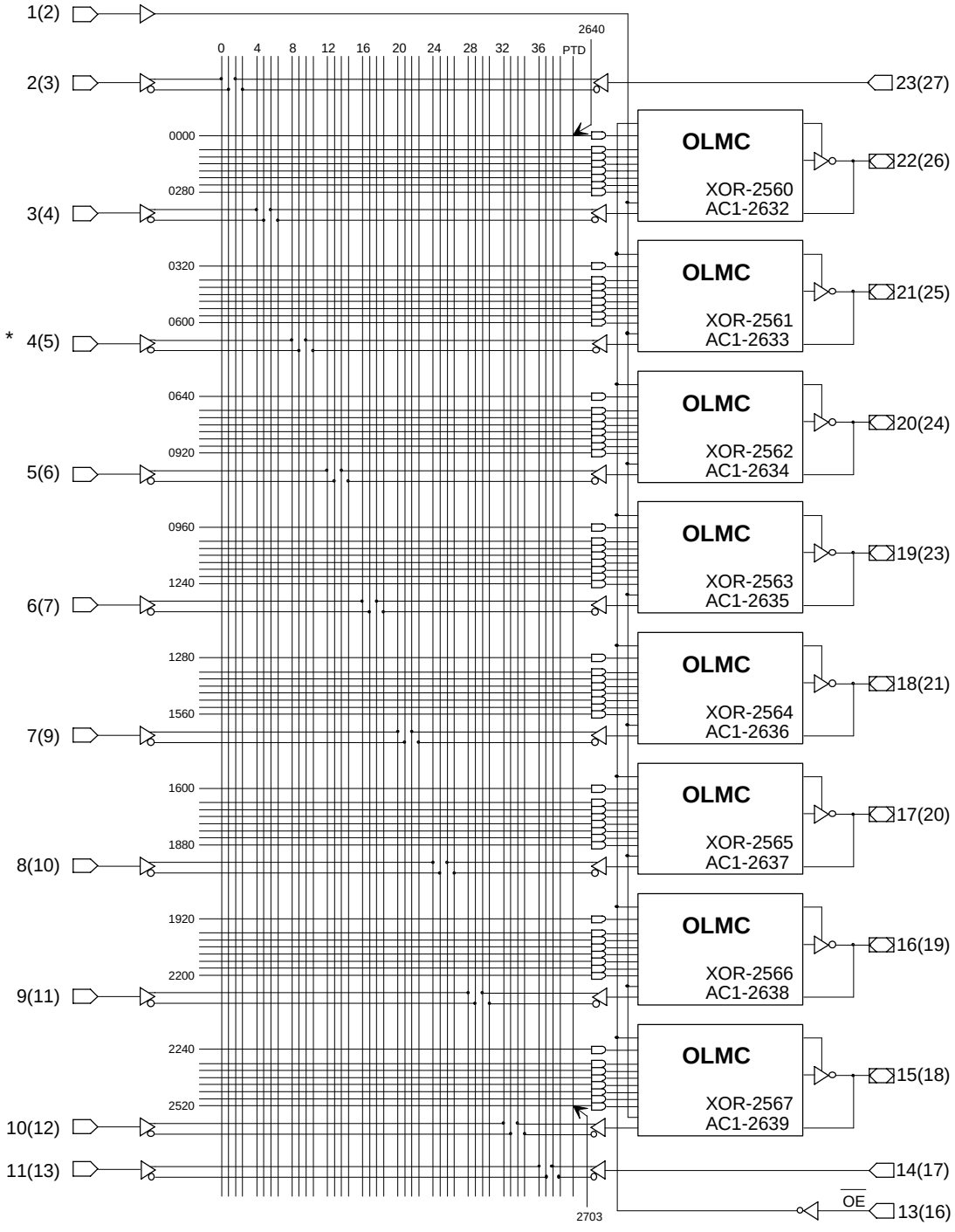
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1(2) & Pin 13(16) are permanently configured as CLK & $\overline{OE}$ for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...		.... 2630, 2631	
Byte7	Byte6	.... Byte1	Byte0

MSB LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

Complex Mode

In the Complex mode, macrocells are configured as output only or I/O functions.

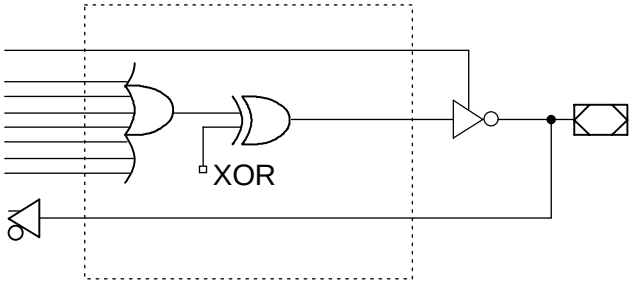
Architecture configurations available in this mode are similar to the common 20L8 and 20P8 devices with programmable polarity in each macrocell.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 15(18) & 22(26)) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1(2) and 13(16) are always available as data inputs into the AND array.

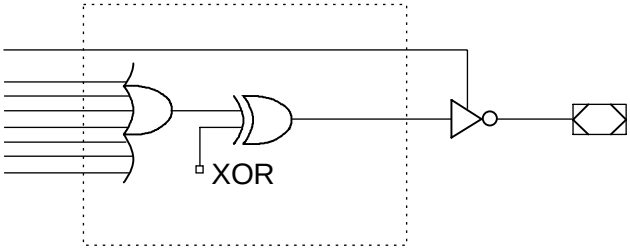
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 16(19) through Pin 21(25) are configured to this function.



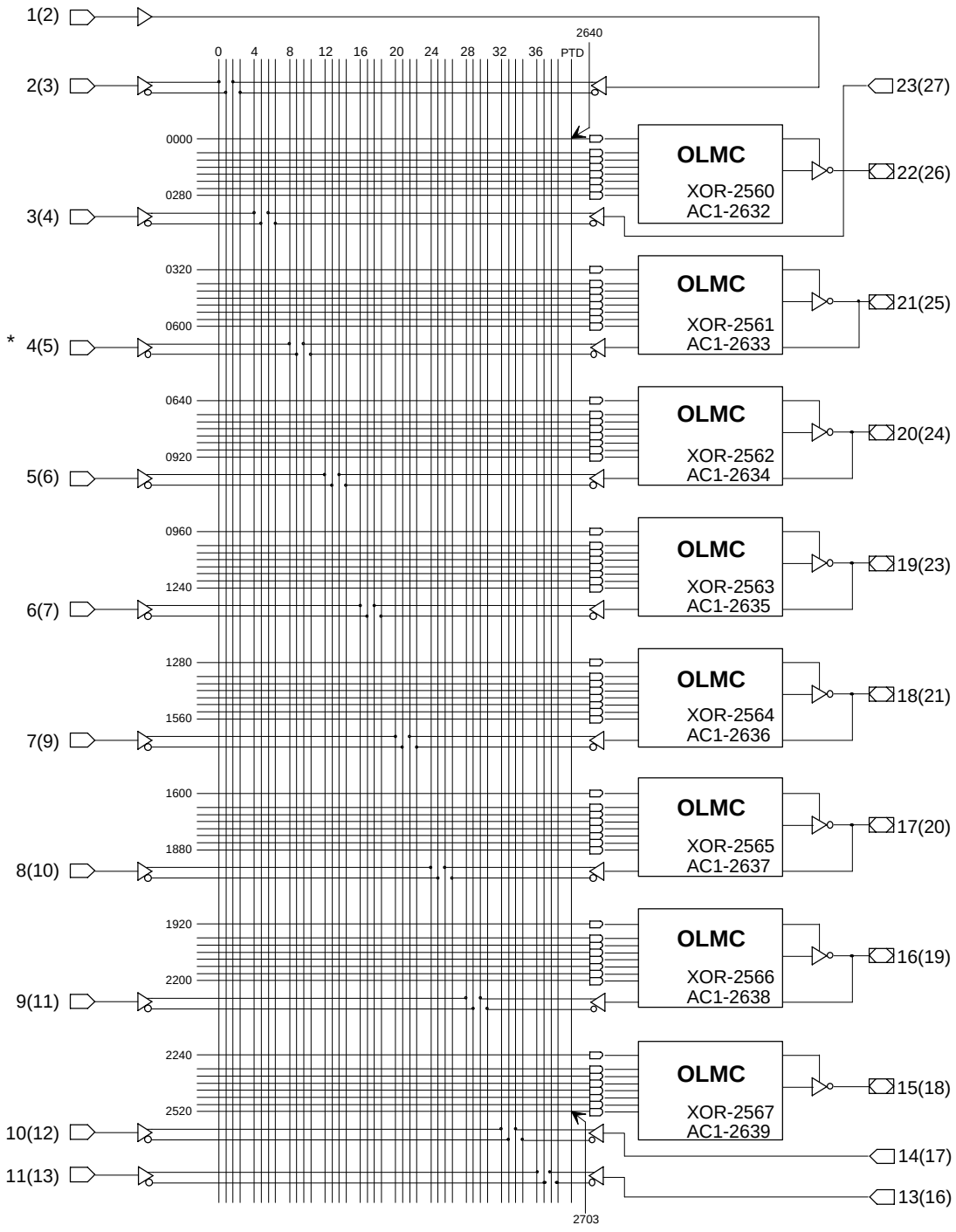
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- Pin 15(18) and Pin 22(26) are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

Simple Mode

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

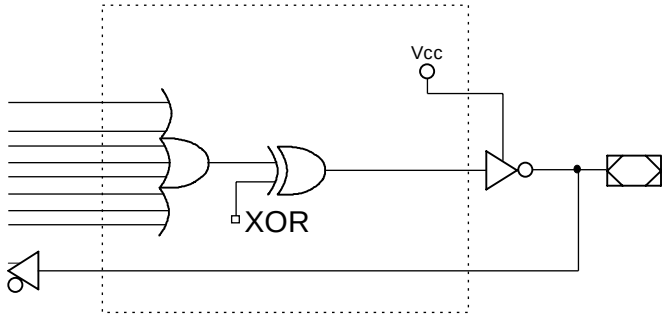
Architecture configurations available in this mode are similar to the common 14L8 and 16P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1(2) and 13(16) are always available as data inputs into the AND array. The center two macrocells (pins 18(21) & 19(23)) cannot be used in the input configuration.

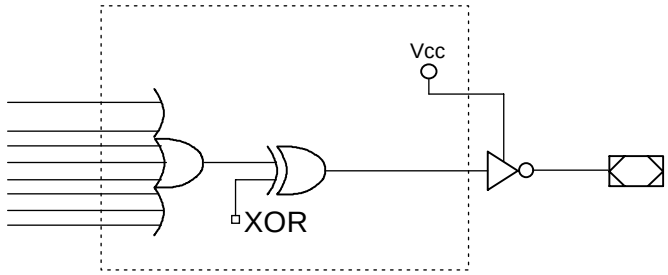
Pin 4(5) is used as dedicated power-down pin on GAL20V8ZD. It cannot be used as functional input.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



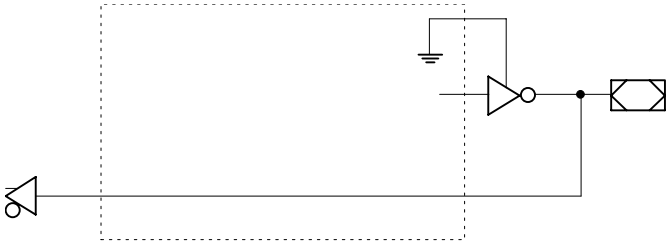
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- All OLMC **except** pins 18(21) & 19(23) can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- Pins 18(21) & 19(23) are permanently configured to this function.



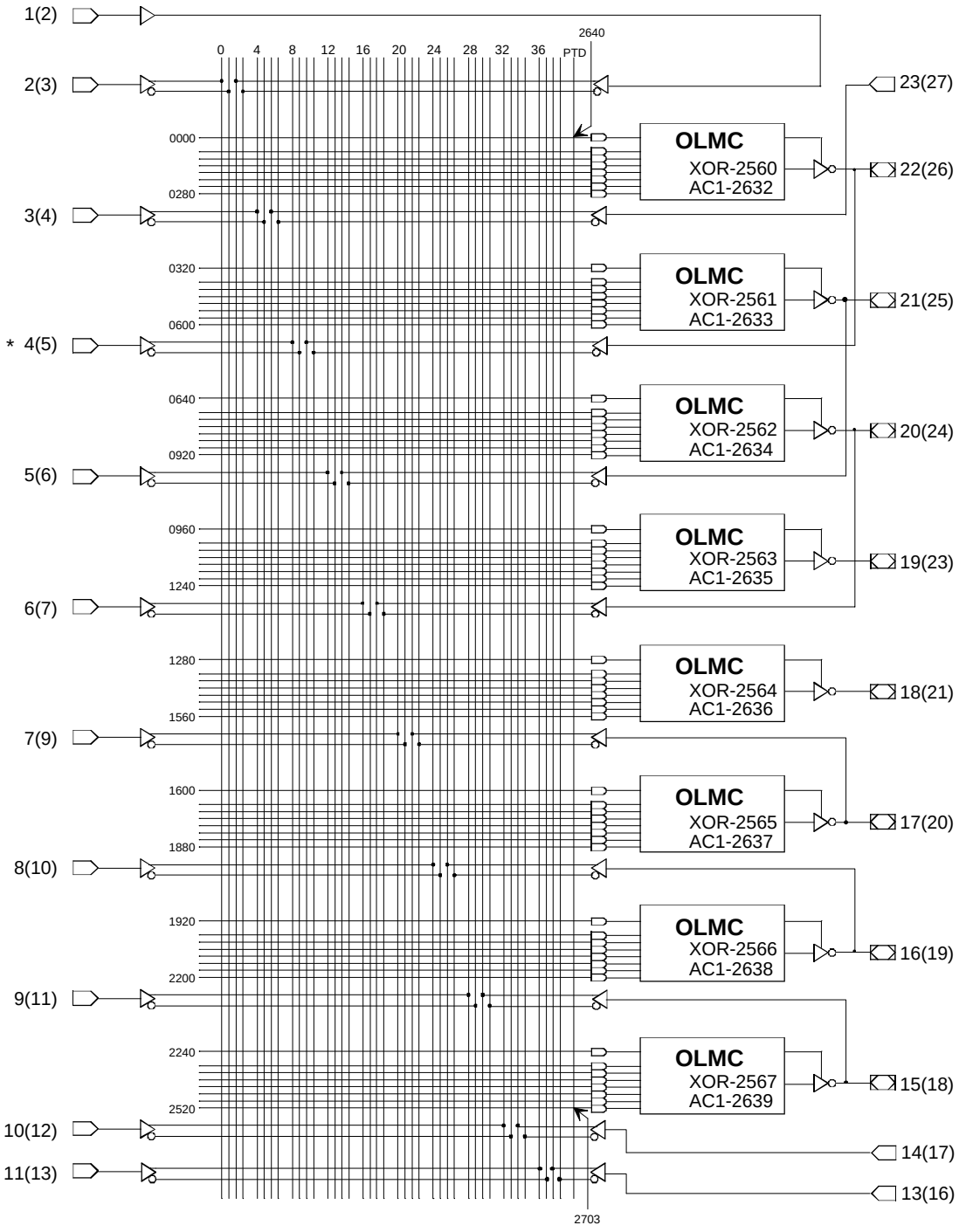
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- All OLMC **except** pins 18(21) & 19(23) can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...	.... 2630, 2631
Byte7 | Byte6	.... Byte1 | Byte0

MSB — LSB

SYN-2704
AC0-2705

* Note: Input not available on GAL20V8ZD

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
		I_{OH} = -100 µA Vin = V_{IL} or V_{IH}	Vcc-1	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	V_{IL} = GND V_{IH} = Vcc Outputs Open	Z-12/-15 ZD-12/-15	—	50	100	µA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15 MHz Outputs Open	Z-12/-15 ZD-12/-15	—	—	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

Capacitance (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested

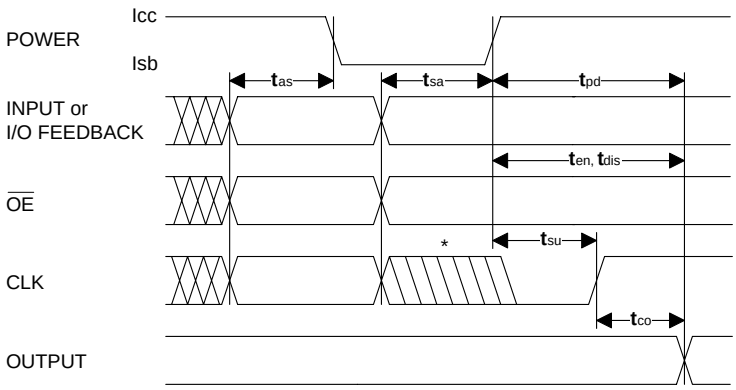
AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	3	12	3	15	ns
tco	A	Clock to Output Delay	2	8	2	10	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns
tas	—	Last Active Input to Standby	60	140	50	150	ns
tsa[4]	—	Standby to Active Output	6	13	5	15	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Specification** section.
3) Refer to **fmax Specification** section.
4) Add **t**sa to **t**pd, **t**su, **t**en and **t**dis when the device is coming out of standby state.

Standby Power Timing Waveforms



* Note: Rising clock edges are allowed during **t**sa but outputs are not guaranteed.

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
tpd	A	Input or I/O to Combinational Output	3	12	3	15	ns
tco	A	Clock to Output Delay	2	8	2	10	ns
tcf[2]	—	Clock to Feedback Delay	—	6	—	7	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
twh	—	Clock Pulse Duration, High	6	—	8	—	ns
twl	—	Clock Pulse Duration, Low	6	—	8	—	ns
ten	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Specification** section.
3) Refer to **fmax Specification** section.

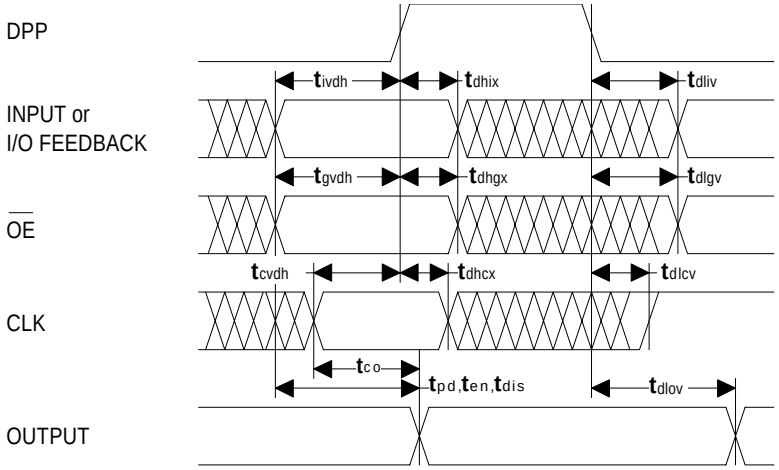
Dedicated Power-Down Pin Specifications

Over Recommended Operating Conditions

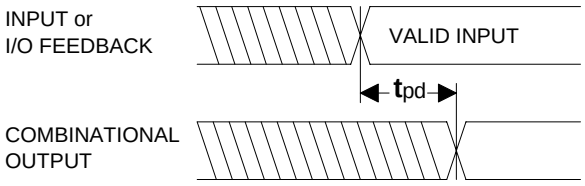
PARAMETER	TEST COND[1].	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
t_{whd}	—	DPP Pulse Duration High	12	—	15	—	ns
t_{wld}	—	DPP Pulse Duration Low	25	—	30	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	5	—	8	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	2	—	5	ns
t_{dhgx}	—	$\overline{OE}$ Don't Care after DPP High	—	6	—	9	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	8	—	11	ns
STANDBY TO ACTIVE							
t_{dliv}	—	DPP Low to Valid Input	12	—	15	—	ns
t_{dlgv}	—	DPP Low to Valid $\overline{OE}$	16	—	20	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	18	—	20	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	24	5	30	ns

1) Refer to **Switching Test Conditions** section.

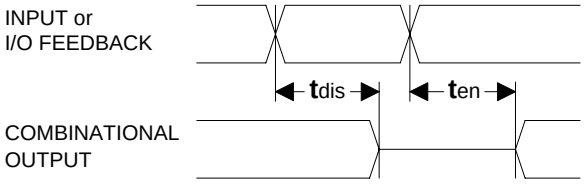
Dedicated Power-Down Pin Timing Waveforms



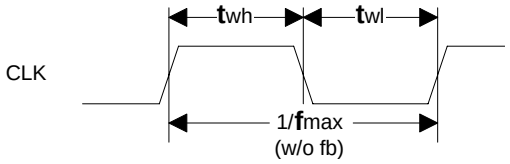
Switching Waveforms



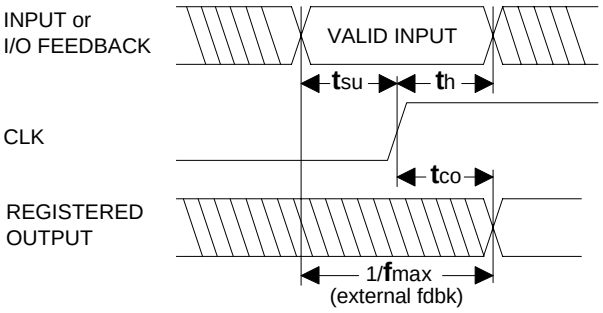
Combinatorial Output



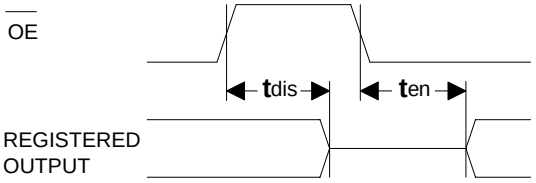
Input or I/O to Output Enable/Disable



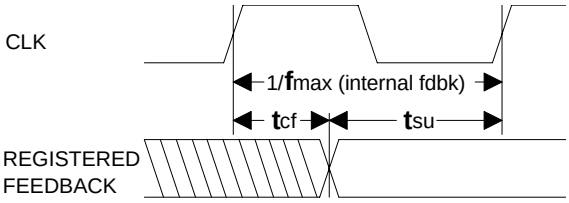
Clock Width



Registered Output

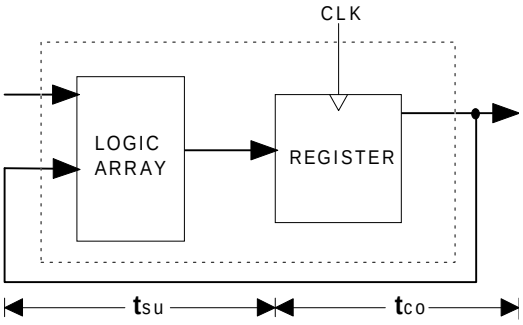


$\overline{OE}$ to Output Enable/Disable



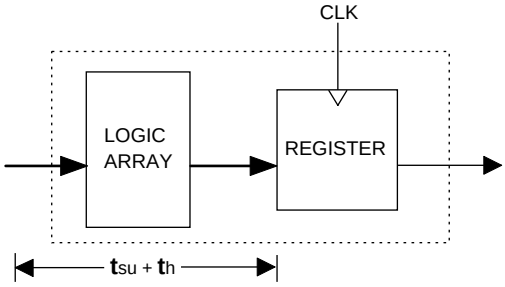
f_{max} with Feedback

fmax Specifications



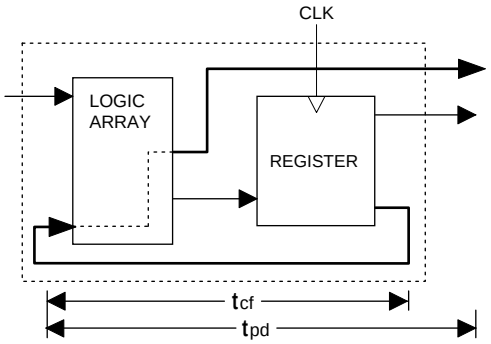
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured **t**su and **t**co.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(**t**wh + **t**wl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting **t**su from the period of fmax w/internal feedback (**t**cf = 1/**f**max - **t**su). The value of **t**cf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to **t**cf + **t**pd.

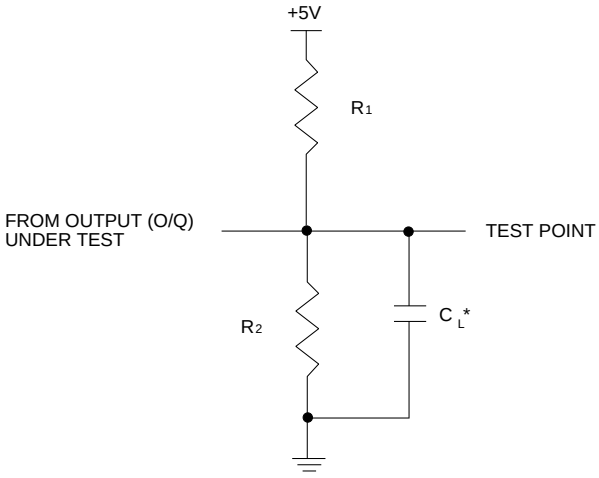
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		300Ω	390Ω	50pF
B	Active High	∞	390Ω	50pF
	Active Low	300Ω	390Ω	50pF
C	Active High	∞	390Ω	5pF
	Active Low	300Ω	390Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Electronic Signature

An electronic signature word is provided in every GAL20V8Z/ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

Security Cell

A security cell is provided in the GAL20V8Z/ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools Section of the Data Book). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Input Transition Detection (ITD)

The GAL20V8Z relies on its internal input detection circuitry to put the device in power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Any valid input transition will put the device back into active state. The first rising clock transition from power-down state only acts as a wake up signal into the device and will not clock the data input through to the output (refer to standby power timing waveform for more detail). Any input pulse widths greater than 5ns at input voltage level of 1.5V will be detected as input transition. The device will not detect any input pulse widths less than 1ns measured at input voltage level of 1.5V as input transition.

Dedicated Power-Down Pin

The GAL20V8ZD uses pin 4 (pin 5 on PLCC) as the dedicated power-down signal to put the device in power-down state. DPP is an active high signal where logic high driven on this signal puts the device into power-down state. Input pin 4 (5) cannot be used as a functional input on this device.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

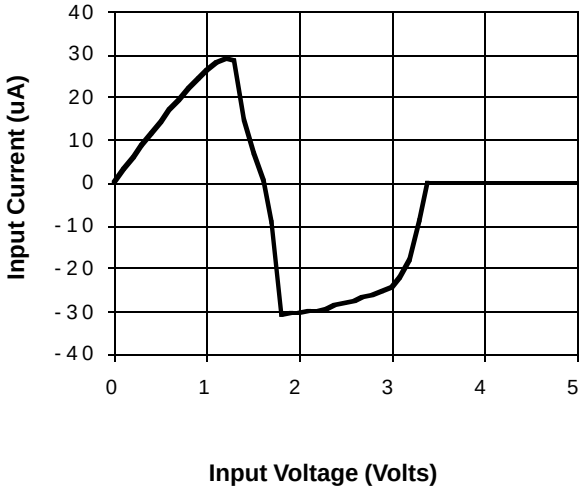
The GAL20V8Z/ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

Input Buffers

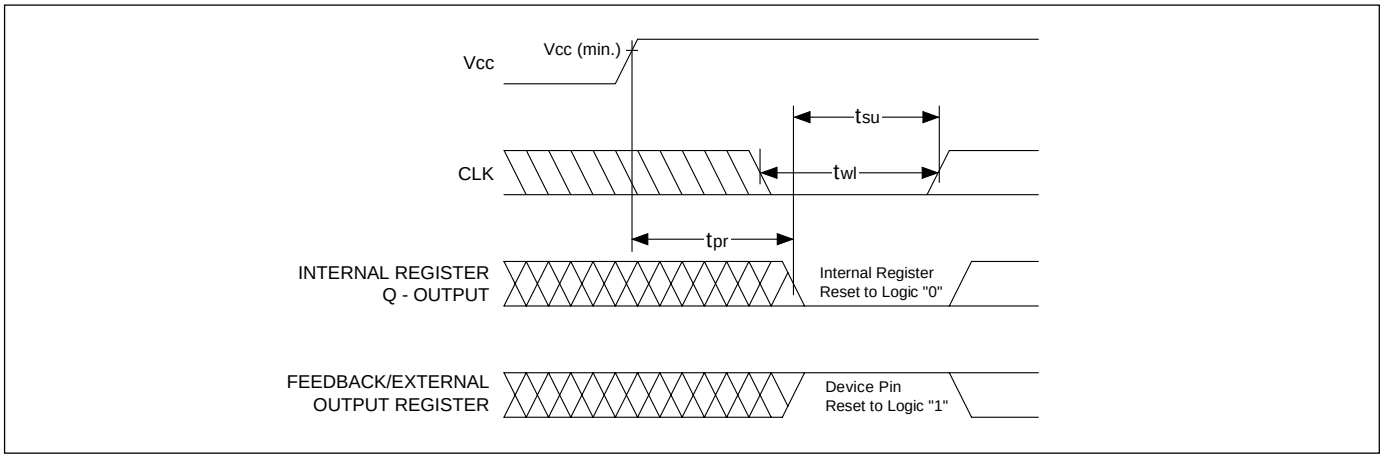
GAL20V8Z/ZD devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL20V8Z/ZD input buffers have latches within the buffers. As a result, when the device goes into standby mode the inputs will be latched to its values prior to standby. In order to overcome the input latches, they will have to be driven by an external source. Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Characteristic

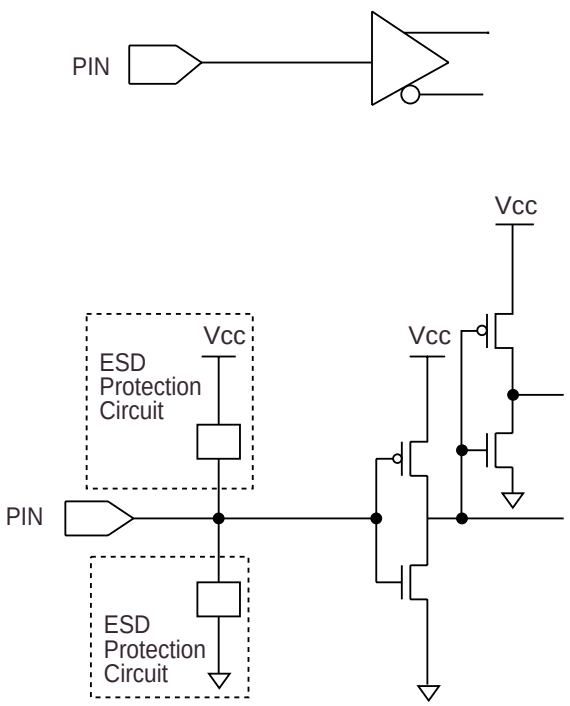


Power-Up Reset

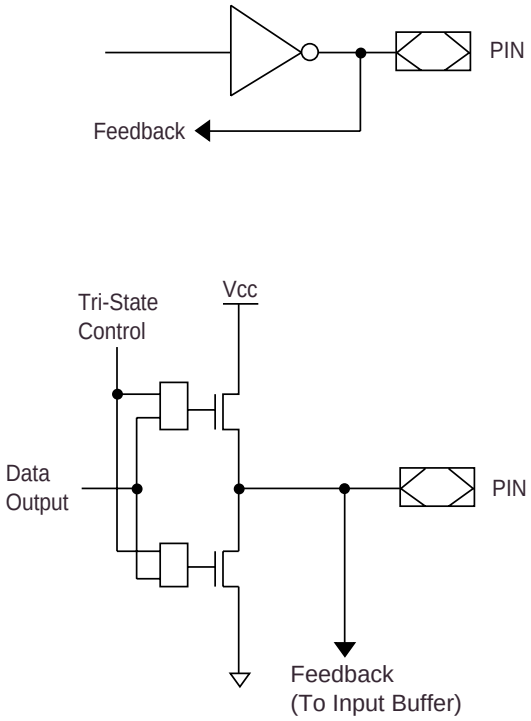


Circuitry within the GAL20V8Z/ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20V8Z/ZD. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



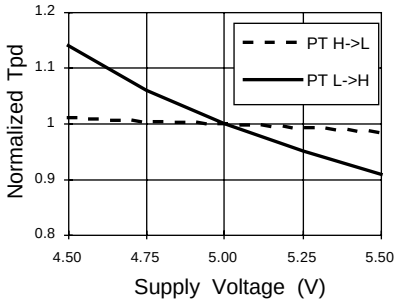
Typical Input



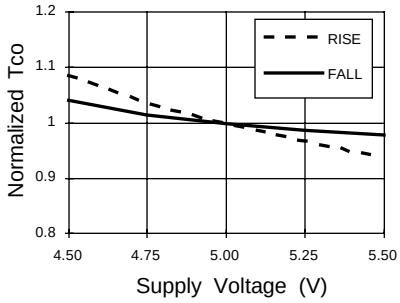
Typical Output

Typical AC and DC Characteristics

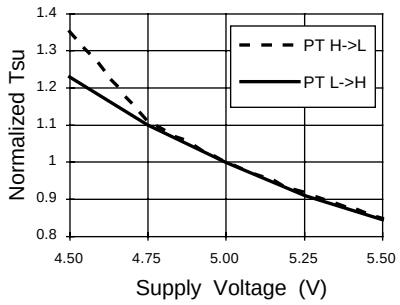
Normalized Tpd vs Vcc



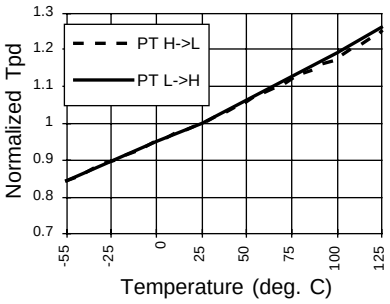
Normalized Tco vs Vcc



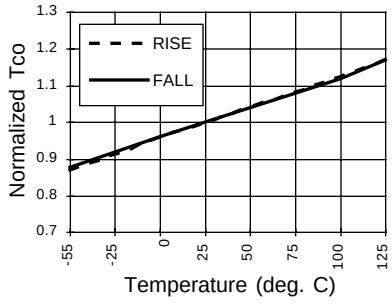
Normalized Tsu vs Vcc



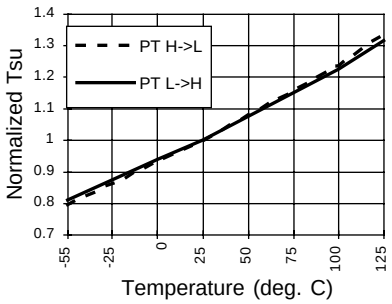
Normalized Tpd vs Temp



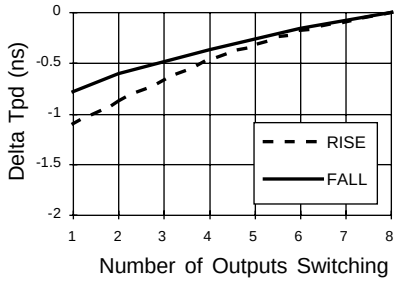
Normalized Tco vs Temp



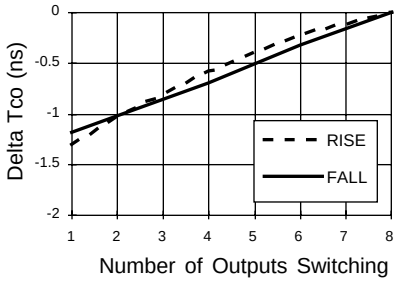
Normalized Tsu vs Temp



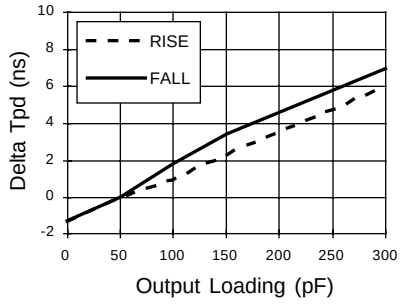
Delta Tpd vs # of Outputs Switching



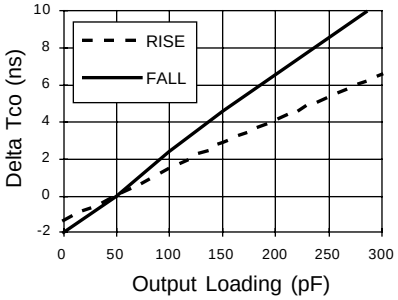
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

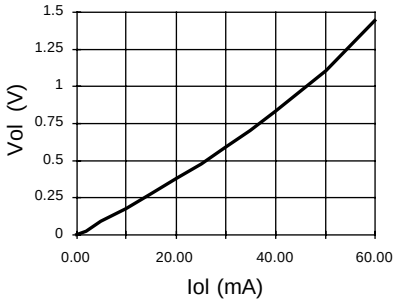


Delta Tco vs Output Loading

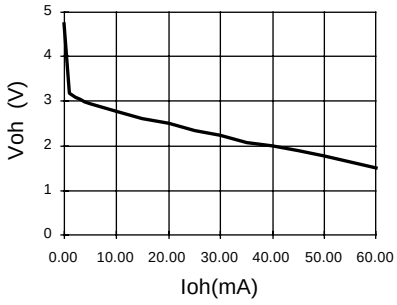


Typical AC and DC Characteristics

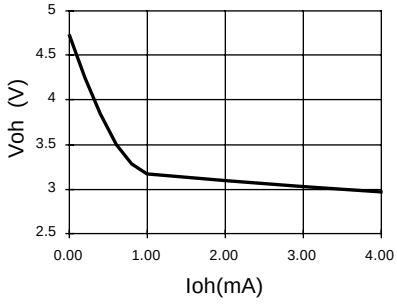
Vol vs Iol



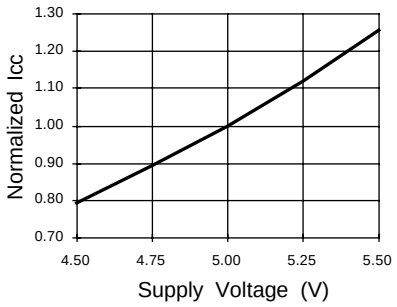
Voh vs Ioh



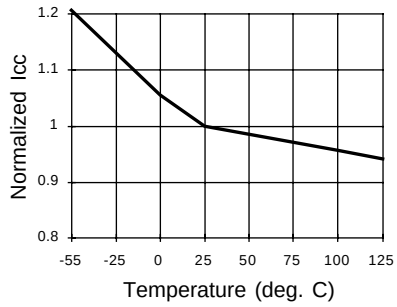
Voh vs Ioh



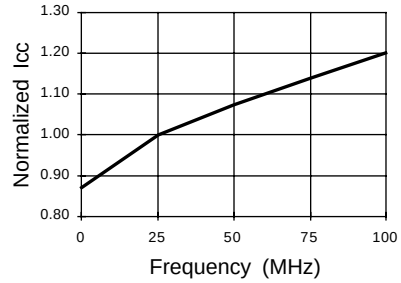
Normalized Icc vs Vcc



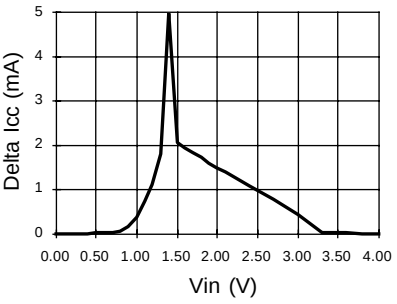
Normalized Icc vs Temp



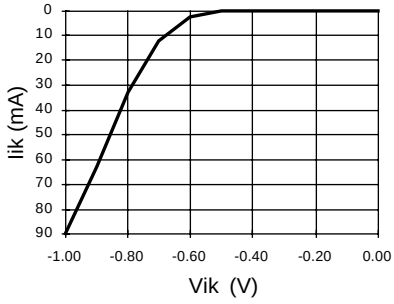
Normalized Icc vs Freq. (DPP & ITD > 10MHz)



Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)