

# SN54LS322A, SN74LS322A 8-BIT SHIFT REGISTERS WITH SIGN EXTEND

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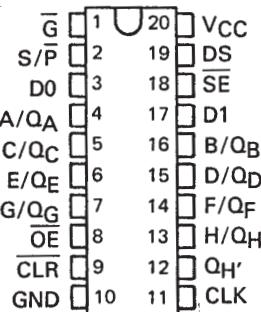
- Multiplexed Inputs/Outputs Provide Improved Bit Density
- 3-State Outputs Drive Bus Lines Directly
- Sign Extend Function
- Direct Overriding Clear

## description

These low-power Schottky eight-bit shift registers feature multiplexed input/output data ports to achieve full eight-bit data handling in a single 20-pin package. Serial data may be entered into the shift-right register through either the D0 or the D1 input as selected by the data select input. A serial output ( $Q_{H'}$ ) is also provided to facilitate expansion. Synchronous parallel loading is accomplished by taking both the register enable and the S/P inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high transition of the clock. The data extend function repeats the sign in the  $Q_A$  flip-flop during shifting. A direct overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not interfere with synchronous operation of the register.

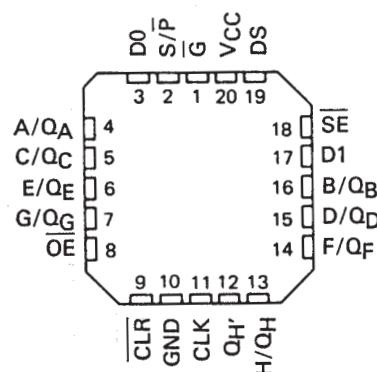
SN54LS322A . . . J OR W PACKAGE  
SN74LS322A . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS322A . . . FK PACKAGE

(TOP VIEW)



## FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT $Q_H$
	CLR	REGISTER $\bar{G}$	S/P	SIGN EXTEND $\bar{SE}$	DATA SELECT DS	OUTPUT ENABLE $\bar{OE}$	CLK	A/QA	B/QB	C/QC . . . H/QH		
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{H0}$	$Q_{H0}$
Shift Right	H	L	H	H	L	L	↑	D0	$Q_{An}$	$Q_{Bn}$	$Q_{Gn}$	$Q_{Gn}$
	H	L	H	H	H	L	↑	D1	$Q_{An}$	$Q_{Bn}$	$Q_{Gn}$	$Q_{Gn}$
Sign Extend	H	L	H	L	X	L	↑	$Q_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Gn}$	$Q_{Gn}$
Load	H	L	L	X	X	X	↑	a	b	c	h	h

When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the S/P input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

$Q_{A0} . . . Q_{H0}$  = the level of  $Q_A$  through  $Q_H$ , respectively, before the indicated steady-state conditions were established

$Q_{An} . . . Q_{Hn}$  = the level of  $Q_A$  through  $Q_H$ , respectively, before the most recent ↑ transition of the clock

D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively

a . . . h = the level of steady-state inputs at inputs A through H respectively

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

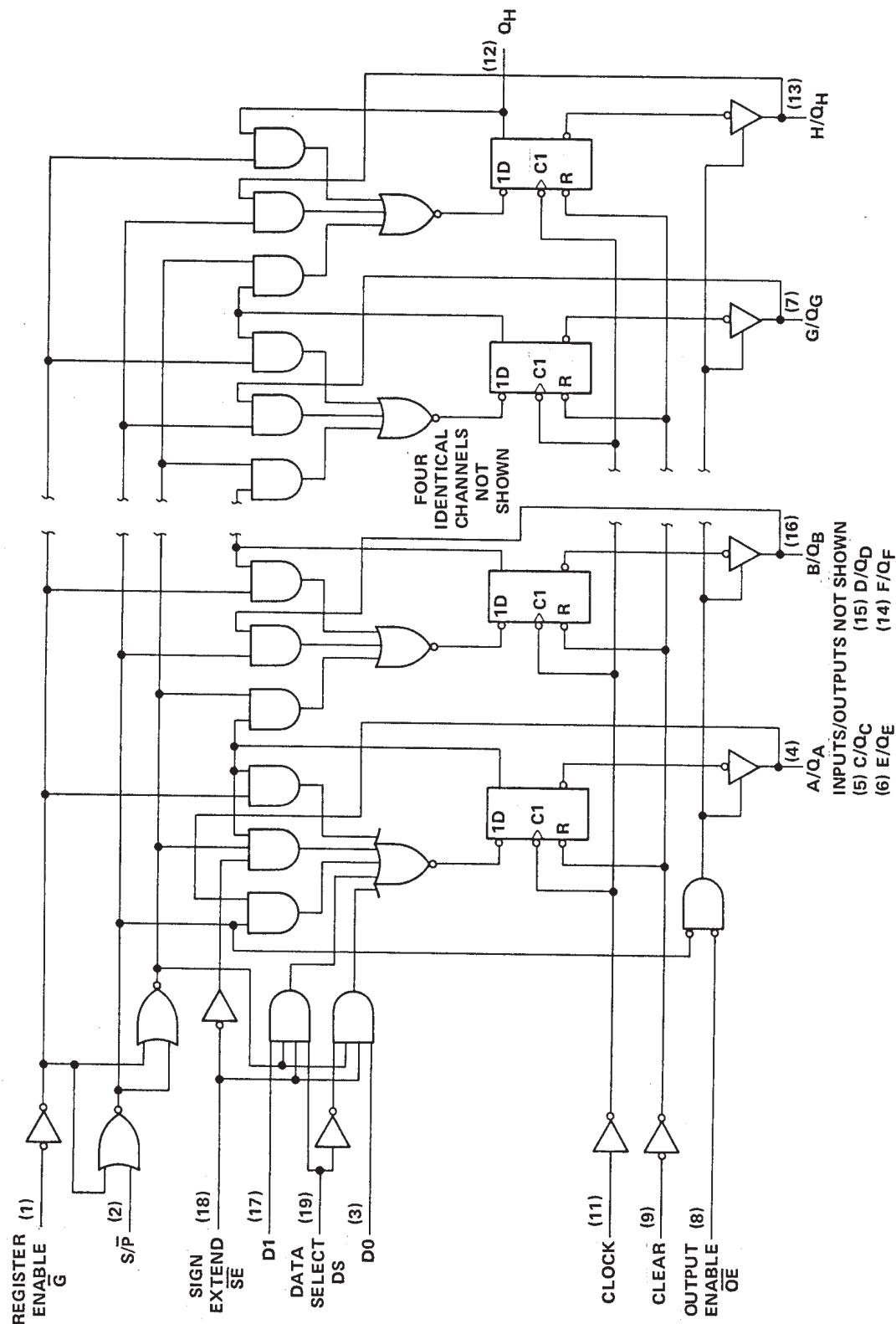
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# SN54LS322A, SN74LS322A 8-BIT SHIFT REGISTERS WITH SIGN EXTEND

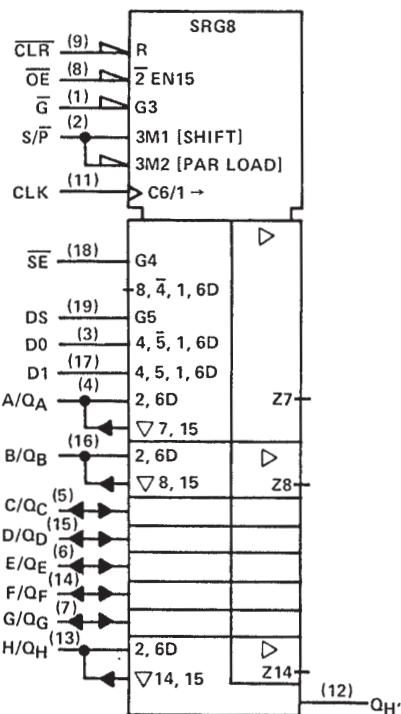
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logic diagram (positive logic)



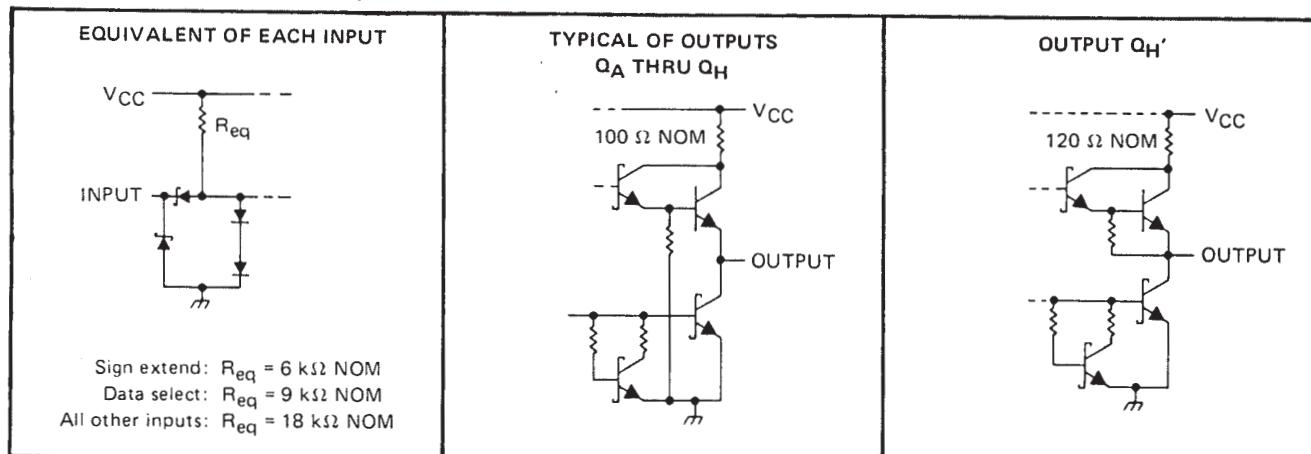
Pin numbers shown are for DW, J, N, and W packages.

logic symbol<sup>†</sup>



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

schematics of inputs and outputs



# SN54LS322A, SN74LS322A 8-BIT SHIFT REGISTERS WITH SIGN EXTEND

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54LS322A	-55°C to 125°C
SN74LS322A	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54LS322A			SN74LS322A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage		0.7			0.5		V
$I_{OH}$	High-level output current	$Q_A$ thru $Q_H$		-1	-2.6		mA	
		$Q_H'$		-0.4	-0.4			
$I_{OL}$	Low-level output current	$Q_A$ thru $Q_H$		12	24		mA	
		$Q_H'$		4	8			
$f_{clock}$	Clock frequency	0	20	0	20		MHz	
$t_{w(clock)}$	Width of clock pulse	Clock high	30	30			ns	
		Clock low	10	10				
$t_{w clear}$		Clear low	20	20			ns	
$t_{su}$	Setup time	Data select	10 $\uparrow$	10 $\uparrow$			ns	
		High-level data $\dagger$	20 $\uparrow$	20 $\uparrow$				
		Low-level data $\dagger$	20 $\uparrow$	20 $\uparrow$				
		Clear inactive-state	20 $\uparrow$	20 $\uparrow$				
		Register enable $\bar{G}$ high	35 $\uparrow$	35 $\uparrow$				
		Register enable $\bar{G}$ low	50 $\uparrow$	50 $\uparrow$				
$t_h$	Hold time	Data select	10 $\uparrow$	10 $\uparrow$			ns	
		Data $\dagger$	2 $\uparrow$	2 $\uparrow$				
		Register enable high or low	0 $\uparrow$	0 $\uparrow$				
$T_A$	Operating free-air temperature	-55	125	0	70		°C	

$\dagger$ Data includes the two serial inputs and the eight input/output data lines.

$\uparrow$ The arrow indicates that the rising edge of the clock pulse is used for reference.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>			SN54LS322A	SN74LS322A	UNIT		
				MIN	TYP <sup>‡</sup>			
VIK	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		V		
V <sub>OH</sub>	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = MAX		2.4	3.2	2.4	3.1	V
	Q <sub>H</sub> '			2.5	3.4	2.7	3.4	
V <sub>OL</sub>	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V
	Q <sub>H</sub>		I <sub>OL</sub> = 24 mA			0.35	0.5	
	Q <sub>A</sub> thru Q <sub>H</sub>		I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4	
	Q <sub>H</sub>		I <sub>OL</sub> = 8 mA			0.35	0.5	
I <sub>OZH</sub>	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.7 V		40		40		μA
I <sub>OZL</sub>	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.4 V		-0.4		-0.4		mA
I <sub>I</sub>	A thru H	V <sub>CC</sub> = MAX	V <sub>I</sub> = 5.5 V	0.1		0.1		mA
	Data select		V <sub>I</sub> = 7 V	0.2		0.2		
	Sign extend		V <sub>I</sub> = 7 V	0.3		0.3		
	Any other		V <sub>I</sub> = 7 V	0.1		0.1		
I <sub>IH</sub>	A thru H, DS	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		40		40		μA
	Sign extend			60		60		
	Any other			20		20		
I <sub>IL</sub>	Data select	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.8		-0.8		mA
	Sign extend			-1.2		-1.2		
	Any other			-0.4		-0.4		
I <sub>OS</sub> <sup>§</sup>	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.25 V (for 54LS only)		-15	-65	-30	-130	mA
	Q <sub>H</sub> '			-10	-50	-20	-100	
I <sub>CC</sub>	V <sub>CC</sub> = MAX			35	60	35	60	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

<sup>§</sup> Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER <sup>¶</sup>	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			See Note 2	20	35		MHz
t <sub>PLH</sub>	CLK	Q <sub>H</sub> '	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF, See Note 2	22	33	ns	
t <sub>PHL</sub>							
t <sub>PHL</sub>							
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 45 pF, See Note 2	16	25	ns	
t <sub>PHL</sub>							
t <sub>PHL</sub>							
t <sub>PZH</sub>	OE	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 5 pF, See Note 2	22	35	ns	
t <sub>PZL</sub>							
t <sub>PZH</sub>							
t <sub>PZL</sub>							

<sup>¶</sup>f<sub>max</sub> ≡ maximum clock frequency

t<sub>PZL</sub> ≡ output enable time to low level

t<sub>PLH</sub> ≡ propagation delay time, low-to-high-level output

t<sub>PHZ</sub> ≡ output disable time from high level

t<sub>PHL</sub> ≡ propagation delay time, high-to-low-level output

t<sub>PZL</sub> ≡ output disable time from low level

t<sub>PZH</sub> ≡ output enable time to high level

NOTE 2: For testing f<sub>max</sub>, all outputs are loaded simultaneously, each with C<sub>L</sub> and R<sub>L</sub> as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.

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