10-Bit Digital-to-Analog Converter with Two-Wire Interface

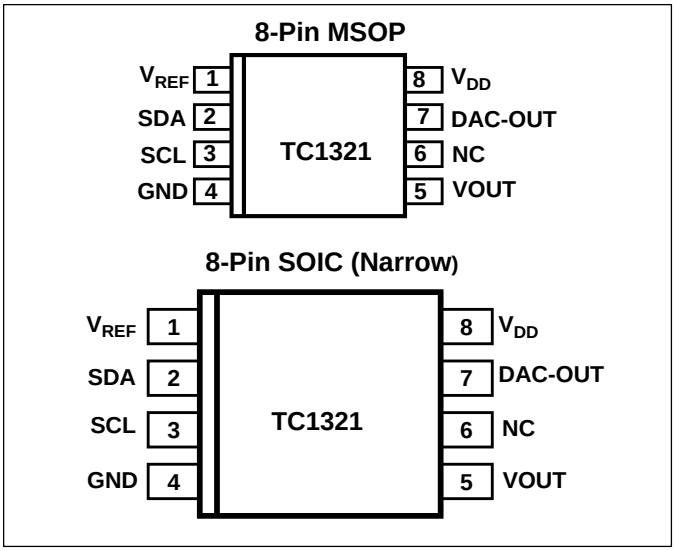
FEATURES

- **10-Bit Digital-Analog Converter**
- **8-Pin SOIC and 8-Pin MSOP Packages**
- **2.7–5.5V Single-Supply Operation**
- **Simple SMBus/I²C Serial Interface**
- **Low Power - 0.35mA Operation, 0.5µA Shutdown**
- **Monotonicity Ensured**

TYPICAL APPLICATIONS

- **Programmable Voltage Sources**
- **Digital-Controlled Amplifiers/Attenuators**
- **Process Monitoring and Control**
- **Microprocessor- controlled systems**

PIN CONFIGURATION



GENERAL DESCRIPTION

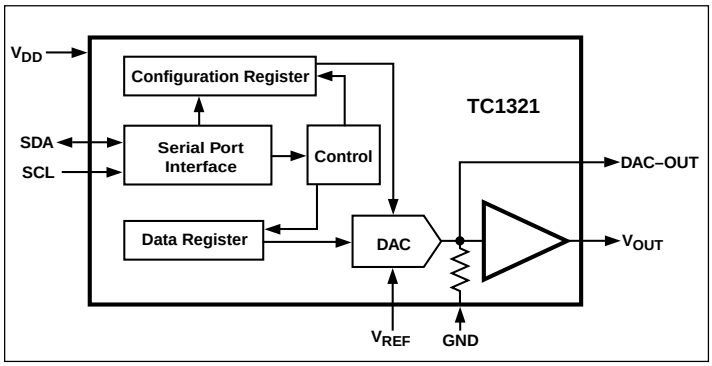
The TC1321 is a serially accessible 10-bit voltage output digital-to-analog converter (DAC). The DAC produces an output voltage that ranges from ground to an externally supplied reference voltage. It operates from a single power supply that can range from 2.7V to 5.5V, making it ideal for a wide range of applications. Built into the part is a power-on reset function that ensures that the device starts at a known condition.

Communication with the TC1321 is accomplished via a simple 2-wire SMBus/I²C™ compatible serial port with the TC1321 acting as a slave only device. The host can enable the SHDN bit in the CONFIG register to activate the low-power standby mode.

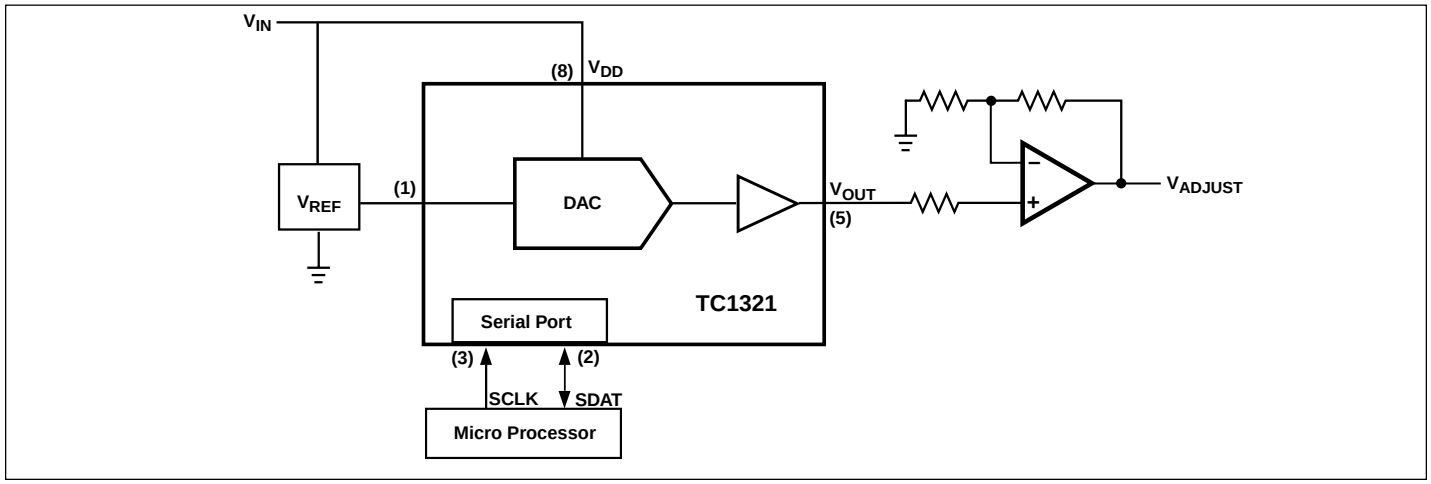
ORDERING INFORMATION

Part No.	Package	Temp. Range
TC1321EOA	8-Pin SOIC (Narrow)	–40°C to +85°C
TC1321EUA	8-Pin MSOP	–40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS DRAWING



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_{DD}) ..... +6V
Voltage On Any Pin ..... (GND – 0.3V) to (V_{DD} + 0.3V)
Operating Temperature (T_A) ..... See Below
Storage Temperature (T_{STG}) ..... – 65°C to +150°C
Current On Any Pin ..... ±50 mA
Package Thermal Resistance (θ_{JA}) ..... 330°C/W

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{DD} = 2.7V to 5.5V, – 40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply						
V_{DD}	Supply Voltage		2.7	—	5.5	V
I_{DD}	Operating Current	V_{DD} = 5.5V, V_{REF} = 1.2V Serial Port Inactive (Note 1)	—	0.35	0.5	mA
$I_{DD\text{-}STANDBY}$	Standby Supply Current	V_{DD} = 3.3V Serial Port Inactive (Note 1)	—	0.1	1	µA

STATIC PERFORMANCE–ANALOG SECTION: (V_{DD} = 2.7V to 5.5V, V_{REF} = 1.2V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Resolution		—	—	10	Bits
INL	Integral Non-Linearity at FS, T_A = +25°C	(Note 2)	—	—	±4.0	LSB
FSE	Full Scale Error		—	–	±3	%FS
DNL	Differential Non-Linearity, T_A = +25°C	All Codes (Note 2)	-1	—	+2	LSB
V_{OS}	Offset Error at V_{OUT}	(Note 2)	—	±0.3	±8	mV
TCV_{OS}	Offset Error Tempco at V_{OUT}		—	10	—	µv/°C
PSRR	Power Supply Rejection Ratio	V_{DD} at DC	—	80	—	dB
V_{REF}	Voltage Reference Range		0	—	V_{DD} – 1.2	V
I_{REF}	Reference Input Leakage Current		—	—	±1.0	µA
V_{SW}	Voltage Swing	V_{REF} ≤ (V_{DD} – 1.2V)	0	—	V_{REF}	V
R_{OUT}	Output Resistance @ V_{OUT}	R_{OUT} (ohmic)	—	5.0	—	Ω
I_{OUT}	Output Current (Source or Sink)		—	2	—	mA
I_{SC}	Output Short-Circuit Current V_{DD} = 5.5V	Source Sink	— —	30 20	50 50	mA mA

NOTES: 1. SDA and SCL must be connected to V_{DD} or GND.
2. Measured at V_{OUT} ≥ 50mV refered to GND to avoid output buffer clipping.

DYNAMIC PERFORMANCE: (V_{DD} = 2.7V to 5.5V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SR	Voltage Output Slew Rate		—	0.8	—	V/µs
t_{SETTLE}	Output Voltage Full Scale Settling Time		—	10	—	µsec
t_{WU}	Wake-up Time		—	20	—	µs
	Digital Feedthrough and Crosstalk	SDA = V_{DD}, SCL = 100kHz	—	5	—	nV-s

SERIAL PORT INTERFACE: (V_{DD} = 2.7V to 5.5V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Logic Input High		2.4	—	V_{DD}	V
V_{IL}	Logic Input Low		—	—	0.6	V
V_{OL}	SDA Output Low	I_{OL} = 3 mA (Sinking Current) I_{OL} = 6 mA	— —	— —	0.4 0.6	V V
C_{IN}	Input Capacitance SDA, SCL		—	5	—	pF
I_{LEAK}	I/O Leakage		—	—	±1.0	µA

SERIAL PORT AC TIMING: V_{DD} = 2.7V to 5.5V, –40°C ≤ (T_A = T_J) ≤ 85°C; C_L = 80pF, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{SMB}	SMBus Clock Frequency		10	—	100	kHz
t_{IDLE}	Bus Free Time Prior to New Transition		4.7	—	—	µsec
$t_{H(START)}$	Start Condition Hold Time		4.0	—	—	µsec
$t_{SU(START)}$	Start Condition Setup Time	90% SCL to 10% SDA (for repeated Start Condition)	4.7	—	—	µsec
$t_{SU(STOP)}$	Stop Condition Setup Time		4.0	—	—	µsec
t_{H-DATA}	Data In Hold Time		100	—	—	nsec
$t_{SU-DATA}$	Data In Setup Time		100	—	—	nsec
t_{LOW}	Low Clock Period	10% to 10%	4.7	—	—	µsec
t_{HIGH}	High Clock Period	90% to 90%	4	—	—	µsec
t_F	SMBus Fall Time	90% to 10%	—	—	300	nsec
t_R	SMBus Rise Time	10% to 90%	—	—	1000	nsec
t_{POR}	Power-On Reset Delay	$V_{DD} \geq V_{POR}$ (Rising Edge)	—	500	—	µsec

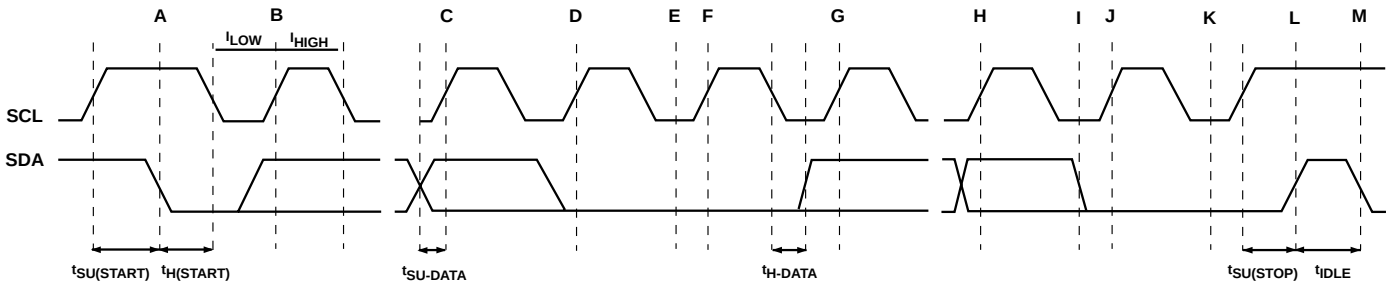
PIN DESCRIPTION

Pin No.	Symbol	Type	Description
1	V_{REF}	Input	Voltage Reference Input
2	SDA	Bi-Directional	SMBUS Serial Data
3	SCL	Input	SMBUS Serial Clock
4	GND	Input	System Ground
5	VOUT	Output	Buffered DAC Output
6	NC	None	Not Connected
7	DAC_OUT	Output	Unbuffered DAC Output
8	V_{DD}	Power	Positive Power Supply Input

TC1321

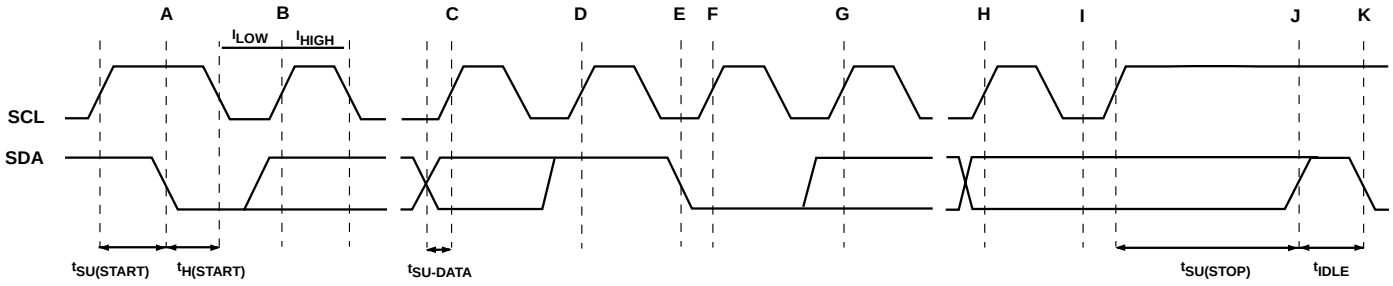
TIMING DIAGRAMS

SMBUS Write Timing Diagram



A = Start Condition
B = MSB of Address Clocked into Slave
C = LSB of Address Clocked into Slave
D = R/W Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Slave
H = LSB of Data Clocked into Slave
I = Slave Pulls SDA Line Low
J = Acknowledge Clocked into Master
K = Acknowledge Clock Pulse
L = Stop Condition, Data Executed by Slave
M = New Start Condition

SMBUS READ Timing Diagram



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E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Master
H = LSB of Data Clocked into Master
I = Acknowledge Clock Pulse
J = Stop Condition
K = New Start Condition

PIN DESCRIPTION

V_{REF}

Input. Voltage Reference Input can range from 0V to 1.2V below V_{DD}.

SDA

Bi-directional. Serial data is transferred on the SMBus in both directions using this pin. See System Management Bus Specification rev. 1.0 for timing diagrams.

SCL

Input. SMBus serial clock. Clocks data into and out of the TC1321. See System Management Bus Specification rev. 1.0 for timing diagrams.

GND

Input. Ground return for all TC1321 functions.

VOUT

Output. Buffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register. See Functional Description section.

DAC_OUT

Output. Unbuffered DAC output voltage. This voltage is a function of the reference voltage and the contents of the DATA register. However, since it is unbuffered, care must be taken that the pin is connected only to a high impedance node.

V_{DD}

Input. Positive power supply input. See electrical specifications.

DETAILED DESCRIPTION

The TC1321 is a monolithic 10-bit digital-to-analog converter that is designed to operate from a single supply that can range from 2.7V to 5.5V. The DAC consists of a data register (DATA), a configuration register (CONF), and a current output amplifier. The TC1321 uses an external reference which also determines the maximum output voltage.

The TC1321 uses a current-steering DAC based on an array of matched current sources which goes into the precision resistor that converts the contents of the Data Register and V_{REF} **into an output voltage, V_{OUT} given by:**

$$V_{OUT} = V_{REF} (DATA/ 1024)$$

Reference Input

The reference pin, V_{REF}, is a buffered high impedance input and because of this the load regulation of the reference source need only to be able to tolerate leakage levels of current (less than 1µA). V_{REF} accepts a voltage range from 0 to (V_{DD} – 1.2V). Input capacitance is typically 10 pF.

Output Amplifier

The TC1321 DAC output is buffered with an internal unity-gain rail-to-rail input/output amplifier with a typical slew rate of 0.8V/µsec. Maximum full-scale transition settling time is 10µsec to within ±1/2 LSB when loaded with 1kΩ in parallel with 100pF.

Standby Mode

The TC1321 allows the host to put it into a low power (I_{DD} = 0.5µA, typical) Standby mode. In this mode, the D/A convertion is halted. The SMBus port operates normally. Standby mode is enabled by setting the SHDN bit in the CONFIG register. The table below summarizes this operation.

Standby Mode Operation

SHDN Bit	Operating Mode
0	Normal
1	Standby

SMBus Slave Address

The TC1321 is internally programmed to have a default SMBus address value of 1001 000b. Seven other addresses are available by custom order (contact factory).

SERIAL PORT OPERATION

The Serial Clock input (SCL) and bi-directional data port (SDA) form a 2-wire bi-directional serial port for programming and interrogating the TC1321. The following conventions are used in this bus architecture:

Write 1 Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 Bits			8 Bits		8 Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Write 2 Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	DATA	ACK	P
	7 Bits			8 Bits		8 Bits		8 Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Read 1 Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	NACK	P
	7 Bits			8 Bits			7 Bits			8 Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data-flow direction.

Data Byte: reads from the register set by the command byte.

Read 2 Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	ACK	DATA	NACK	P
	7 Bits			8 Bits			7 Bits			8 Bits		8 Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data-flow direction.

Data Byte: reads from the register set by the command byte.

Receive 1 Byte Format

S	ADDRESS	RD	ACK	DATA	NACK	P
	7 Bits			8 Bits		

S = Start Condition
P = Stop Condition
Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last Read Byte or Write Byte transmission.

Receive 1 Byte Format

S	ADDRESS	RD	ACK	DATA	ACK	DATA	NACK	P
	7 Bits			8 Bits		8 Bits		

S = Start Condition
P = Stop Condition
Shaded = Slave Transmission

Data Byte: reads data from the register commanded by the last Read Byte or Write Byte transmission.

Figure 1. SMBus Protocols

TC1321 Serial Bus Conventions

TERM	EXPLANATION
Transmitter	The device sending data to the bus.
Receiver	The device receiving data from the bus.
Master	The device which controls the bus: initiating transfers (START), generating the clock, and terminating transfers. (STOP)
Slave	The device addressed by the master.
Start	A unique condition signaling the beginning of a transfer indicated by SDA falling (High –Low) while SCL is high.
Stop	A unique condition signaling the end of a transfer indicated by SDA rising (Low –High) while SCL is high.
ACK	A Receiver acknowledges the receipt of each byte with this unique condition. The Receiver drives SDA low during SCL high of the ACK clock-pulse. The Master provides the clock pulse for the ACK cycle.
Busy	Communication is not possible because the bus is in use.
NOT Busy	When the bus is idle, both SDA and SCL will remain high.
Data Valid	The state of SDA must remain stable during the High period of SCL in order for a data bit to be considered valid. SDA only changes state while SCL is low during normal data transfers. (See Start and Stop conditions.)

All transfers take place under control of a host, usually a CPU or microcontroller, acting as the Master, which provides the clock signal for all transfers. The TC1321 *always* operates as a Slave. The serial protocol is illustrated in Figure 1. All data transfers have two phases; all bytes are transferred MSB first. Accesses are initiated by a start condition (START), followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a Stop Condition (STOP). A convention called *Acknowledge* (ACK) confirms receipt of each byte. Note that SDA can change only during periods when SCL is LOW (SDA changes while SCL is HIGH are reserved for Start and Stop Conditions).

Start Condition (START)

The TC1321 continuously monitors the SDA and SCL lines for a start condition (a HIGH to LOW transition of SDA while SCL is HIGH), and will not respond until this condition is met.

Address Byte

Immediately following the Start Condition, the host must transmit the address byte to the TC1321. The 7-bit SMBus address for the TC1321 is 1001000. The 7-bit address transmitted in the serial bit stream must match for the TC1321 to respond with an Acknowledge (indicating the TC1321 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read-Write Bit. This bit is a 1 for a read operation or 0 for a write operation. During the first phase of any transfer this bit will be set = 0 to indicate that the command byte is being written.

Acknowledge (ACK)

Acknowledge (ACK) provides a positive handshake between the host and the TC1321. The host releases SDA after transmitting eight bits, then generates a ninth clock cycle to allow the TC1321 to pull the SDA line LOW to acknowledge that it successfully received the previous eight bits of data or address.

Data Byte

After a successful ACK of the address byte, the host must transmit the data byte to be written or clock out the data to be read. (See the appropriate timing diagrams.) ACK will be generated after a successful write of a data byte into the TC1321.

Stop Condition (STOP)

Communications must be terminated by a stop condition (a LOW to HIGH transition of SDA while SCL is HIGH). The Stop Condition must be communicated by the transmitter to the TC1321. NOTE: Refer to Timing Diagrams for serial bus timing.

REGISTER SET AND PROGRAMMER'S MODEL

TC1321 Command Set (SMBus READ_BYTE and WRITE_BYTE)

COMMAND BYTE DESCRIPTION		
COMMAND	**CODE**	**FUNCTION**
RWD	00h	Read/Write Data (DATA)
RWCR	01h	Read/Write Configuration (CONFIG)

Configuration Register (CONFIG), 8-BITS, READ/WRITE

CONFIGURATION REGISTER (CONFIG)							
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
RESERVED							SHDN

BIT	POR	FUNCTION	TYPE	OPERATION
D[0]	0	STANDBY switch	ReadWrite	1 = standby, 0 = normal
D[7]-D[1]	0	Reserved - Always returns zero when read.	N/A	N/A

Data Register (DATA), 10-Bits, READ/WRITE

Data Register (DATA) for 1st BYTE

D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]
MSB	X	X	X	X	X	X	X

Data Register (DATA) for 2nd BYTE

D[1]	D[0]	X	X	X	X	X	X
X	LSB	X	X	X	X	X	X

The DAC output voltage is a function of reference voltage and the binary value of the contents of the register DATA. The transfer function is given by the expression:

$$V_{OUT} = V_{REF} \times \left[\frac{DATA}{1024}\right]$$

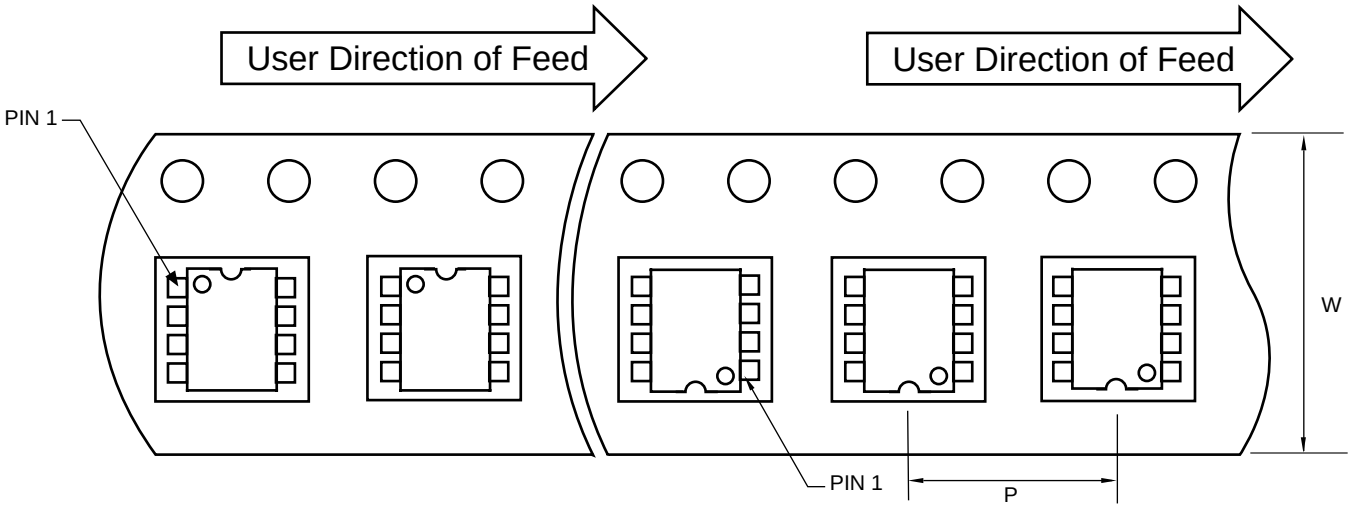
Register Set Summary

The TC1321's register set is summarized below. All registers are 10-bits wide.

NAME	DESCRIPTION	POR State	READ	WRITE
DATA	Data Register (2 BYTE format)	0000000000b*	✓	✓
CONFIG	CONFIG Register	0000 0000b	✓	✓

TAPING FORM

Component Taping Orientation for 8-Pin MSOP Devices



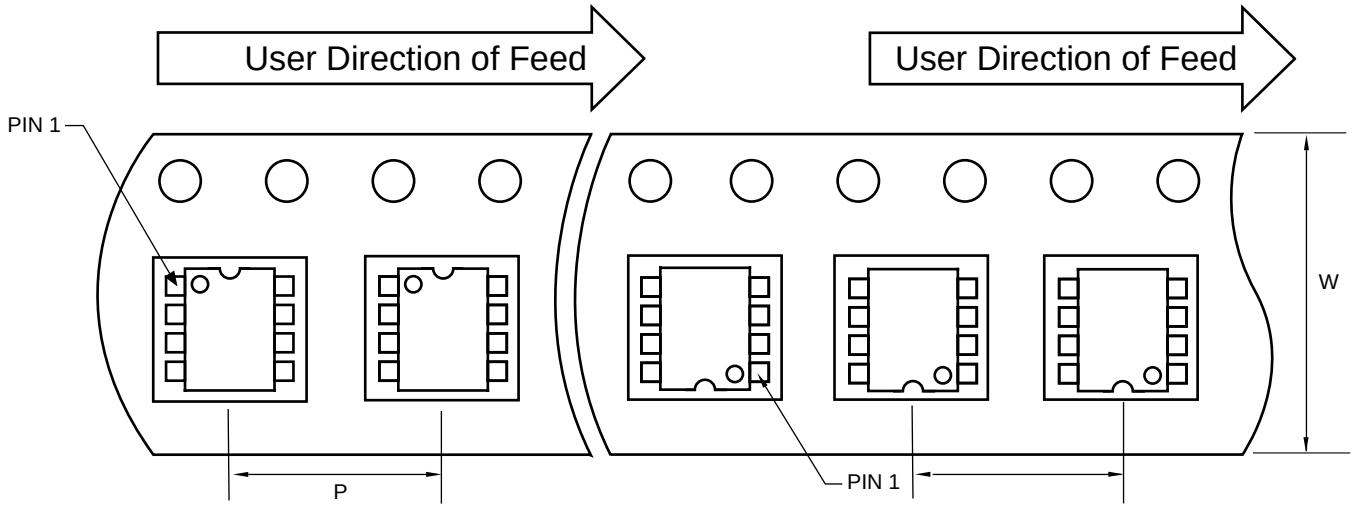
Standard Reel Component Orientation
for TR Suffix Device

Reverse Reel Component Orientation
for RT Suffix Device

Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin MSOP	12 mm	8 mm	2500	13 in

Component Taping Orientation for 8-Pin SOIC (Narrow) Devices



Standard Reel Component Orientation
for TR Suffix Device

Standard Reel Component Orientation
for RT Suffix Device

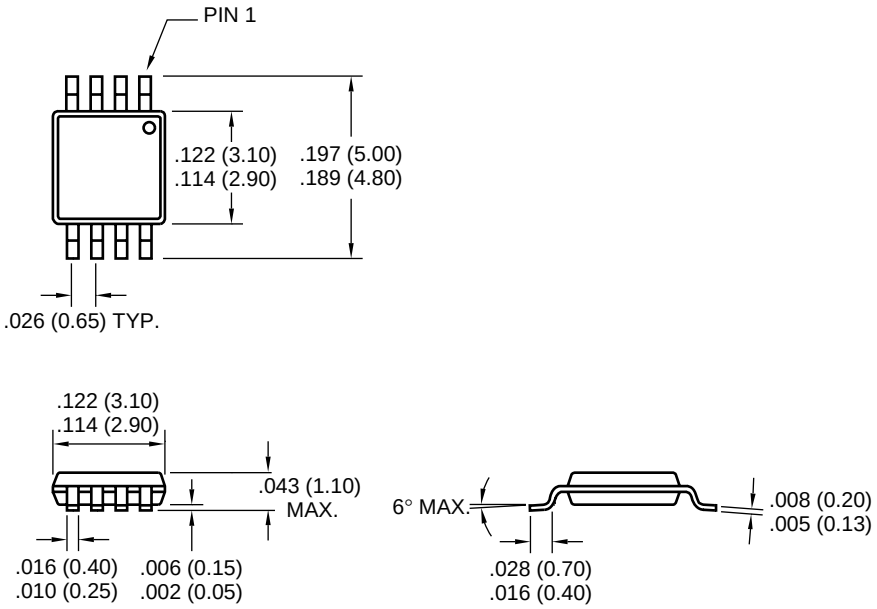
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
8-Pin SOIC (N)	12 mm	8 mm	2500	13 in

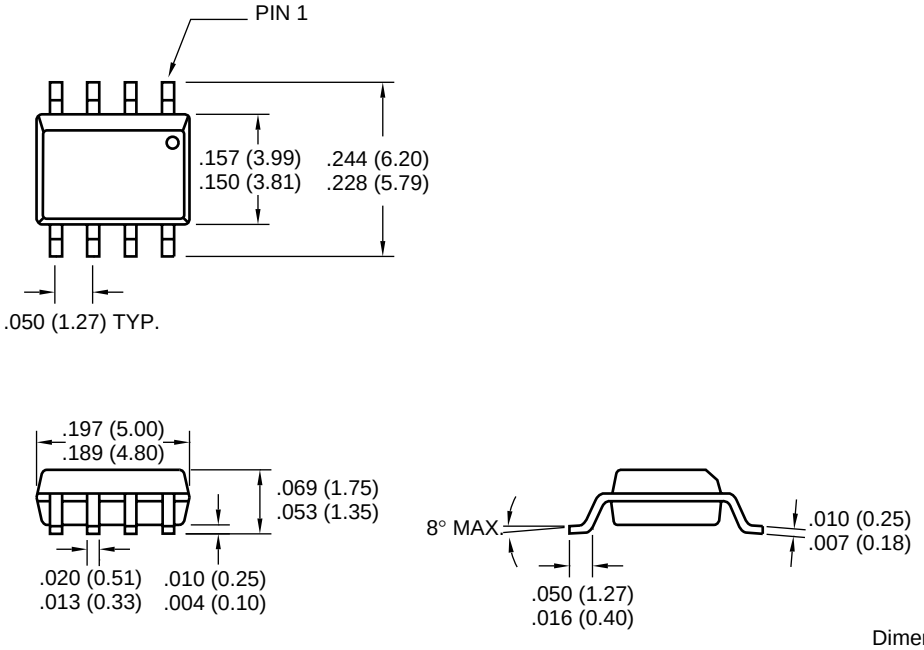
TC1321

PACKAGE DIMENSIONS

8-Pin MSOP



8-Pin SOIC (Narrow)



Dimensions: inches (mm)

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