Comlinear CLC007
Serial Digital Cable Driver

Features

- External pull-down resistors not required
- Differential inputs and outputs
- Low power dissipation
- Single +5V or -5.2V supply
- Replacement for GS9007 in most applications

General Description

The Comlinear CLC007 is a monolithic, high speed cable driver, designed to drive digital signals at data rates from DC to over 400Mbps. The CLC007 was designed to conform to the SMPTE 259M standard for transmission of serial digital video signals over 75Ω transmission lines. Rise and fall times are 650ps, minimizing the jitter induced with slowly transitioning signals. The output voltage levels are 1.6V and are set by an internal bandgap reference which is accurate and low drift. This allows 800mV swings to be realized at the end of a back-matched 75Ω cable.

National designed CLC007 to use less power than other solutions by the use of a class AB output stage which does not require any external termination resistors for output stage bias. The result is less power consumption (185mW with both outputs loaded) and less board space used. The differential inputs can be driven with a wide variety of digital signals, including ECL and DC shifted ECL as well as with input signals with substantially smaller swings than ECL. As a result, the CLC007 makes an excellent general purpose high speed driver for digital applications.

The CLC007 is available in an 8 pin SOIC package and operates from a single +5V or -5.2V supply.

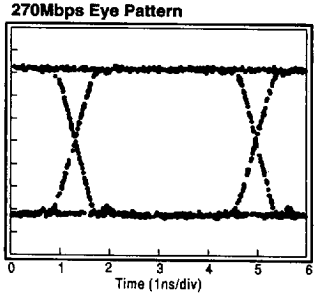
Applications

- Digital routers and distribution amplifiers
- Coaxial cable driver for digital transmission line
- Twisted pair driver
- Digital distribution amplifiers
- SMPTE, Sonet/SDH, and ATM compatible driver
- Buffer applications

Key Specifications

- 650ps rise and fall times
- Data rates <400Mbps
- 2 sets of complimentary outputs
- 200mV differential input
- Low residual jitter ($25ps_{pp}$)

270Mbps Eye Pattern



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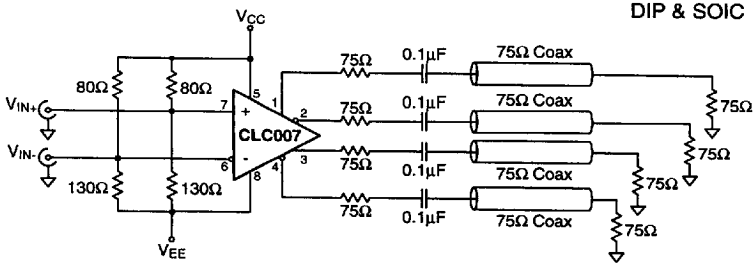
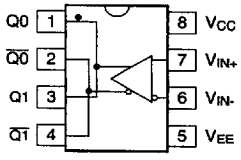
Typical Application



Pinout
DIP & SOIC



CLC007 Electrical Characteristics (V_{CC} = 0V, V_{EE} = - 5V; unless specified)

Parameters	Conditions	Typ	MIN/MAX RATINGS			Units	Notes
Ambient Temperature	CLC007AJE	+25°C	+25°C	0 to 70°C	-40 to 85°C		
STATIC DC PERFORMANCE							
supply current, loaded		39	–	–	–	mA	C, 2
supply current, unloaded		34	28/37	26/39	26/39	mA	A
output HIGH voltage	(V_{OH})	-1.7	-2.0/1.4	-2.0/1.4	-2.0/1.4	V	A
output LOW voltage	(V_{OL})	-3.3	-3.6/3.0	-3.6/3.0	-3.6/3.0	V	A
input bias current		10	30	50	50	µA	B
output swing		1.65	1.55/1.75	1.53/1.77	1.51/1.79	V	A
common mode input range upper limit		-0.7	-0.8	-0.8	-0.8	V	
common mode input range lower limit		-2.6	-2.5	-2.5	-2.5	V	
minimum differential input swing		200	200	200	200	mV	C
power supply rejection ratio		26	20	20	20	dB	A
AC PERFORMANCE							
output rise & fall time		650	425/825	400/850	400/850	ps	A, 1, 2
overshoot		5				%	C
propagation delay		1.0				ns	C
duty cycle distortion		50				ps	C
residual jitter		25	–	–	–	ps_{pp}	C
MISCELLANEOUS PERFORMANCE							
input capacitance		1.0				pF	C
output resistance		10				Ω	C
output inductance		6				nH	C

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes

A) Spec is 100% tested at +25°C, sample tested at +85°C.
B) Spec is 100% tested at +35°C at wafer probe.
C) Spec is guaranteed by design.
1) Measured between the 20% and 80% levels of the waveform.
2) Measured with both outputs driving 150Ω, AC coupled at 270Mbps.

Absolute Maximum Ratings

supply voltage	6V
output current	30mA
maximum junction temperature	+125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10sec)	+300°C
ESD rating (human body model)	1000V

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
Surface mount AJE	105°C/W	125°C/W

Reliability Information

Transistor count	72
MTTF	254Mhr

Ordering Information

Model	Temperature Range	Description
CLC007AJE	-40°C to +85°C	8-pin SOIC

Suggested Operating Range

supply voltage range (V_{CC} – V_{EE})	+4.5V to +5.5V

CLC007 OPERATION

Input Interfacing

The inputs to the CLC007 are high impedance, high gain differential inputs which are buffered with emitter followers. You need to make certain that the DC level of the inputs is between 0.8 and 2.5V below V_{CC}. Therefore, if dealing with an input signal with an 800mV swing, you need the DC bias to be between -1.2V and -2.1V. If the signal is coming to the CLC007 over any appreciable distance, (at the data rates that the CLC007 will operate at, more than about 10cm is an appreciable distance) then you will also need to have a termination to the transmission line that is carrying the signal to the inputs. Four common input schemes are shown below. Note how in Figures 2, 4 and 5 there are resistor networks which provide a Thevinin equivalent termination resistance to a bias voltage that sits within the -1.2V to -2.1V range.

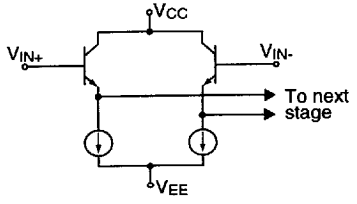


Figure 1: Input Stage

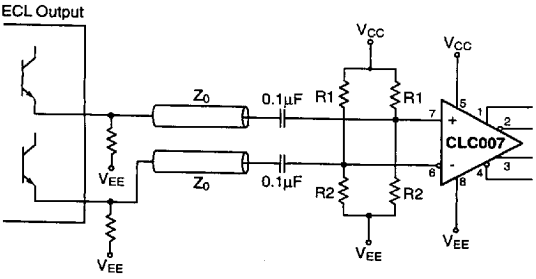


Figure 2: AC Coupled Input

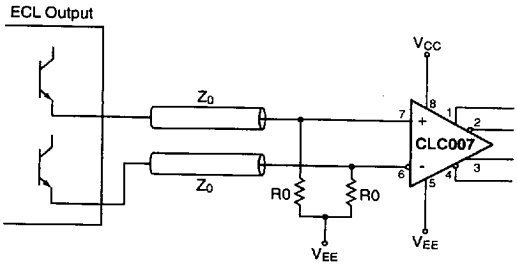


Figure 3: DC Coupled Input

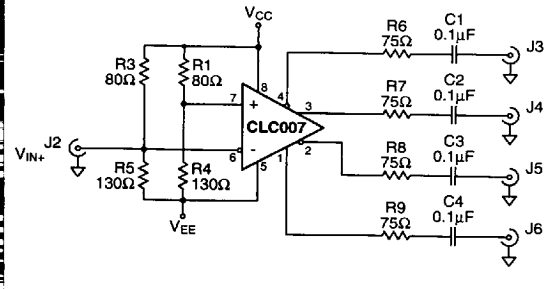


Figure 4: Single Ended 50Ω ECL Input

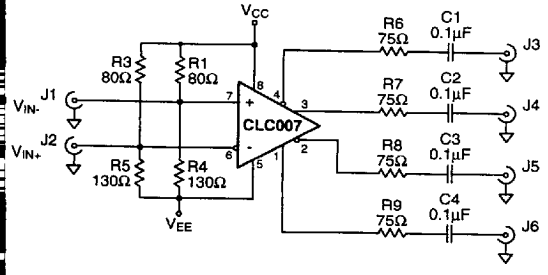


Figure 5: Differential 50Ω ECL Input

Output Interfacing

The CLC007 has a class AB output (see Figure 6). This output structure does not require any standing current in the output transistors and therefore does not need any output pull-down resistors. The advantages that this structure brings to you, are lower power dissipation, and lower system component counts. This output stage will operate properly with both AC and DC coupled outputs. The output logic levels are set with a bandgap voltage reference, and although they are compatible with 10K ECL logic after double termination, the outputs do not have the same temperature coefficients as genuine ECL logic. The result of this is that when used to drive an ECL gate, noise immunity will be decreased at the extremes of the temperature range.

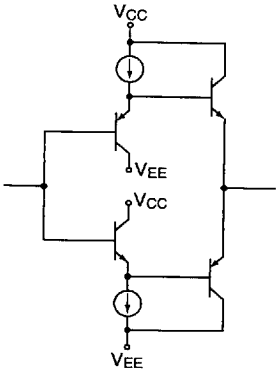


Figure 6: Output Stage

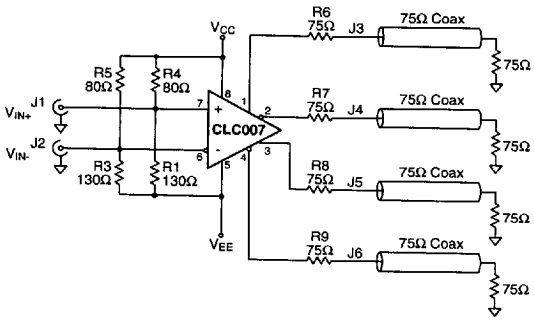


Figure 7: Differential Input DC Coupled Output

Rise and Fall Time

Rise and fall times are significantly affected by output capacitance. To maximize them eliminate stray capacitance at the output pin by placing the impedance matching resistor close to the device and keep trace lengths to a minimum. A graph showing these effects is shown in Figure 8. Test conditions were 150Ω load to ground with the capacitance in parallel.

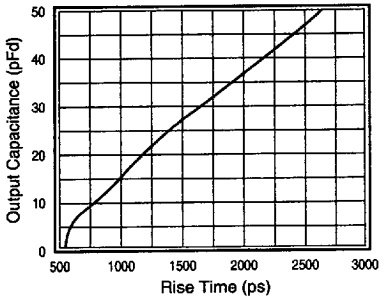


Figure 8. Rise Time vs. C_L

PCB Layout Recommendations

Printed circuit board layout affects the performance characteristics of the CLC007. The following are general guidelines for the PCB layout of the CLC007.

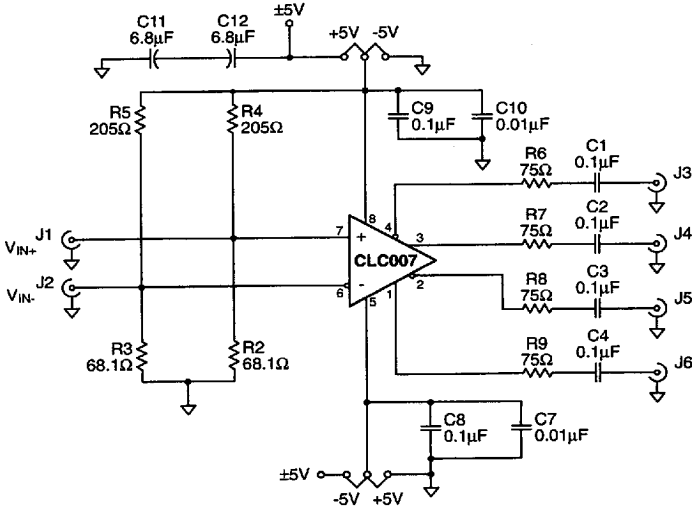
- Use a ground plane
- De-couple power pins with 0.01µF ceramic capacitors placed <0.1" from power pins. Bypass supply with 6.8µF tantalum capacitors.
- Provide short, symmetrical ground return paths for:
  - the inputs
  - the supply bypass capacitors
  - the load
- Provide a short, grounded guard trace that:
  - goes under the centerline of the package
  - is 0.1" (3mm) from the package pins
  - is on top and bottom of the printed circuit board with connecting vias
- For optimum system performance a power plane is also recommended.

Evaluation Board

An evaluation board layout and schematic are shown on the following pages. The artwork shows the board solder masks, trace layers, and ground plane. ***To order an evaluation board contact your local sales representative or National support center and request part number CLC730056.***

The evaluation board provides a guide to proper circuit layout as well as an easy means for prototyping and taking measurements. This board is designed to provide flexible circuit evaluation, thus your application may not require all parts listed in the materials list, or need different values. The evaluation board for the CLC007 is identical to that of the CLC006. Components not listed in the CLC007 evaluation data board parts list are not needed.

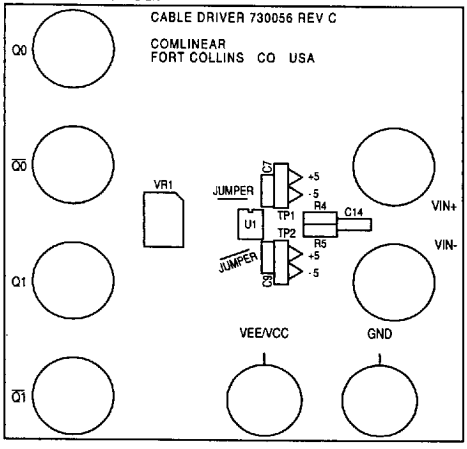
Note for ECL supply voltages install the two jumpers in the locations labeled -5V on the evaluation board. For PECL supply voltages install the two jumpers in the locations labeled +5V on the evaluation board.



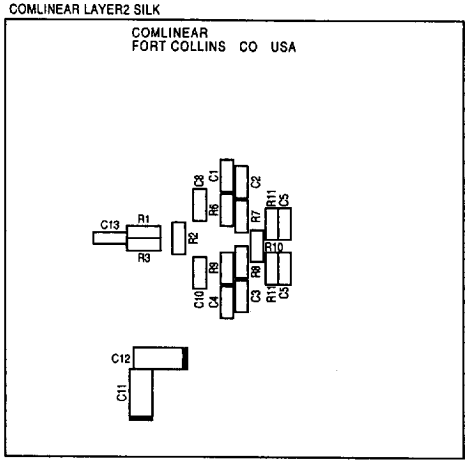
CLC007 Evaluation Board Schematic

Item	Reference Designator	Part Description	Qty
1	C1,C2,C3,C4,C8,C9	0.1µF SMD Capacitor, Size 1206	6
2	C7,C10,C13,C14	0.01µF SMD Capacitor, Size 1206	4
3	C11,C12	6.8µF SMD Tantalum Capacitor, Size 6032	2
4	J1,J2	BNC PC Amphenol #31-5329-52RFX	2
5	J3,J4,J5,J6	BNC PC Amphenol #31-5329-72RFX	4
6	R3,R1	68.1Ω SMD Resistor, Size 1206	2
7	R4,R5	205Ω SMD Resistor, Size 1206	2
8	R6,R7	75Ω SMD Resistor, Size 1206	4
9	U1	CLC007AJE Cable Driver	1
10	+5,-5	Jumper	2

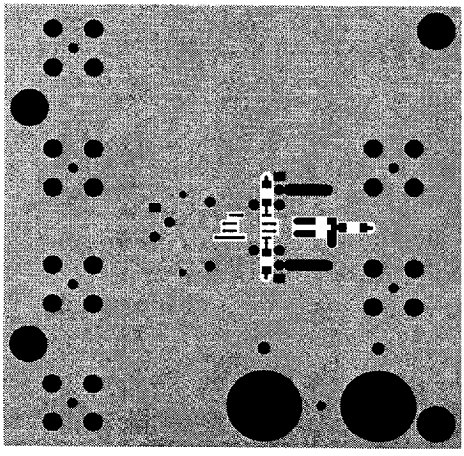
COMLINEAR LAYER1 SILK



COMLINEAR LAYER2 SILK



COMLINEAR LAYER1



COMLINEAR LAYER2