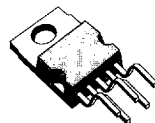


## 5V-0.5A VERY LOW DROP REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE ( $5V \pm 4\%$ ) OVER FULL TEMPERATURE RANGE ( $-40 / 125^{\circ}C$ )
- VERY LOW VOLTAGE DROP ( $0.75V_{max}$ ) OVER FULL T RANGE
- OUTPUT CURRENT UP TO 500mA
- RESET FUNCTION
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- +80V LOAD DUMP PROTECTION
- -80V LOAD DUMP PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



Pentawatt

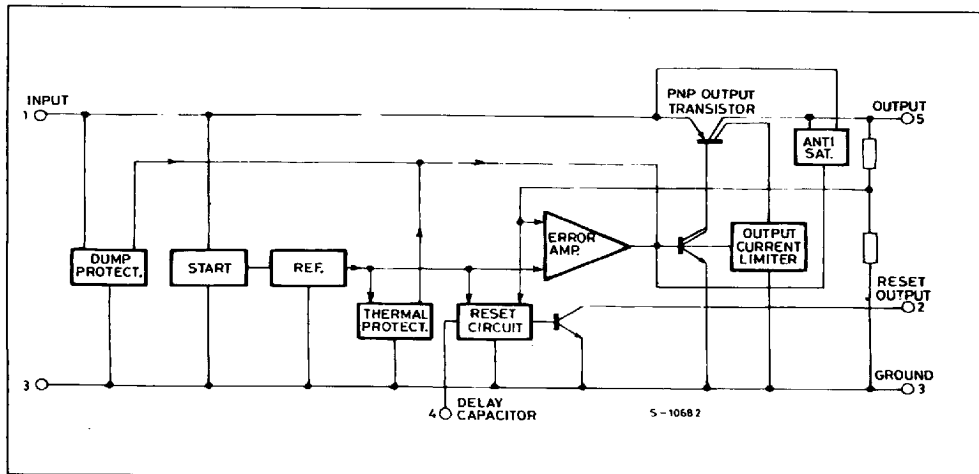
ORDERING NUMBER: L4947/R

### DESCRIPTION

The L4947/R is a monolithic integrated circuit in Pentawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L4947/R can work correctly even during the cranking phase, when the battery voltage could

fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems : a signal is available (after an externally programmable delay) to reset the microprocessor at power-on phase ; at power-off, this signal becomes low inhibiting the microprocessor.

### BLOCK DIAGRAM



October 1991

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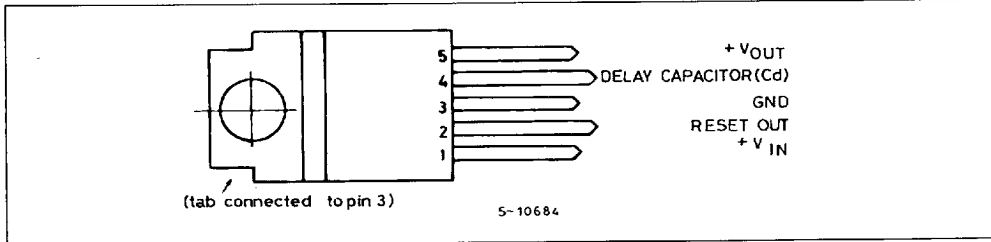
191

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_i$	DC Input Voltage	35	V
	DC Reverse Input Voltage	- 18	V
	Transient Input Overvoltages :	80	V
	Load Dump :		
	5ms ≤ $t_{rise}$ ≤ 10ms		
	$\tau_f$ Fall Time Constant = 100ms		
$V_R$	$R_{SOURCE} \geq 0.5\Omega$	- 80	V
	Field Decay :		
	5ms ≤ $t_{fall}$ ≤ 10ms, $R_{SOURCE} \geq 10\Omega$		
	$\tau_r$ Rise Time Constant = 33ms	± 100	V
	Low Energy Spike :		
	$t_{rise} = 1\mu s$ , $t_{fall} = 500\mu s$ , $R_{SOURCE} \geq 10\Omega$		
$T_J, T_{stg}$	$f_r$ Repetition Frequency = 5Hz		
$V_R$	Reset Output Voltage	35	V
$T_J, T_{stg}$	Junction and Storage Temperature Range	- 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

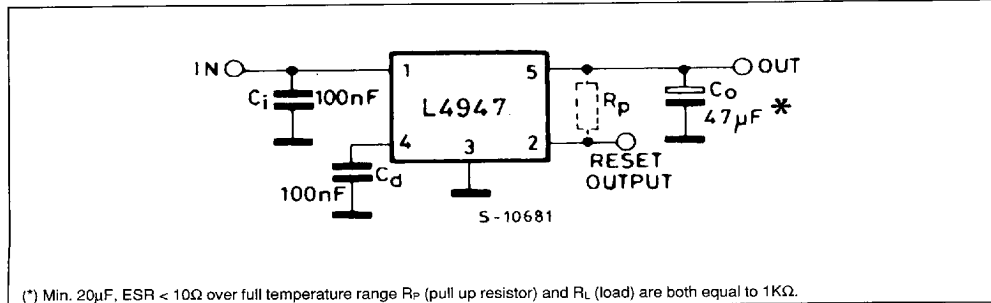
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th j-case}$	Thermal Resistance Junction-case	Max 3.5	°C/W

TEST CIRCUIT



(\*) Min. 20μF, ESR < 10Ω over full temperature range  $R_p$  (pull up resistor) and  $R_L$  (load) are both equal to 1KΩ.

**ELECTRICAL CHARACTERISTICS** (refer to the test circuit,  $V_i = 14.4\text{V}$ ,  $C_o = 47\mu\text{F}$ ,  $\text{ESR} < 10\Omega$ ,  $R_p = 1\text{K}\Omega$ ,  $R_L = 1\text{K}\Omega$ ,  $-40^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_o$	Output Voltage	$I_o = 0\text{mA}$ to $500\text{mA}$ Over Full T Range $T_J = 25^\circ\text{C}$	4.80	5.00	5.20	V
$V_i$	Operating Input Voltage	$I_o = 0\text{mA}$ to $(*) 500\text{mA}$	6		26	V
$\Delta V_o$	Line Regulation	$V_i = 6\text{V}$ to $26\text{V}$ ; $I_o = 5\text{mA}$		2	10	mV
$\Delta V_o$	Load Regulation	$I_o = 5\text{mA}$ to $500\text{mA}$		15	60	mV
$V_i - V_o$	Dropout Voltage	$I_o = 500\text{mA}$ , $T_J = 25^\circ\text{C}$ Over Full T Range		0.40	0.55 0.75	V
$I_q$	Quiescent Current	$I_o = 0\text{mA}$ , $T_J = 25^\circ\text{C}$ $I_o = 0\text{mA}$ Over Full T $I_o = 500\text{mA}$ Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			-0.5		mV/ $^\circ\text{C}$
SVR	Supply Volt. Rej.	$I_o = 350\text{mA}$ ; $f = 120\text{Hz}$ $C_o = 100\mu\text{F}$ ; $V_i = 12\text{V} \pm 5V_{pp}$	50	60		dB
$I_{sc}$	Output Short Circuit Current		0.50	0.80	1.50	A
$V_R$	Reset Output Saturation Voltage	$1.5\text{V} < V_o < V_{RT(\text{off})}$ , $I_R = 1.6\text{mA}$ $3.0\text{V} < V_o < V_{RT(\text{off})}$ , $I_R = 8\text{mA}$			0.40 0.40	V V
$I_R$	Reset Output Leakage Current	$V_o$ in Regulation, $V_R = 5\text{V}$			50	$\mu\text{A}$
$V_{RT(\text{peak})}$	Power On-Off Reset out Peak Voltage	$1\text{K}\Omega$ Reset Pull-up to $V_o$ , $T_J = 25^\circ\text{C}$		0.50	0.80	V
$V_{RT(\text{off})}$	Power OFF $V_o$ Threshold	$V_o$ @ Reset Out H to L Transition $T_J = 25^\circ\text{C}$	4.70 4.75	$V_o - 0.15$		V V
$V_{RT(\text{on})}$	Power ON $V_o$ Threshold	$V_o$ @ Reset Out L to H Transition		$V_{RT(\text{off})} + 0.05$	$V_o - 0.04$	V
$V_{Hyst}$	Power ON-Off Hysteresis	$V_{RT(\text{on})} - V_{RT(\text{off})}$		0.05		V
$V_d$	Delay Comparator Threshold	$V_d$ @ Reset Out L to H Transition	3.65	4.00	4.35	V
		$V_d$ @ Reset Out H to L Transition	3.20	3.55	3.90	V
$V_{dH}$	Delay Comparator Hysteresis			0.45		V
$I_d$	Delay Capacitor Charging Current	$V_d = 3\text{V}$ , $T_J = 25^\circ\text{C}$		20		$\mu\text{A}$
$V_{disch}$	Delay Capacitor Discharge Voltage	$V_o < V_{RT(\text{off})}$		0.55	1.20	V
$T_d$	Power on Reset Delay Time	$C_d = 100\text{nF}$ , $T_J = 25^\circ\text{C}$	10	20	30	ms

(\*) For a DC voltage  $26 < V_i < 37\text{V}$  the device is not operating

## FUNCTIONAL DESCRIPTION

The L4947/R is a very low drop 5V/0.5A voltage regulator provided with a reset function and therefore particularly suited to meet the requirements of supplying the microprocessor systems used in automotive and industrial applications.

The block diagram shows the basic structure of the device : the reference, the error amplifier, the driver, the power PNP, the protection and reset

functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at  $T_J = 25^\circ\text{C}$ , max. 750mV over the full temperature range @  $I_o = 500\text{mA}$ ). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where  $I_o = 500\text{mA}$ .

The current consumption of the device (quiescent

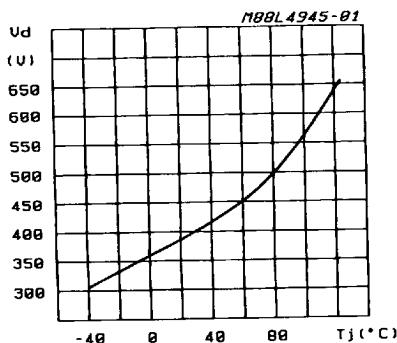
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current) is maximum 13mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The reset function supervises the regulator output voltage inhibiting the microprocessor when the device is out of regulation and resetting it at the power-on after a settable delay. The reset is LOW when the output voltage value is lower than the reset threshold voltage. At the power-on phase the output voltage increases (see Fig. 2) and - when it reaches the power-on  $V_O$  threshold  $V_{RT(On)}$  - the reset output becomes HIGH after a delay time set by the external capacitor  $C_d$ . At the power-off the output voltage decreases : at the  $V_{RT(Off)}$  threshold value ( $V_O$ -0.15V typ. value) the reset output instantaneously goes down (LOW status) inhibiting the microprocessor. The typical

**Figure 1: Typical Dropout Voltage vs.  $T_j$**   
( $I_o = 500\text{mA}$ ).



**Figure 2: Reset Waveforms:**  
 (1) Without External Capacitor  $C_d$ .  
 (2) With External Capacitor  $C_d$ .

