MC145158-2

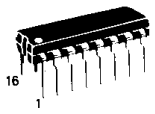
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

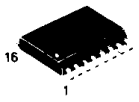
The MC145158-2 has a fully programmable 14-bit reference counter, as well as fully programmable ÷ N and ÷ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145158-2 is an improved-performance drop-in replacement for the MC145158-1. Power consumption has decreased and ESD and latch-up performance have improved.

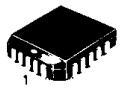
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 1023
- Dual Modulus Capability; ÷ A Range = 0 to 127
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOG
CASE 751G



FN SUFFIX
PLCC
CASE 775

ORDERING INFORMATION

MC145158P2	Plastic DIP
MC145158DW2	SOG Package
MC145158FN2	PLCC Package

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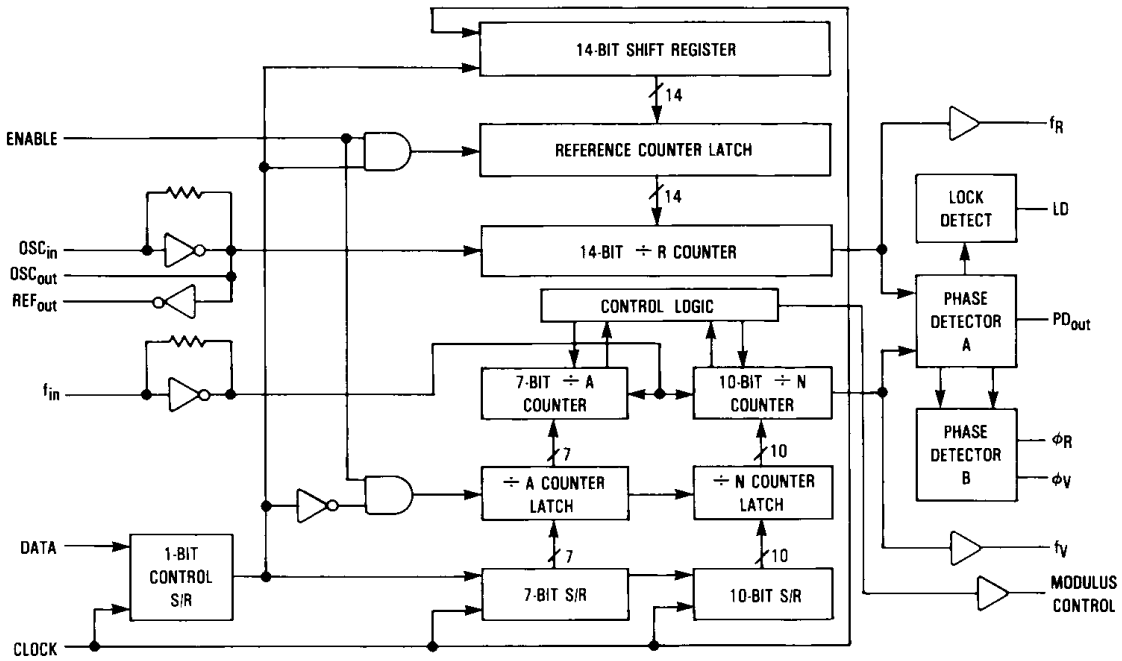
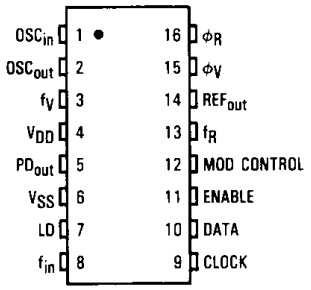
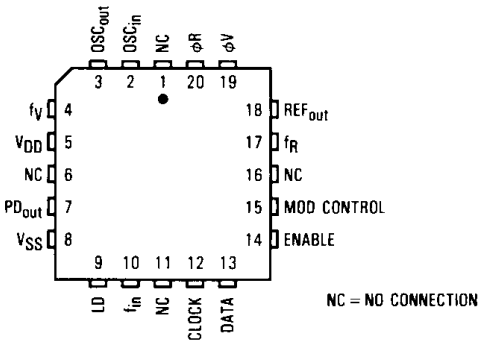
BLOCK DIAGRAM



PIN ASSIGNMENTS



PLASTIC DIP
SOG PACKAGE



PLCC PACKAGE

PIN DESCRIPTIONS

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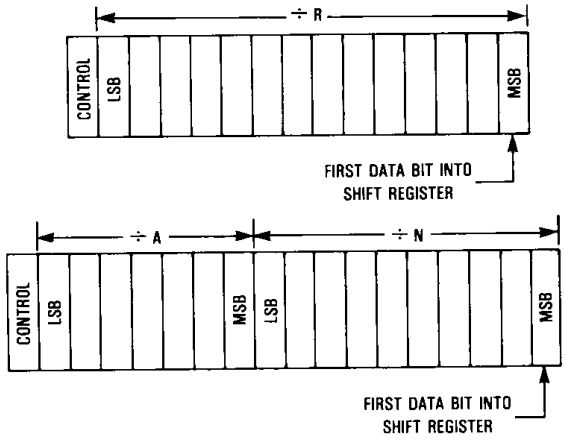
INPUTS

f_{in}—Frequency Input

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mV p-p. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

CLOCK, DATA—Shift Clock, Serial Data Inputs

Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic one selects the reference counter latch and a logic zero selects the ÷ A, ÷ N counter latch. The data entry format is as follows:



ENABLE—Latch Enable Input

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. Enable is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}—Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUTS

PD_{out}—Phase Detector A Output

This single ended (three-state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕV, ϕR—Phase Detector B Outputs

Double-ended phase detector outputs. These outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

Modulus Control—Dual-Modulus Prescale Control Output

This output generates a signal by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). Modulus Control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N•P + A where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual-modulus version offers a distinct advantage. The dual-modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V—R Counter Output, N Counter Output

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD—Lock Detector Output

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}—Buffered Oscillator Output

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY

V_{DD}

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}

The most negative supply potential. This pin is usually ground.

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FAMILY CHARACTERISTICS

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient), except SW1, SW2	−0.5 to V_{DD}+0.5	V
V_{out}	Output Voltage (DC or Transient), SW1 or SW2 (R_{pullup} = 4.7 kΩ)	−0.5 to +15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: −12 mW/°C from 65°C to 85°C
PLCC Package: −12 mW/°C from 65°C to 85°C
SOG Package: −7 mW/°C from 65°C to 85°C

These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V dc, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pullup devices. Unused outputs must be left open.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		–	3	9	3	9	3	9	V
I_{ss}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 Vp-p ac-coupled sine wave R = 128, A = 32, N = 128	3	–	3.5	–	3	–	3	mA
			5	–	10	–	7.5	–	7.5	
			9	–	30	–	24	–	24	
I_{SS}	Quiescent Supply Current (not including pullup current component)	$V_{in} = V_{DD}$ or V_{SS}, I_{out} = 0 μA	3	–	800	–	800	–	1600	μA
			5	–	1200	–	1200	–	2400	
			9	–	1600	–	1600	–	3200	
V_{in}	Input Voltage—f_{in}, OSC_{in}	Input ac-coupled sine wave	–	500	–	500	–	500	–	mVp-p
V_{IL}	Low-Level Input Voltage—f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input dc-coupled square wave	3	–	0	–	0	–	0	V
		$V_{out} \ge 3.5$ V	5	–	0	–	0	–	0	
		$V_{out} \ge 6.3$ V	9	–	0	–	0	–	0	
V_{IH}	High-Level Input Voltage—f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input dc-coupled square wave	3	3.0	–	3.0	–	3.0	–	V
		$V_{out} \le 1.5$ V	5	5.0	–	5.0	–	5.0	–	
		$V_{out} \le 2.7$ V	9	9.0	–	9.0	–	9.0	–	
V_{IL}	Low-Level Input Voltage—except f_{in}, OSC_{in}		3	–	0.9	–	0.9	–	0.9	V
			5	–	1.5	–	1.5	–	1.5	
			9	–	2.7	–	2.7	–	2.7	
V_{IH}	High-Level Input Voltage—except f_{in}, OSC_{in}		3	2.1	–	2.1	–	2.1	–	V
			5	3.5	–	3.5	–	3.5	–	
			9	6.3	–	6.3	–	6.3	–	
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9	±2	±50	±2	±25	±2	±22	μA
I_{IL}	Input Leakage Current (Data, Clock, Enable—without Pullups)	$V_{in} = V_{SS}$	9	–	−0.3	–	−0.1	–	−1.0	μA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9	–	0.3	–	0.1	–	1.0	μA
I_{IL}	Pullup Current (all inputs with Pullups)	$V_{in} = V_{SS}$	9	−20	−400	−20	−200	−20	−170	μA
C_{in}	Input Capacitance		–	–	10	–	10	–	10	pF

Continued

FAMILY CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage—OSC_{out}	$I_{out} \approx 0\ \mu A$ $V_{in} = V_{DD}$	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High-Level Output Voltage—OSC_{out}	$I_{out} \approx 0\ \mu A$ $V_{in} = V_{SS}$	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low-Level Output Voltage—Other Outputs	$I_{out} \approx 0\ \mu A$	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High-Level Output Voltage—Other Outputs	$I_{out} \approx 0\ \mu A$	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage—SW1, SW2	$R_{pullup} = 4.7\ k\Omega$	—	15	—	15	—	15	—	V
I_{OL}	Low-Level Sinking Current—Modulus Control	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	mA
I_{OH}	High-Level Sourcing Current—Modulus Control	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	−0.60 −0.90 −1.50	— — —	−0.50 −0.75 −1.25	— — —	−0.30 −0.50 −0.80	— — —	mA
I_{OL}	Low-Level Sinking Current—Lock Detect	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.25 0.64 1.30	— — —	0.20 0.51 1.00	— — —	0.15 0.36 0.70	— — —	mA
I_{OH}	High-Level Sourcing Current—Lock Detect	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	−0.25 −0.64 −1.30	— — —	−0.20 −0.51 −1.00	— — —	−0.15 −0.36 −0.70	— — —	mA
I_{OL}	Low-Level Sinking Current—SW1, SW2	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.05	— — —	mA
I_{OL}	Low-Level Sinking Current—Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	mA
I_{OH}	High-Level Sourcing Current—Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	−0.44 −0.64 −1.30	— — —	−0.35 −0.51 −1.00	— — —	−0.22 −0.36 −0.70	— — —	mA
I_{OZ}	Output Leakage Current—PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	±0.3	—	±0.1	—	±1.0	μA
I_{OZ}	Output Leakage Current—SW1, SW2	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	±0.3	—	±0.1	—	±3.0	μA
C_{out}	Output Capacitance—PD_{out}	PD_{out}—3-State	—	—	10	—	10	—	10	pF

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FAMILY CHARACTERISTICS

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to Modulus Control (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, Enable to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, Modulus Control (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, Modulus Control (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Lock Detect (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

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SWITCHING WAVEFORMS

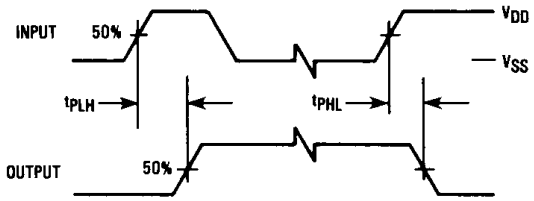
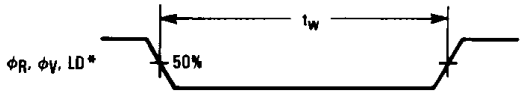


Figure 1



*f_R in phase with f_V.

Figure 2

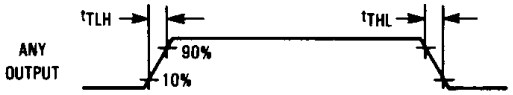
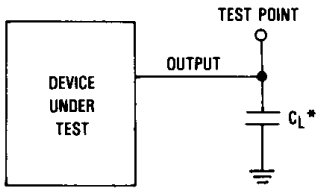
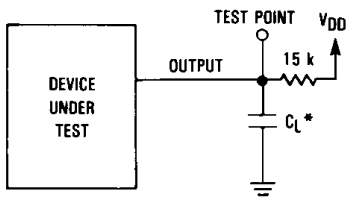


Figure 3



*Includes all probe and jig capacitance.

Figure 4. Test Circuit



*Includes all probe and jig capacitance.

Figure 5. Test Circuit

FAMILY CHARACTERISTICS

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to Clock $t_{w(H)}$ below (Figure 6)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to Clock (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, Clock to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, Clock to Enable (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, Enable to Clock (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, Clock, Enable (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times—Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	μs

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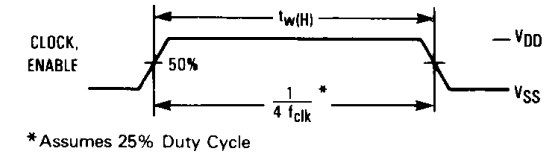
SWITCHING WAVEFORMS



*Assumes 25% Duty Cycle

Figure 6

Figure 8

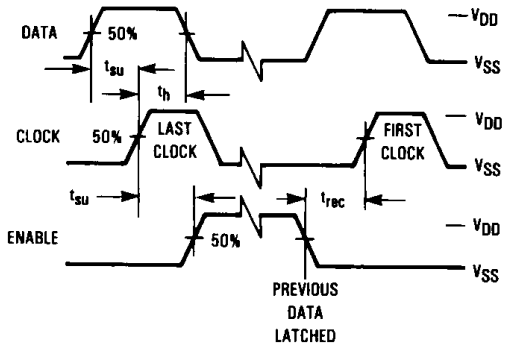
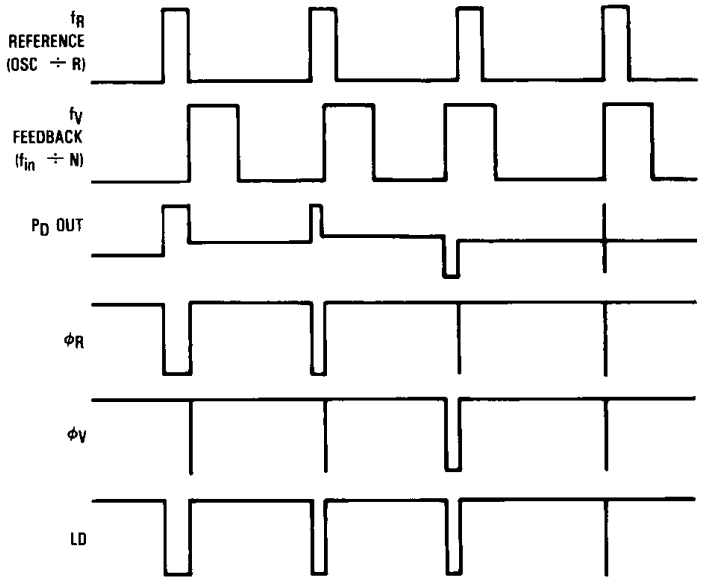


Figure 7

FAMILY CHARACTERISTICS

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R≥8, A≥0, N≥8 V_{in} = 500 mVp-p ac-coupled sine wave	3 5 9	– – –	6 15 15	– – –	6 15 15	– – –	6 15 15	MHz
		R≥8, A≥0, N≥8 V_{in} = 1 Vp-p ac-coupled sine wave	3 5 9	– – –	12 22 25	– – –	12 20 22	– – –	7 20 22	MHz
		R≥8, A≥0, N≥8 $V_{in} = V_{DD}$ to V_{SS} dc-coupled square wave	3 5 9	– – –	13 25 25	– – –	12 22 25	– – –	8 22 25	MHz



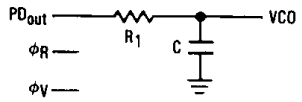
NOTE: The P_D output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

Figure 9. Phase Detector/Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

A)

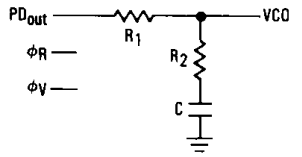


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

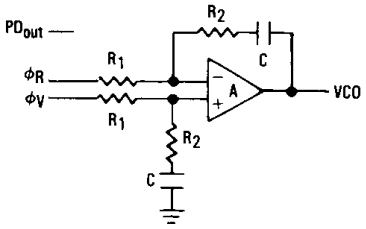


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\ \omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)\,sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design ω_n (Natural Frequency) $\cong \frac{2\pi fr}{10}$ (at phase detector input),

Damping Factor: $\zeta \cong 1$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA. Tab Books, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design*, 1987.
BR504/D, Electronic Tuning Address Systems, Motorola Semiconductor Products, Inc., 1986.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

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DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

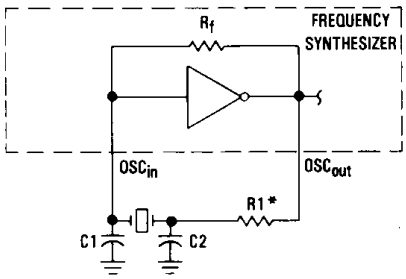
The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.

For $V_{DD} = 5$ V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where

$C_{in} = 5$ pF (see Figure 11)
$C_{out} = 6$ pF (see Figure 11)
$C_a = 1$ pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)



*May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

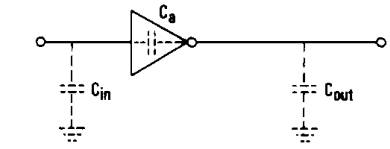
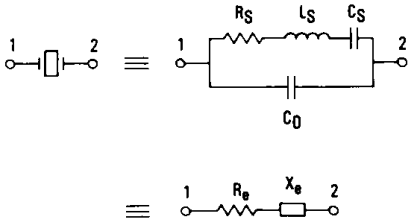


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases; i.e., R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize

DESIGN CONSIDERATIONS

loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdiven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit—Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2; Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

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DESIGN CONSIDERATIONS

DUAL-MODULUS PRESCALING

OVERVIEW

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual-modulus frequency synthesizers contain this feature and can be used with a variety of dual-modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/ ÷ 4 to ÷ 128/ ÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual-modulus prescaler approaches suitable for use with the MC145152-2, MC145156-2, or MC145158-2 are:

MC12009	÷ 5/ ÷ 6	440 MHz
MC12011	÷ 8/ ÷ 9	500 MHz
MC12013	÷ 10/ ÷ 11	500 MHz
MC12015	÷ 32/ ÷ 33	225 MHz
MC12016	÷ 40/ ÷ 41	225 MHz
MC12017	÷ 64/ ÷ 65	225 MHz
MC12018	÷ 128/ ÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application,i.e.

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P − 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from zero through P − 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters. The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\ P + A$ or $(P - 1)\ P$ since A is free to assume the value of zero.

$$N_{Tmax} = N_{max} \cdot P + A_{max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its modulus control is low.

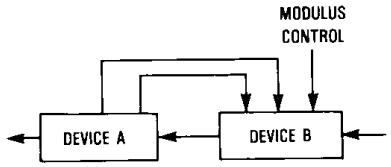
For the maximum frequency into the prescaler ($f_{VCO}max$), the value used for P must be large enough such that:

A. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
B. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual-modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value for N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

A. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
B. Always program all higher order ÷ A counter bits above "a" to zero.
C. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using two devices, several dual-modulus values are achievable:



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/ ÷ 21	÷ 32/ ÷ 33	÷ 40/ ÷ 41
MC10138	÷ 50/ ÷ 51	÷ 80/ ÷ 81	÷ 100/ ÷ 101
MC10154	÷ 40/ ÷ 41 OR ÷ 80/ ÷ 81	÷ 64/ ÷ 65 OR ÷ 128/ ÷ 129	÷ 80/ ÷ 81

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.