LMV793/LMV794 88 MHz, Low Noise, 1.8V CMOS Input, Decompensated Operational Amplifiers

Check for Samples: LMV793, LMV794

FEATURES

(Typical 5V Supply, Unless Otherwise Noted)

- **Input Referred Voltage Noise 5.8 nV/√Hz**
- **Input Bias Current 100 fA**
- **Gain Bandwidth Product 88 MHz**
- **Supply Current per Channel**
  - **LMV793 1.15 mA**
  - **LMV794 1.30 mA**
- **Rail-to-Rail Output Swing**
  - **@ 10 kΩ Load 25 mV from Rail**
  - **@ 2 kΩ Load 45 mV from Rail**
- **Ensured 2.5V and 5.0V Performance**
- **Total Harmonic Distortion 0.04% @1 kHz, 600Ω**
- **Temperature Range −40°C to 125°C**

APPLICATIONS

- **ADC Interface**
- **Photodiode Amplifiers**
- **Active Filters and Buffers**
- **Low Noise Signal Processing**
- **Medical Instrumentation**
- **Sensor Interface Applications**

DESCRIPTION

The LMV793 (single) and the LMV794 (dual) CMOS input operational amplifiers offer a low input voltage noise density of 5.8 nV/√Hz while consuming only 1.15 mA (LMV793) of quiescent current. The LMV793/LMV794 are stable at a gain of 10 and have a gain bandwidth product (GBW) of 88 MHz. The LMV793/LMV794 have a supply voltage range of 1.8V to 5.5V and can operate from a single supply. The LMV793/LMV794 each feature a rail-to-rail output stage capable of driving a 600Ω load and sourcing as much as 60 mA of current.

The LMV793/LMV794 provide optimal performance in low voltage and low noise systems. A CMOS input stage, with typical input bias currents in the range of a few femto-Amperes, and an input common mode voltage range, which includes ground, make the LMV793/LMV794 ideal for low power sensor applications where high speeds are needed.

The LMV793/LMV794 are manufactured using TI's advanced VIP50 process. The LMV793 is offered in either a 5-Pin SOT23 or an 8-Pin SOIC package. The LMV794 is offered in either the 8-Pin SOIC or the 8-Pin VSSOP.

Typical Application

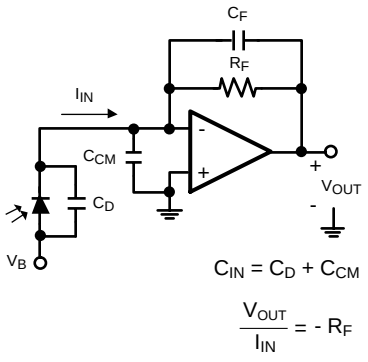


Figure 1. Photodiode Transimpedance Amplifier

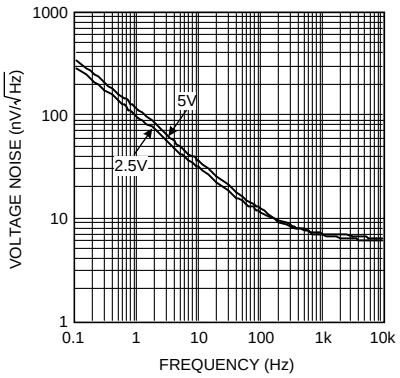


Figure 2. Input Referred Voltage Noise vs. Frequency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Human Body Model	2000V
	Machine Model	200V
	Charge-Device Model	1000V
V_{IN} Differential		±0.3V
Supply Voltage ($V^+ - V^-$)		6.0V
Input/Output Pin Voltage		V^+ +0.3V, V^- −0.3V
Storage Temperature Range		−65°C to 150°C
Junction Temperature(4)		+150°C
Soldering Information	Infrared or Convection (20 sec)	235°C
	Wave Soldering Lead Temp (10 sec)	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Temperature Range(2)		−40°C to 125°C
Supply Voltage ($V^+ - V^-$)	−40°C ≤ T_A ≤ 125°C	2.0V to 5.5V
	0°C ≤ T_A ≤ 125°C	1.8V to 5.5V
Package Thermal Resistance (θ_{JA}(2))	5-Pin SOT-23	180°C/W
	8-Pin SOIC	190°C/W
	8-Pin VSSOP	236°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

2.5V Electrical Characteristics(1)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5V, V^- = 0V, $V_{CM} = V^+/2 = V_O$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage			0.1	±1.35 **±1.65**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift(4)	LMV793		−1.0		µV/°C
		LMV794		−1.8		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.

2.5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 2.5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
I_B	Input Bias Current	V_{CM} = 1.0V [5] [6]	−40°C ≤ T_A ≤ 85°C		0.05	1 **25**	pA
			−40°C ≤ T_A ≤ 125°C		0.05	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 1.0V [6]			10		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V		80 **75**	94		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80 **75**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB		−0.3 **-0.3**		1.5 **1.5**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.15V to 2.2V, R_L = 2 kΩ to $V^+/2$	LMV793	85 **80**	98		dB
			LMV794	82 **78**	92		
		V_{OUT} = 0.15V to 2.2V, R_L = 10 kΩ to $V^+/2$		88 **84**	110		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to $V^+/2$			25	75 **82**	mV from either rail
		R_L = 10 kΩ to $V^+/2$			20	65 **71**	
	Output Voltage Swing Low	R_L = 2 kΩ to $V^+/2$			30	75 **78**	
		R_L = 10 kΩ to $V^+/2$			15	65 **67**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV [7]		35 **28**	47		mA
		Sinking to V^+ V_{IN} = –200 mV [7]		7 **5**	15		
I_S	Supply Current Per Amplifier	LMV793			0.95	1.30 **1.65**	mA
		LMV794			1.1	1.50 **1.85**	
SR	Slew Rate	A_V = +10, Rising (10% to 90%)			32		V/µs
		A_V = +10, Falling (90% to 10%)			24		
GBW	Gain Bandwidth	A_V = +10, R_L = 10 kΩ			88		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz			6.2		nV/√Hz
i_n	Input Referred Current Noise Density	f = 1 kHz			0.01		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 600Ω			0.01		%

(5) Positive current corresponds to current flowing into the device.
(6) This parameter is specified by design and/or characterization and is not tested in production.
(7) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

5V Electrical Characteristics[1]

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min [2]	Typ [3]	Max [2]	Units
V_{OS}	Input Offset Voltage				0.1	±1.35 **±1.65**	mV
TC V_{OS}	Input Offset Voltage Temperature Drift[4]	LMV793			−1.0		µV/°C
		LMV794			−1.8		
I_B	Input Bias Current	V_{CM} = 2.0V[5] [6]	−40°C ≤ T_A ≤ 85°C		0.1	1 **25**	pA
			−40°C ≤ T_A ≤ 125°C		0.1	1 **100**	
I_{OS}	Input Offset Current	V_{CM} = 2.0V[6]			10		fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		80 **75**	100		dB
PSRR	Power Supply Rejection Ratio	2.0V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80 **75**	100		dB
		1.8V ≤ V^+ ≤ 5.5V, V_{CM} = 0V		80	98		
CMVR	Common Mode Voltage Range	CMRR ≥ 60 dB CMRR ≥ 55 dB		−0.3 **-0.3**		4 **4**	V
A_{VOL}	Open Loop Voltage Gain	V_{OUT} = 0.3V to 4.7V, R_L = 2 kΩ to $V^+/2$	LMV793	85 **80**	97		dB
			LMV794	82 **78**	89		
		V_{OUT} = 0.3V to 4.7V, R_L = 10 kΩ to $V^+/2$		88 **84**	110		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to $V^+/2$	LMV793		35	75 **82**	mV from either rail
			LMV794		35	75 **82**	
		R_L = 10 kΩ to $V^+/2$			25	65 **71**	
	Output Voltage Swing Low	R_L = 2 kΩ to $V^+/2$	LMV793		42	75 **78**	
			LMV794		45	80 **83**	
		R_L = 10 kΩ to $V^+/2$			20	65 **67**	
I_{OUT}	Output Current	Sourcing to V^- V_{IN} = 200 mV[7]		45 **37**	60		mA
		Sinking to V^+ V_{IN} = –200 mV[7]		10 **6**	21		
I_S	Supply Current per Amplifier	LMV793			1.15	1.40 **1.75**	mA
		LMV794 per Channel			1.30	1.70 **2.05**	

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlations using the statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Offset voltage average drift is determined by dividing the change in V_{OS} by temperature change.
(5) Positive current corresponds to current flowing into the device.
(6) This parameter is specified by design and/or characterization and is not tested in production.
(7) The short circuit test is a momentary test, the short circuit duration is 1.5 ms.

5V Electrical Characteristics[1] (continued)

Unless otherwise specified, all limits are specified for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$ = V_O. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min [2]	Typ [3]	Max [2]	Units
SR	Slew Rate	A_V = +10, Rising (10% to 90%)		35		V/µs
		A_V = +10, Falling (90% to 10%)		28		
GBW	Gain Bandwidth	A_V = +10, R_L = 10 kΩ		88		MHz
e_n	Input Referred Voltage Noise Density	f = 1 kHz		5.8		nV/√Hz
i_n	Input Referred Current Noise Density	f = 1 kHz		0.01		pA/√Hz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 600Ω		0.01		%

Connection Diagram

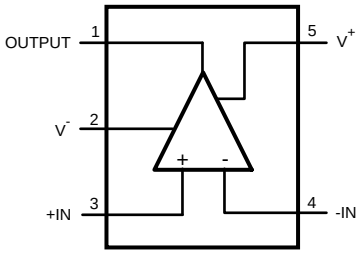


Figure 3. 5-Pin SOT-23 (LMV793)
Top View

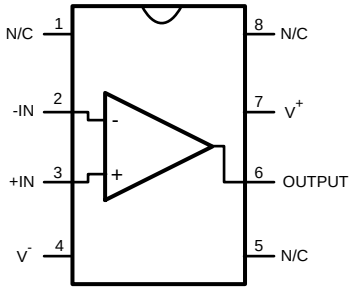


Figure 4. 8-Pin SOIC (LMV793)
Top View

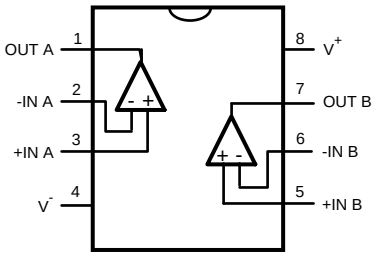


Figure 5. 8-Pin SOIC/VSSOP (LMV794)
Top View

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

Supply Current vs. Supply Voltage (LMV793)

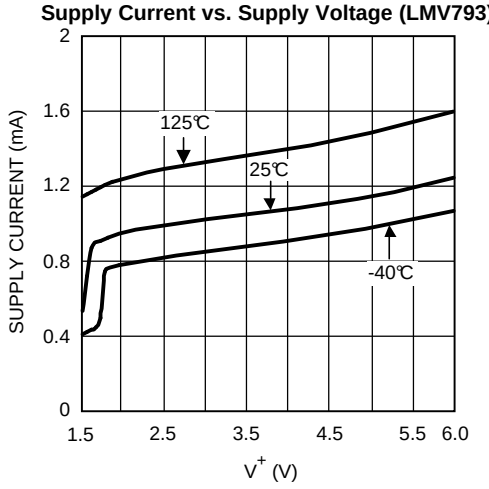


Figure 6.

Supply Current vs. Supply Voltage (LMV794)

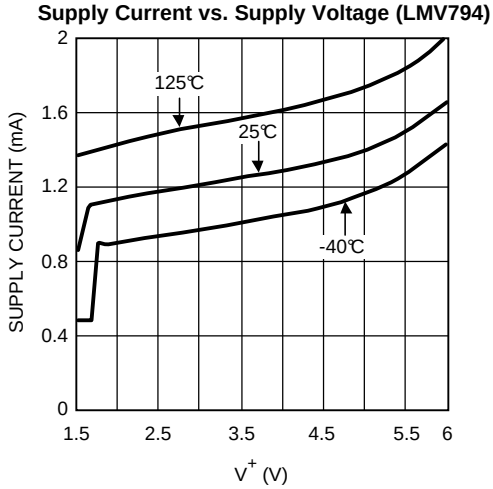


Figure 7.

V_{OS} vs. V_{CM}

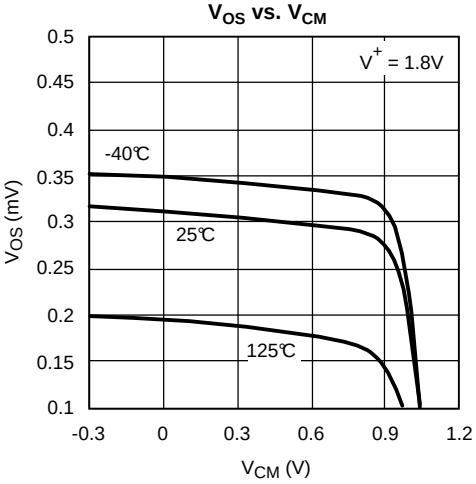


Figure 8.

V_{OS} vs. V_{CM}

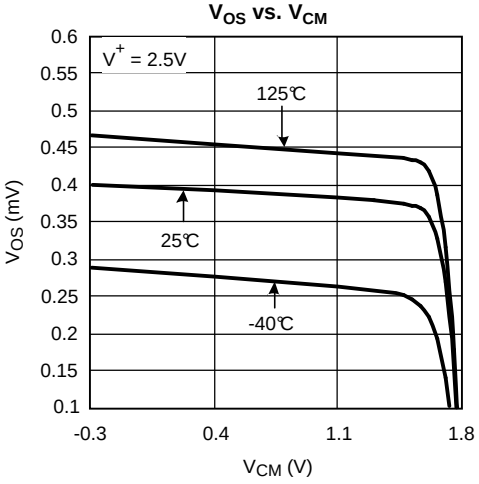


Figure 9.

V_{OS} vs. V_{CM}

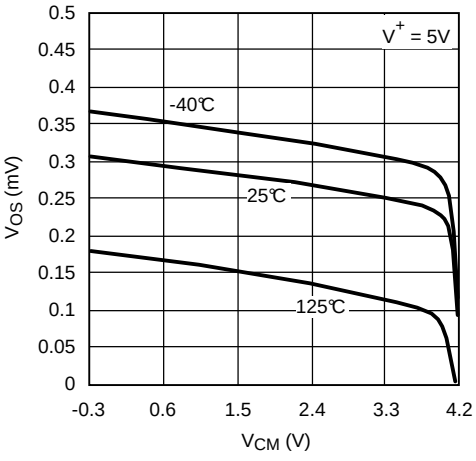


Figure 10.

V_{OS} vs. Supply Voltage

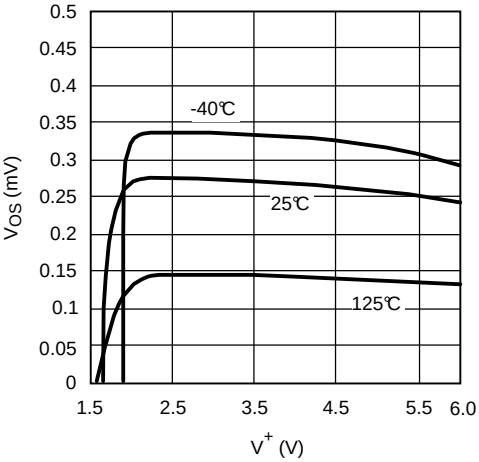


Figure 11.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

Slew Rate vs. Supply Voltage

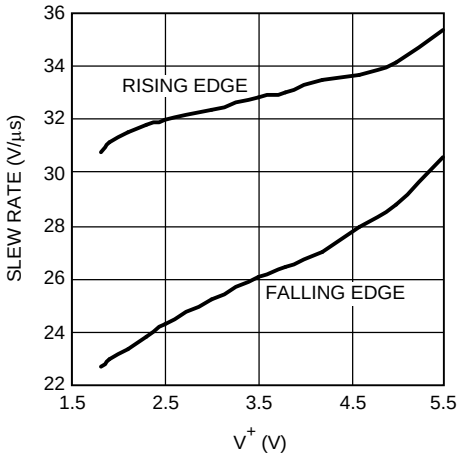


Figure 12.

Input Bias Current vs. V_{CM}

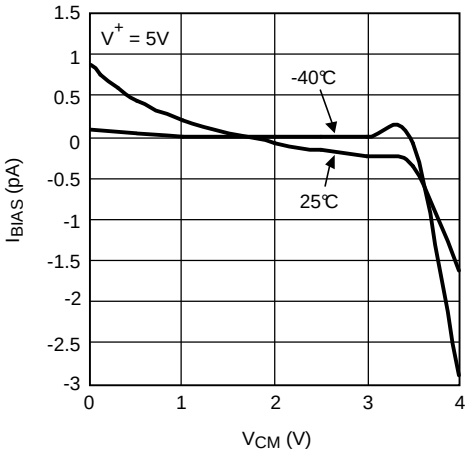


Figure 13.

Input Bias Current vs. V_{CM}

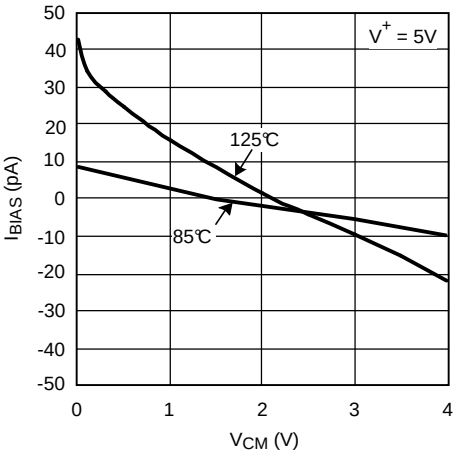


Figure 14.

Sourcing Current vs. Supply Voltage

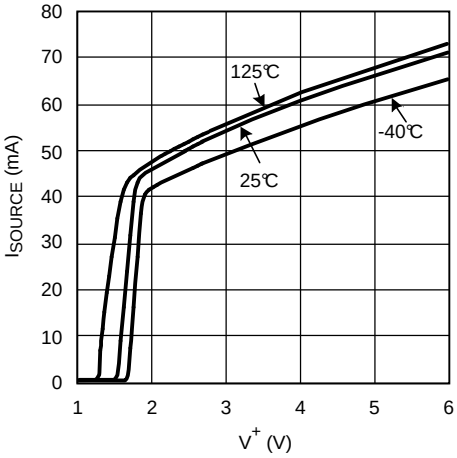


Figure 15.

Sinking Current vs. Supply Voltage

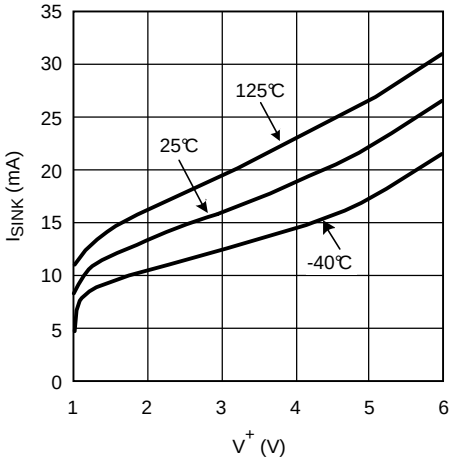


Figure 16.

Sourcing Current vs. Output Voltage

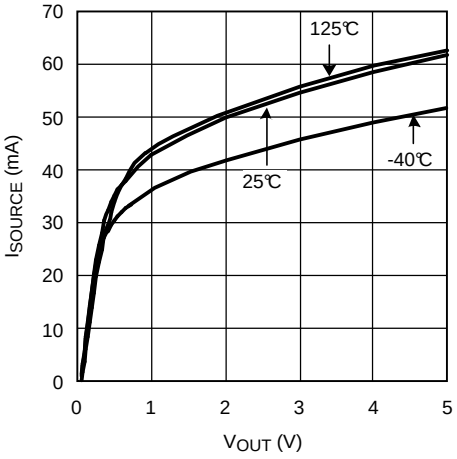


Figure 17.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

Sinking Current vs. Output Voltage

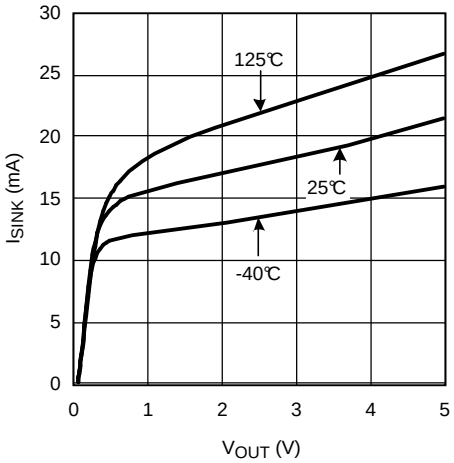


Figure 18.

Positive Output Swing vs. Supply Voltage

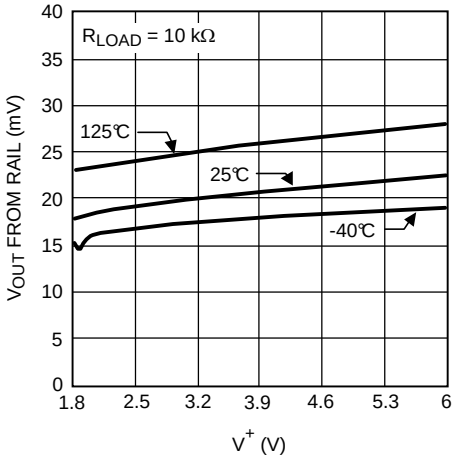


Figure 19.

Negative Output Swing vs. Supply Voltage

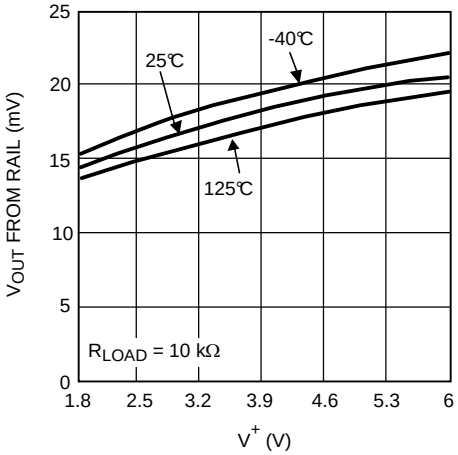


Figure 20.

Positive Output Swing vs. Supply Voltage

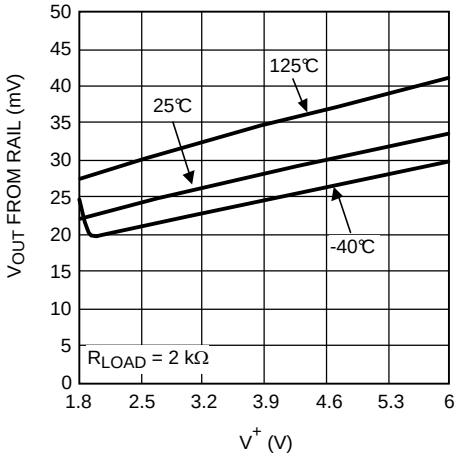


Figure 21.

Negative Output Swing vs. Supply Voltage

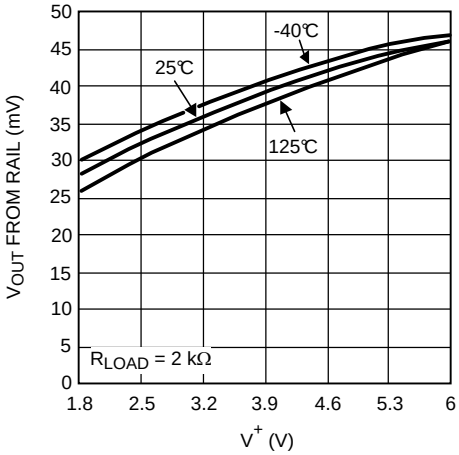


Figure 22.

Positive Output Swing vs. Supply Voltage

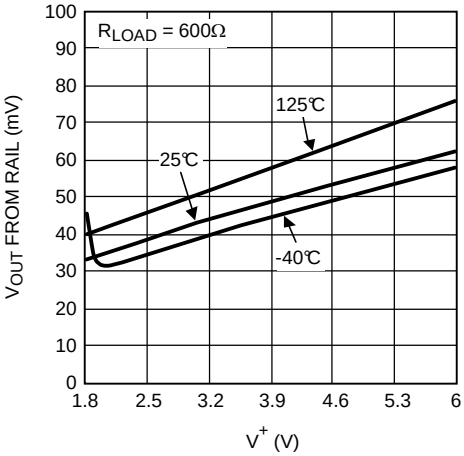


Figure 23.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

Negative Output Swing vs. Supply Voltage

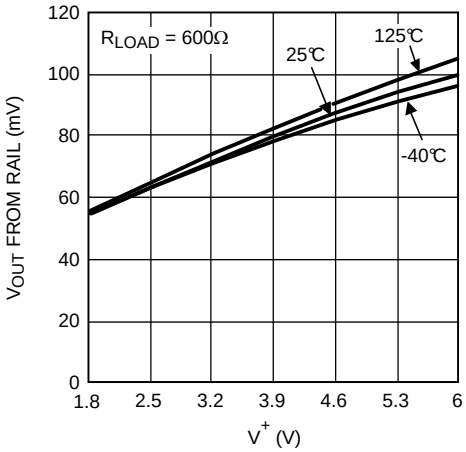


Figure 24.

Time Domain Voltage Noise

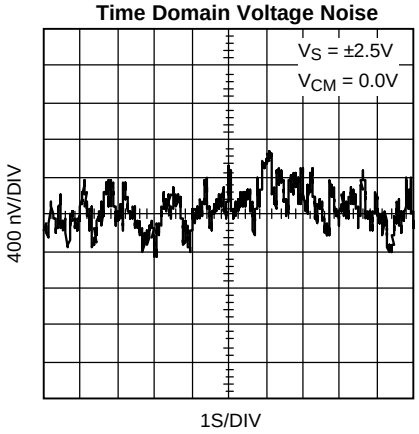


Figure 25.

Input Referred Voltage Noise vs. Frequency

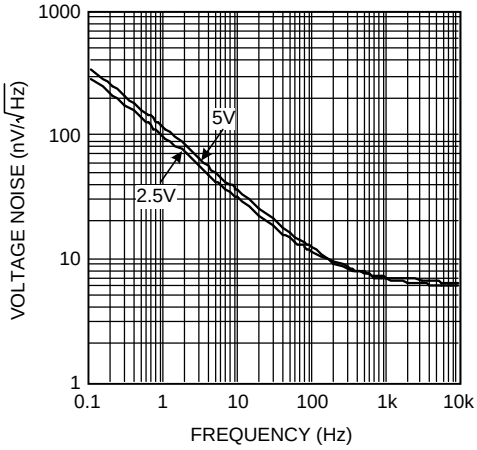


Figure 26.

Overshoot and Undershoot vs. C_{LOAD}

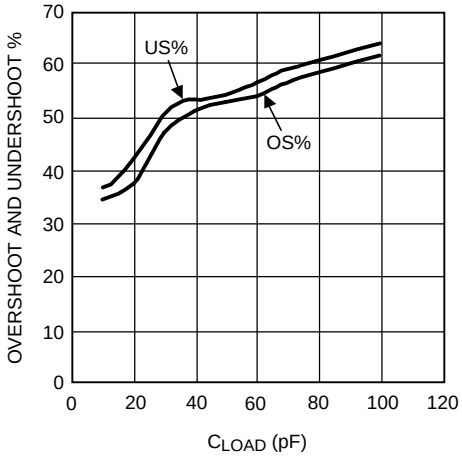


Figure 27.

THD+N vs. Frequency

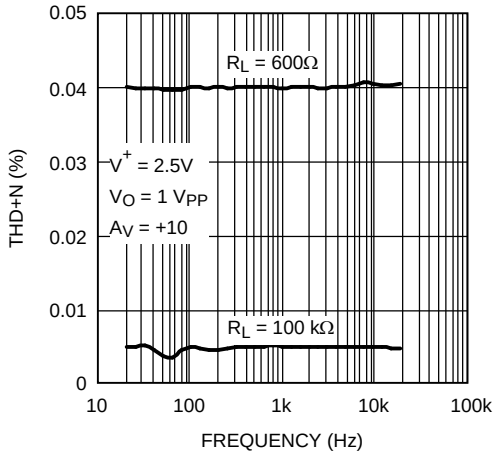


Figure 28.

THD+N vs. Frequency

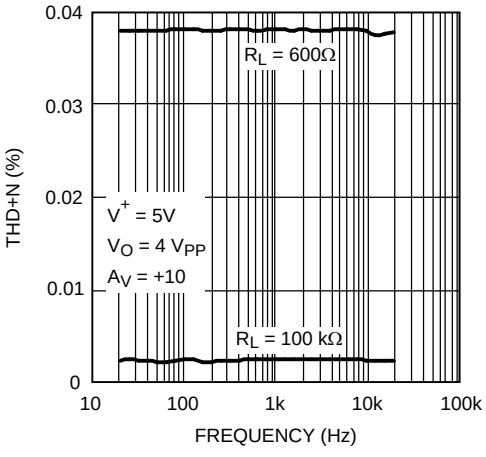


Figure 29.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})

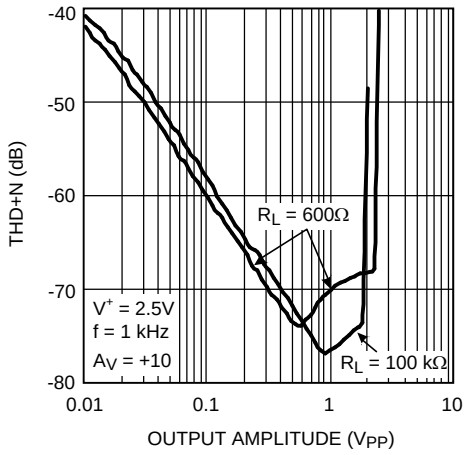


Figure 30.

THD+N vs. Peak-to-Peak Output Voltage (V_{OUT})

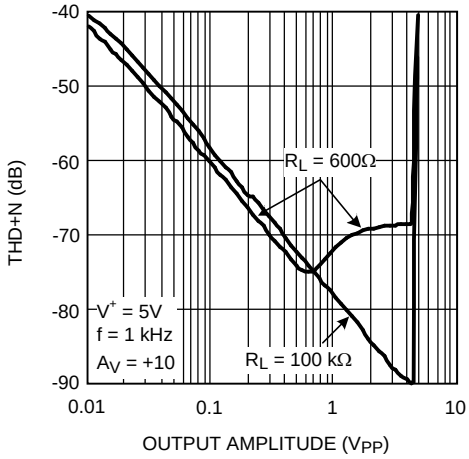


Figure 31.

Open Loop Gain and Phase

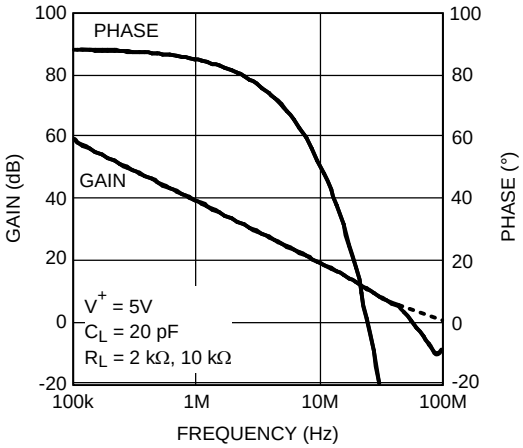


Figure 32.

Closed Loop Output Impedance vs. Frequency

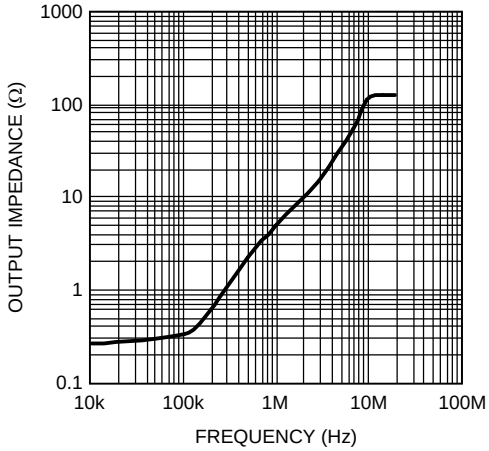


Figure 33.

Small Signal Transient Response, A_V = +10

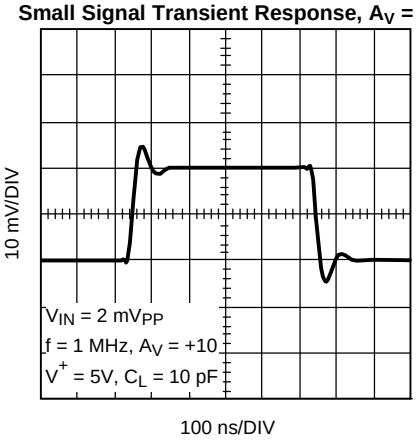


Figure 34.

Large Signal Transient Response, A_V = +10

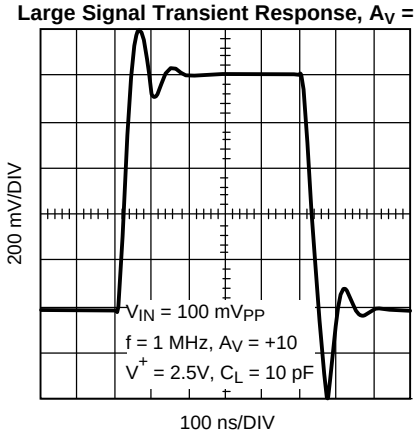


Figure 35.

Typical Performance Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V^- = 0, V^+ = Supply Voltage = 5V, V_{CM} = V^+/2.

Small Signal Transient Response, A_V = +10

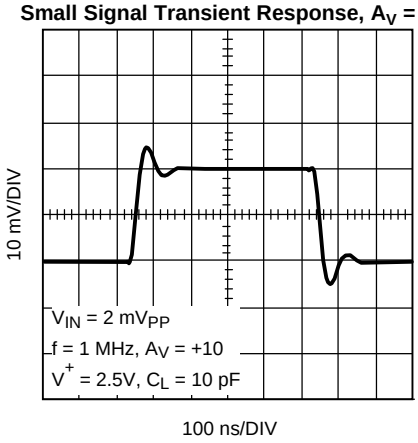


Figure 36.

Large Signal Transient Response, A_V = +10

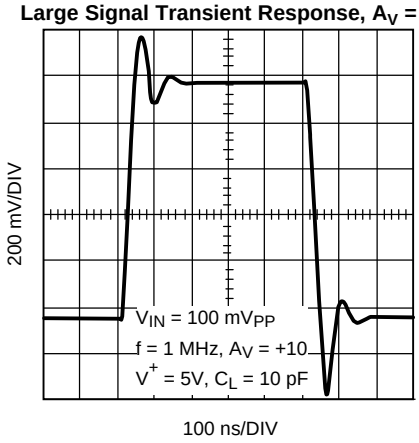


Figure 37.

PSRR vs. Frequency

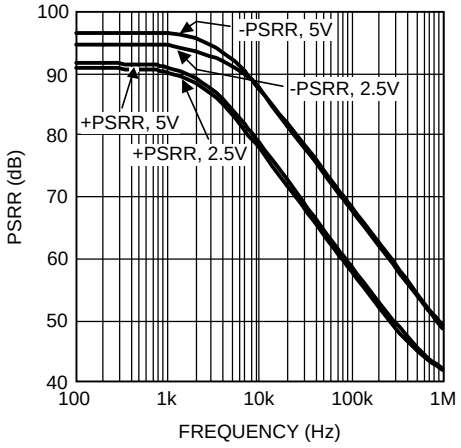


Figure 38.

CMRR vs. Frequency

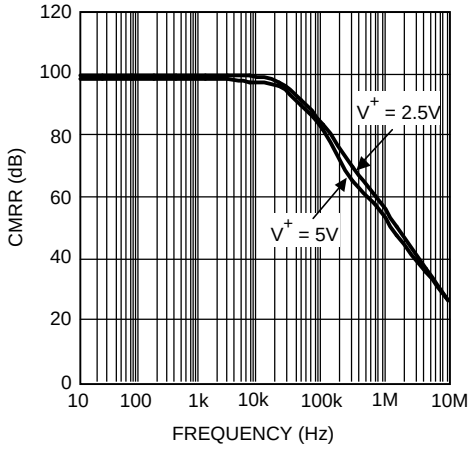


Figure 39.

Input Common Mode Capacitance vs. V_{CM}

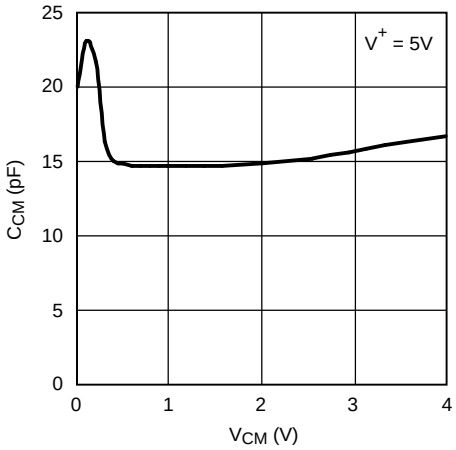


Figure 40.

APPLICATION INFORMATION

ADVANTAGES OF THE LMV793/LMV794

Wide Bandwidth at Low Supply Current

The LMV793/LMV794 are high performance op amps that provide a GBW of 88 MHz with a gain of 10 while drawing a low supply current of 1.15 mA. This makes them ideal for providing wideband amplification in data acquisition applications.

With the proper external compensation the LMV793/LMV794 can be operated at gains of ±1 and still maintain much faster slew rates than comparable unity gain stable amplifiers. The increase in bandwidth and slew rate is obtained without any additional power consumption over the LMV796.

Low Input Referred Noise and Low Input Bias Current

The LMV793/LMV794 have a very low input referred voltage noise density (5.8 nV/$\sqrt{Hz}$ at 1 kHz). A CMOS input stage ensures a small input bias current (100 fA) and low input referred current noise (0.01 pA/$\sqrt{Hz}$). This is very helpful in maintaining signal integrity, and makes the LMV793/LMV794 ideal for audio and sensor based applications.

Low Supply Voltage

The LMV793 and LMV794 have performance specified at 2.5V and 5V supply. These parts are specified to be operational at all supply voltages between 2.0V and 5.5V, for ambient temperatures ranging from −40°C to 125°C, thus utilizing the entire battery lifetime. The LMV793/LMV794 are also specified to be operational at 1.8V supply voltage, for temperatures between 0°C and 125°C optimizing their usage in low-voltage applications.

RRO and Ground Sensing

Rail-to-rail output swing provides the maximum possible dynamic range. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is used to boost the current drive capability of the output stage. This allows the LMV793/LMV794 to source more than 40 mA of current at 1.8V supply. This also limits the performance of these parts as comparators, and hence the usage of the LMV793 and the LMV794 in an open-loop configuration is not recommended. The input common-mode range includes the negative supply rail which allows direct sensing at ground in single supply operation.

Small Size

The small footprint of the LMV793 and the LMV794 package saves space on printed circuit boards, and enables the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. Long traces between the signal source and the op amp make the signal path more susceptible to noise pick up.

The physically smaller LMV793/LMV794 packages, allow the op amp to be placed closer to the signal source, thus reducing noise pickup and maintaining signal integrity.

USING THE DECOMPENSATED LMV793

Advantages of Decompensated Op Amps

A unity gain stable op amp, which is fully compensated, is designed to operate with good stability down to gains of ±1. The large amount of compensation does provide an op amp that is relatively easy to use; however, a decompensated op amp is designed to maximize the bandwidth and slew rate without any additional power consumption. This can be very advantageous.

The LMV793/LMV794 require a gain of ±10 to be stable. However, with an external compensation network (a simple RC network) these parts can be stable with gains of ±1 and still maintain the higher slew rate. Looking at the Bode plots for the LMV793 and its closest equivalent unity gain stable op amp, the LMV796, one can clearly see the increased bandwidth of the LMV793. Both plots are taken with a parallel combination of 20 pF and 10 kΩ for the output load.

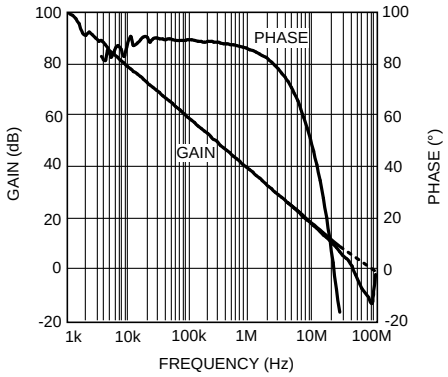


Figure 41. LMV793 A_{VOL} vs. Frequency

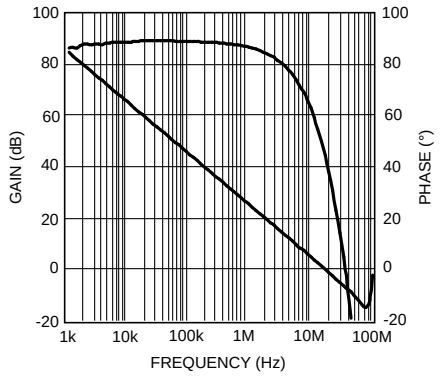


Figure 42. LMV796 A_{VOL} vs. Frequency

Figure 41 shows the much larger 88 MHz bandwidth of the LMV793 as compared to the 17 MHz bandwidth of the LMV796 shown in Figure 42. The decompensated LMV793 has five times the bandwidth of the LMV796.

What is a Decompensated Op Amp?

The differences between the unity gain stable op amp and the decompensated op amp are shown in Figure 43. This Bode plot assumes an ideal two pole system. The dominant pole of the decompensated op amp is at a higher frequency, f_1, as compared to the unity-gain stable op amp which is at f_d as shown in Figure 43. This is done in order to increase the speed capability of the op amp while maintaining the same power dissipation of the unity gain stable op amp. The LMV793/LMV794 have a dominant pole at 1.6 kHz. The unity gain stable LMV796/LMV797 have their dominant pole at 300 Hz.

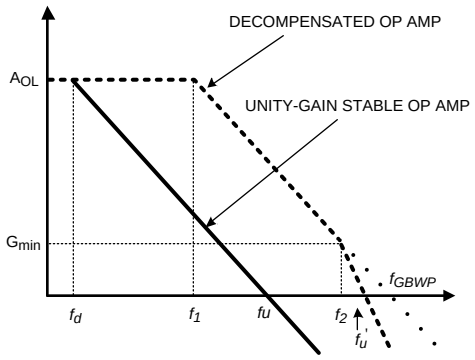


Figure 43. Open Loop Gain for Unity-Gain Stable Op Amp and Decompensated Op Amp

Having a higher frequency for the dominate pole will result in:

1. The DC open-loop gain (A_{VOL}) extending to a higher frequency.
2. A wider closed loop bandwidth.
3. Better slew rate due to reduced compensation capacitance within the op amp.

The second open loop pole (f_2) for the LMV793/LMV794 occurs at 45 MHz. The unity gain (f_u') occurs after the second pole at 51 MHz. An ideal two pole system would give a phase margin of 45° at the location of the second pole. The LMV793/LMV794 have parasitic poles close to the second pole, giving a phase margin closer to 0°. Therefore it is necessary to operate the LMV793/LMV794 at a closed loop gain of 10 or higher, or to add external compensation in order to assure stability.

For the LMV796, the gain bandwidth product occurs at 17 MHz. The curve is constant from f_d to f_u which occurs before the second pole.

For the LMV793/LMV794, the GBW = 88 MHz and is constant between f_1 and f_2. The second pole at f_2 occurs before A_{VOL} = 1. Therefore f_u' occurs at 51 MHz, well before the GBW frequency of 88 MHz. For decompensated op amps the unity gain frequency and the GBW are no longer equal. G_{min} is the minimum gain for stability and for the LMV793/LMV794 this is a gain of 18 to 20 dB.

Input Lead-Lag Compensation

The recommended technique which allows the user to compensate the LMV793/LMV794 for stable operation at any gain is lead-lag compensation. The compensation components added to the circuit allow the user to shape the feedback function to make sure there is sufficient phase margin when the loop gain is as low as 0 dB and still maintain the advantages over the unity gain op amp. Figure 44 shows the lead-lag configuration. Only R_C and C are added for the necessary compensation.

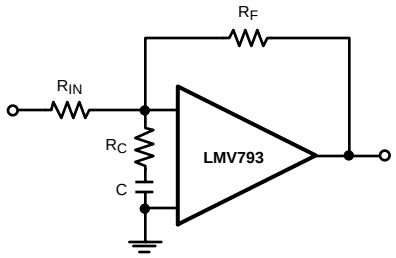


Figure 44. LMV793 with Lead-Lag Compensation for Inverting Configuration

To cover how to calculate the compensation network values it is necessary to introduce the term called the feedback factor or F. The feedback factor F is the feedback voltage V_A-V_B across the op amp input terminals relative to the op amp output voltage V_{OUT}.

$$F = \frac{V_A - V_B}{V_{OUT}} \tag{1}$$

From feedback theory the classic form of the feedback equation for op amps is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + AF} \tag{2}$$

A is the open loop gain of the amplifier and AF is the loop gain. Both are highly important in analyzing op amps. Normally AF >>1 and so the above equation reduces to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{F} \tag{3}$$

Deriving the equations for the lead-lag compensation is beyond the scope of this datasheet. The derivation is based on the feedback equations that have just been covered. The inverse of feedback factor for the circuit in Figure 44 is:

$$\frac{1}{F} = \left(1 + \frac{R_F}{R_{IN}}\right)\left(\frac{1 + s(R_c + R_{IN} \parallel R_F)\, C}{1 + sR_cC}\right) \tag{4}$$

where 1/F's pole is located at

$$f_p = \frac{1}{2\pi R_cC} \tag{5}$$

1/F's zero is located at

$$f_z = \frac{1}{2\pi(R_c + R_{IN} \parallel R_F)C} \tag{6}$$

$$\left.\frac{1}{F}\right|_{f = 0} = 1 + \frac{R_F}{R_{IN}} \tag{7}$$

The circuit gain for Figure 44 at low frequencies is $-R_F/R_{IN}$, but F, the feedback factor is not equal to the circuit gain. The feedback factor is derived from feedback theory and is the same for both inverting and non-inverting configurations. Yes, the feedback factor at low frequencies is equal to the gain for the non-inverting configuration.

$$\left.\frac{1}{F}\right|_{f = \infty} = \left(1 + \frac{R_F}{R_{IN}}\right)\left(1 + \frac{R_{IN} \parallel R_F}{R_C}\right) \tag{8}$$

From this formula, we can see that

- 1/F's zero is located at a lower frequency compared with 1/F's pole.
- 1/F's value at low frequency is $1 + R_F/R_{IN}$.
- This method creates one additional pole and one additional zero.
- This pole-zero pair will serve two purposes:
  - To raise the 1/F value at higher frequencies prior to its intercept with A, the open loop gain curve, in order to meet the G_{min} = 10 requirement. For the LMV793/LMV794 some overcompensation will be necessary for good stability.
  - To achieve the previous purpose above with no additional loop phase delay.

Please note the constraint $1/F \geq G_{min}$ needs to be satisfied only in the vicinity where the open loop gain A and 1/F intersect; 1/F can be shaped elsewhere as needed. The 1/F pole must occur before the intersection with the open loop gain A.

In order to have adequate phase margin, it is desirable to follow these two rules:

1. 1/F and the open loop gain A should intersect at the frequency where there is a minimum of 45° of phase margin. When over-compensation is required the intersection point of A and 1/F is set at a frequency where the phase margin is above 45°, therefore increasing the stability of the circuit.
2. 1/F's pole should be set at least one decade below the intersection with the open loop gain A in order to take advantage of the full 90° of phase lead brought by 1/F's pole which is F's zero. This ensures that the effect of the zero is fully neutralized when the 1/F and A plots intersect each other.

Calculating Lead-Lag Compensation for LMV793/LMV794

Figure 45 is the same plot as Figure 41, but the A_{VOL} and phase curves have been redrawn as smooth lines to more readily show the concepts covered, and to clearly show the key parameters used in the calculations for lead-lag compensation.

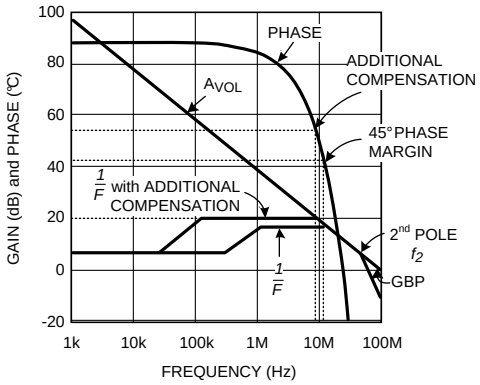


Figure 45. LMV793/LMV794 Simplified Bode Plot

To obtain stable operation with gains under 10 V/V the open loop gain margin must be reduced at high frequencies to where there is a 45° phase margin when the gain margin of the circuit with the external compensation is 0 dB. The pole and zero in F, the feedback factor, control the gain margin at the higher frequencies. The distance between F and A_{VOL} is the gain margin; therefore, the unity gain point (0 dB) is where F crosses the A_{VOL} curve.

For the example being used $R_{IN} = R_F$ for a gain of −1. Therefore F = 6 dB at low frequencies. At the higher frequencies the minimum value for F is 18 dB for 45° phase margin. From *Equation 8* we have the following relationship:

$$\left(1 + \frac{R_F}{R_{IN}}\right)\left(1 + \frac{R_{IN} \parallel R_F}{R_C}\right) = 18 \text{ dB} = 7.9 \tag{9}$$

Now set $R_F = R_{IN} = R$. With these values and solving for R_C we have $R_C = R/5.9$. Note that the value of C does not affect the ratio between the resistors. Once the value of the resistors are set, then the position of the pole in F must be set. A 2 kΩ resistor is used for R_F and R_{IN} in this design. Therefore the value for R_C is set at 330Ω, the closest standard value for 2 kΩ/5.9.

Rewriting *Equation 5* to solve for the minimum capacitor value gives the following equation:

$$C = 1/(2\pi f_p R_C) \tag{10}$$

The feedback factor curve, F, intersects the A_{VOL} curve at about 12 MHz. Therefore the pole of F should not be any larger than 1.2 MHz. Using this value and R_c = 330Ω the minimum value for C is 390 pF. Figure 46 shows that there is too much overshoot, but the part is stable. Increasing C to 2.2 nF did not improve the ringing, as shown in Figure 47.

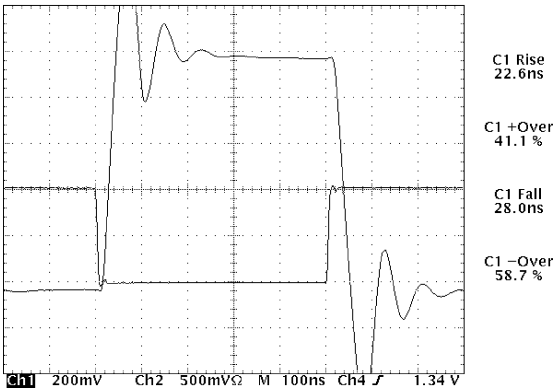


Figure 46. First Try at Compensation, Gain = −1

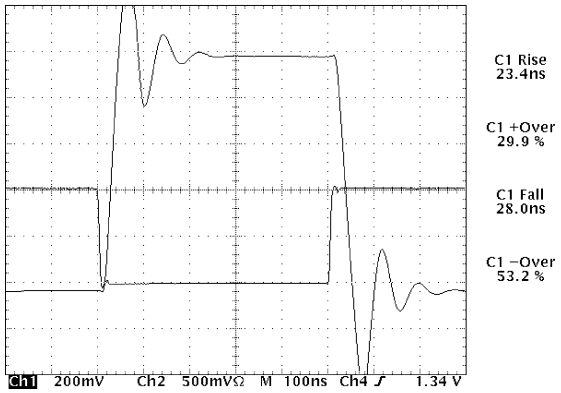


Figure 47. C Increased to 2.2 nF, Gain = −1

Some over-compensation appears to be needed for the desired overshoot characteristics. Instead of intersecting the A_{VOL} curve at 18 dB, 2 dB of over-compensation will be used, and the A_{VOL} curve will be intersected at 20 dB. Using *Equation 8* for 20 dB, or 10 V/V, the closest standard value of R_C is 240Ω. The following two waveforms show the new resistor value with C = 390 pF and 2.2 nF. Figure 49 shows the final compensation and a very good response for the 1 MHz square wave.

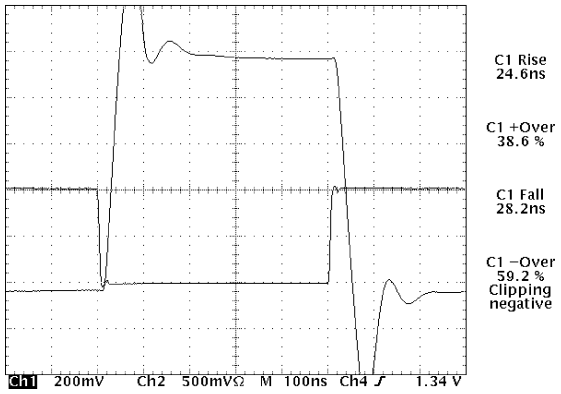


Figure 48. R_C = 240Ω and C = 390 pF, Gain = −1

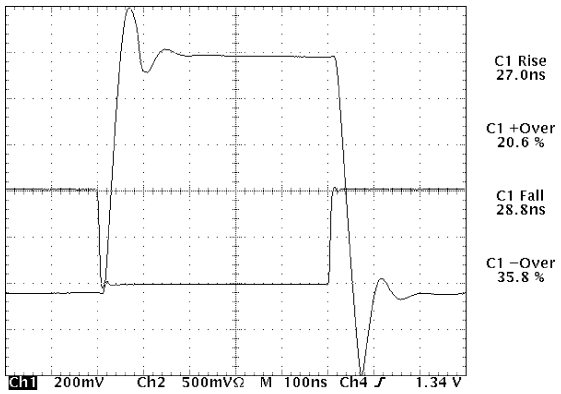


Figure 49. R_C = 240Ω and C = 2.2 nF, Gain = −1

To summarize, the following steps were taken to compensate the LMV793 for a gain of −1:

1. Values for R_c and C were calculated from the Bode plot to give an expected phase margin of 45°. The values were based on $R_{IN} = R_F = 2$ kΩ. These calculations gave $R_c = 330Ω$ and C = 390 pF.
2. To reduce the ringing C was increased to 2.2 nF which moved the pole of F, the feedback factor, farther away from the A_{VOL} curve.
3. There was still too much ringing so 2 dB of over-compensation was added to F. This was done by decreasing R_C to 240Ω.

The LMV796 is the fully compensated part which is comparable to the LMV793. Using the LMV796 in the same setup, but removing the compensation network, provide the response shown in Figure 50 .

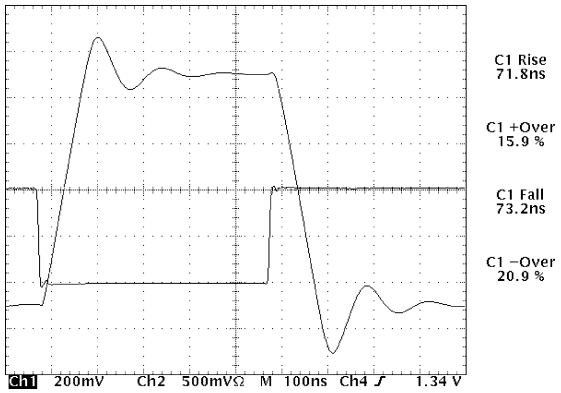


Figure 50. LMV796 Response

For large signal response the rise and fall times are dominated by the slew rate of the op amps. Even though both parts are quite similar the LMV793 will give rise and fall times about 2.5 times faster than the LMV796. This is possible because the LMV793 is a decompensated op amp and even though it is being used at a gain of −1, the speed is preserved by using a good technique for external compensation.

Non-Inverting Compensation

For the non-inverting amp the same theory applies for establishing the needed compensation. When setting the inverting configuration for a gain of −1, F has a value of 2. For the non-inverting configuration both F and the actual gain are the same, making the non-inverting configuration more difficult to compensate. Using the same circuit as shown in Figure 44, but setting up the circuit for non-inverting operation (gain of +2) results in similar performance as the inverting configuration with the inputs set to half the amplitude to compensate for the additional gain. Figure 51 below shows the results.

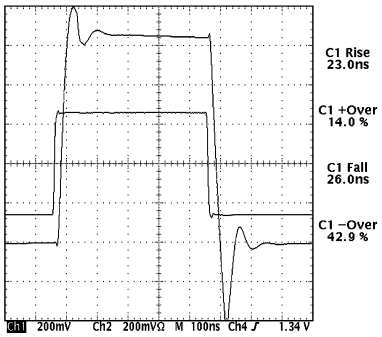


Figure 51. R_C = 240Ω and C = 2.2 nF, Gain = +2

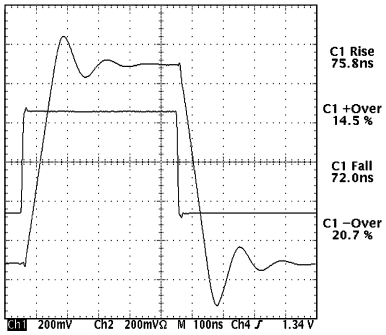


Figure 52. LMV796 Response Gain = +2

The response shown in Figure 51 is close to the response shown in Figure 49. The part is actually slightly faster in the non-inverting configuration. Decreasing the value of R_C to around 200Ω can decrease the negative overshoot but will have slightly longer rise and fall times. The other option is to add a small resistor in series with the input signal. Figure 52 shows the performance of the LMV796 with no compensation. Again the decompensated parts are almost 2.5 times faster than the fully compensated op amp.

The most difficult op amp configuration to stabilize is the gain of +1. With proper compensation the LMV793/LMV794 can be used in this configuration and still maintain higher speeds than the fully compensated parts. Figure 53 shows the gain = 1, or the buffer configuration, for these parts.

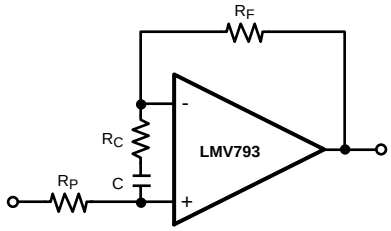


Figure 53. LMV793 with Lead-Lag Compensation for Non-Inverting Configuration

Figure 53 is the result of using *Equation 8* and additional experimentation in the lab. R_P is not part of *Equation 8*, but it is necessary to introduce another pole at the input stage for good performance at gain = +1. *Equation 8* is shown below with $R_{IN} = \infty$.

$$\left(1 + \frac{R_F}{R_c}\right) = 18 \text{ dB} = 7.9 \tag{11}$$

Using 2 kΩ for R_F and solving for R_C gives R_C = 2000/6.9 = 290Ω. The closest standard value for R_C is 300Ω. After some fine tuning in the lab R_C = 330Ω and R_P = 1.5 kΩ were choosen as the optimum values. R_P together with the input capacitance at the non-inverting pin inserts another pole into the compensation for the LMV793/LMV794. Adding this pole and slightly reducing the compensation for 1/F (using a slightly higher resistor value for R_C) gives the optimum response for a gain of +1. Figure 54 is the response of the circuit shown in Figure 53. Figure 55 shows the response of the LMV796 in the buffer configuration with no compensation and $R_P = R_F = 0$.

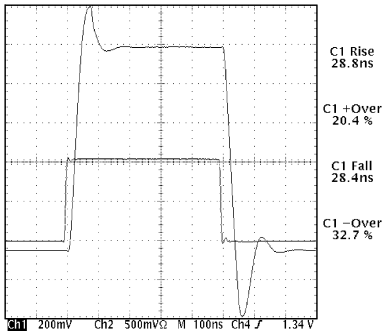


Figure 54. R_C = 330Ω and C = 10 nF, Gain = +1

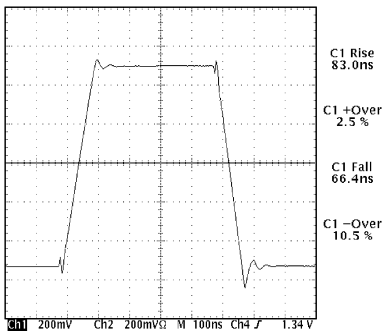


Figure 55. LMV796 Response Gain = +1

With no increase in power consumption the decompensated op amp offers faster speed over the compensated equivalent part. These examples used R_F = 2 kΩ. This value is high enough to be easily driven by the LMV793/LMV794, yet small enough to minimize the effects from the parasitic capacitance of both the PCB and the op amp.

Note: When using the LMV793/LMV794, proper high frequency PCB layout must be followed. The GBW of these parts is 88 MHz, making the PCB layout significantly more critical than when using the compensated counterparts which have a GBW of 17 MHz.

TRANSIMPEDANCE AMPLIFIER

An excellent application for either the LMV793 or the LMV794 is as a transimpedance amplifier. With a GBW product of 88 MHz these parts are ideal for high speed data transmission by light. The circuit shown on the front page of the datasheet is the circuit used to test the LMV793/LMV794 as transimpedance amplifiers. The only change is that VB is tied to the V_{CC} of the part, thus the direction of the diode is reversed from the circuit shown on the front page.

Very high speed components were used in testing to check the limits of the LMV793/LMV794 in a transimpedance configuration. The photo diode part number is PIN-HR040 from OSI Optoelectronics. The diode capacitance for this part is only about 7 pF for the 2.5V bias used (V_{CC} to virtual ground). The rise time for this diode is 1 nsec. A laser diode was used for the light source. Laser diodes have on and off times under 5 nsec. The speed of the selected optical components allowed an accurate evaluation of the LMV793 as a transimpedance amplifier. TIs Evaluation Board for decompensated op amps, PN 551013271-001 A, was used and only minor modifications were necessary and no traces had to be cut.

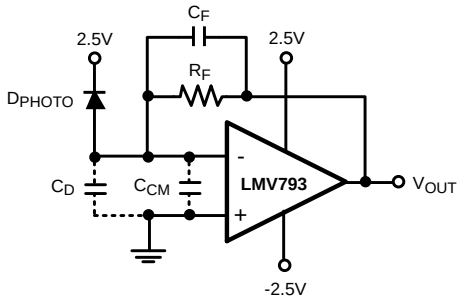


Figure 56. Transimpedance Amplifier

Figure 56 is the complete schematic for a transimpedance amplifier. Only the supply bypass capacitors are not shown. C_D represents the photo diode capacitance which is given on its datasheet. C_{CM} is the input common mode capacitance of the op amp and, for the LMV793 it is shown in the last drawing of the Typical Performance Characteristics section of this datasheet. In Figure 56 the inverting input pin of the LMV793 is kept at virtual ground. Even though the diode is connected to the 2.5V line, a power supply line is AC ground, thus C_D is connected to ground.

Figure 57 shows the schematic needed to derive F, the feedback factor, for a transimpedance amplifier. In this figure $C_D + C_{CM} = C_{IN}$. Therefore it is critical that the designer knows the diode capacitance and the op amp input capacitance. The photo diode is close to an ideal current source once its capacitance is included in the model. What kind of circuit is this? Without C_F there is only an input capacitor and a feedback resistor. This circuit is a differentiator! Remember, differentiator circuits are inherently unstable and must be compensated. In this case C_F compensates the circuit.

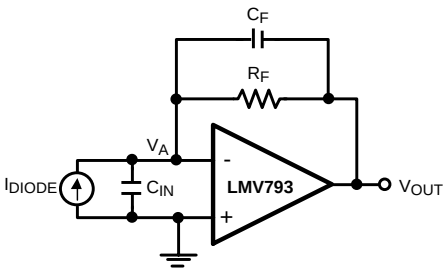


Figure 57. Transimpedance Feedback Model

Using feedback theory, $F = V_A/V_{OUT}$, this becomes a voltage divider giving the following equation:

$$F = \frac{1 + sC_FR_F}{1 + sR_F(C_F + C_{IN})} \tag{12}$$

The noise gain is 1/F. Because this is a differentiator circuit, a zero must be inserted. The location of the zero is given by:

$$f_z = \frac{1}{1 + sR_F(C_F + C_{IN})} \tag{13}$$

C_F has been added for stability. The addition of this part adds a pole to the circuit. The pole is located at:

$$f_p = \frac{1}{1 + sC_FR_F} \tag{14}$$

To attain maximum bandwidth and still have good stability the pole is to be located on the open loop gain curve which is A. If additional compensation is required one can always increase the value of C_F, but this will also reduce the bandwidth of the circuit. Therefore A = 1/F, or AF = 1. For A the equation is:

$$A = \frac{\omega_{GBW}}{\omega} = \frac{f_{GBW}}{f} \tag{15}$$

The expression f_{GBW} is the gain bandwidth product of the part. For a unity gain stable part this is the frequency where A = 1. For the LMV793 f_{GBW} = 88 MHz. Multiplying A and F results in the following equation:

$$AF\Big|_{f_P} = \frac{f_{GBW}}{f} \times \frac{1 + sC_FR_F}{1 + sR_F(C_F + C_{IN})} =$$

$$\frac{f_{GBW}}{f} \times \frac{\sqrt{1 + \left(\frac{C_FR_F}{C_FR_F}\right)^2}}{\sqrt{1 + \left(\frac{R_F(C_F + C_{IN})}{C_FR_F}\right)^2}} = 1 \tag{16}$$

For the above equation s = jω. To find the actual amplitude of the equation the square root of the square of the real and imaginary parts are calculated. At the intersection of F and A, we have:

$$\omega = \frac{1}{C_FR_F} \tag{17}$$

After a bit of algebraic manipulation the above equation reduces to:

$$1 + \left(\frac{C_F + C_{IN}}{C_F}\right)^2 = 8\pi^2 f_{GBW}^2 R_F^2 C_F^2 \tag{18}$$

In the above equation the only unknown is C_F. In trying to solve this equation the fourth power of C_F must be dealt with. An excel spread sheet with this equation can be used and all the known values entered. Then through iteration, the value of C_F when both sides are equal will be found. That is the correct value for C_F, and of course the closest standard value is used for C_F.

Before moving the lab, the transfer function of the transimpedance amplifier must be found and the units must be in Ohms.

$$V_{OUT} = \frac{-R_F}{1 + sC_FR_F} \times I_{DIODE} \tag{19}$$

The LMV793 was evaluated for R_F = 10 kΩ and 100 kΩ, representing a somewhat lower gain configuration and with the 100 kΩ feedback resistor a fairly high gain configuration. The R_F = 10 kΩ is covered first. Looking at the Figure 39 chart for C_{CM} for the operating point selected C_{CM} = 15 pF. Note that for split supplies V_{CM} = 2.5V, C_{IN} = 22 pF and f_{GBW} = 88 MHz. Solving for C_F the calculated value is 1.75 pF, so 1.8 pF is selected for use. Checking the frequency of the pole finds that it is at 8.8 MHz, which is right at the minimum gain recommended for this part. Some over compensation was necessary for stability and the final selected value for C_F is 2.7 pF. This moves the pole to 5.9 MHz. Figure 58 and Figure 59 show the rise and fall times obtained in the lab with a 1V output swing. The laser diode was difficult to drive due to thermal effects making the starting and ending point of the pulse quite different, therefore the two separate scope pictures.

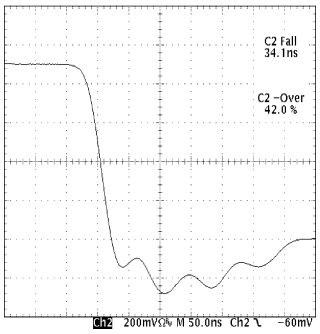


Figure 58. Fall Time

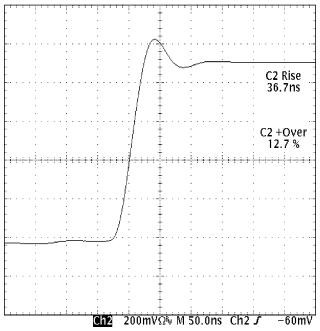


Figure 59. Rise Time

In Figure 58 the ringing and the hump during the on time is from the laser. The higher drive levels for the laser gave ringing in the light source as well as light changing from the thermal characteristics. The hump is due to the thermal characteristics.

Solving for C_F using a 100 kΩ feedback resistor, the calculated value is 0.54 pF. One of the problems with more gain is the very small value for C_F. A 0.5 pF capacitor was used, its measured value being 0.64 pF. For the 0.64 pF location the pole is at 2.5 MHz. Figure 60 shows the response for a 1V output.

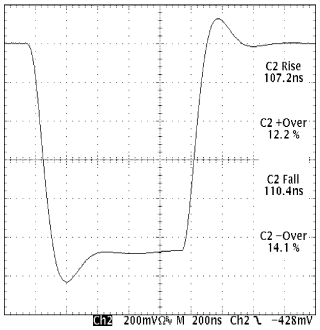


Figure 60. High Gain Response

A transimpedance amplifier is an excellent application for the LMV793. Even with the high gain using a 100 kΩ feedback resistor, the bandwidth is still well over 1 MHz. Other than a little over compensation for the 10 kΩ feedback resistor configuration using the LMV793 was quite easy. Of course a very good board layout was also used for this test. For information on photo diodes please contact OSI Optoelectronics, (310) 978-0516. For further information on transimpedance amplifiers please contact your Texas Instruments representative.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	23

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMV793MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 93MA
LMV793MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 93MA
LMV793MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 93MA
LMV793MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 93MA
LMV793MF/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AS4A
LMV793MF/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AS4A
LMV793MFX/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AS4A
LMV793MFX/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AS4A
LMV794MA/NOPB	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 94MA
LMV794MA/NOPB.A	Active	Production	SOIC (D) | 8	95 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 94MA
LMV794MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 94MA
LMV794MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LMV7 94MA
LMV794MM/NOPB	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN4A
LMV794MM/NOPB.A	Active	Production	VSSOP (DGK) | 8	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN4A
LMV794MMX/NOPB	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN4A
LMV794MMX/NOPB.A	Active	Production	VSSOP (DGK) | 8	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	AN4A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

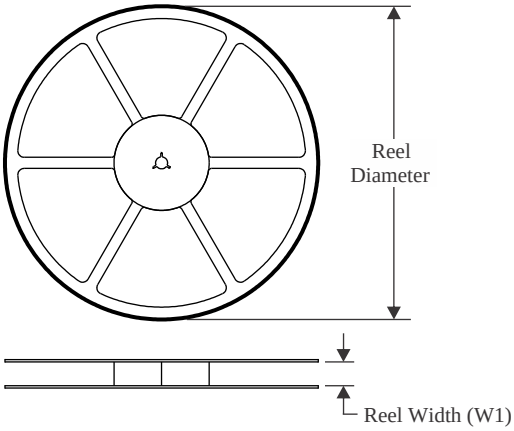
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

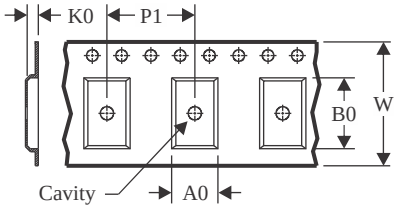
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

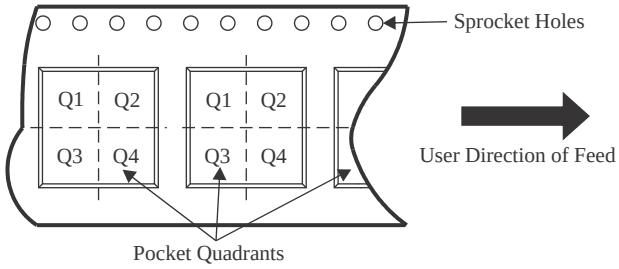


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

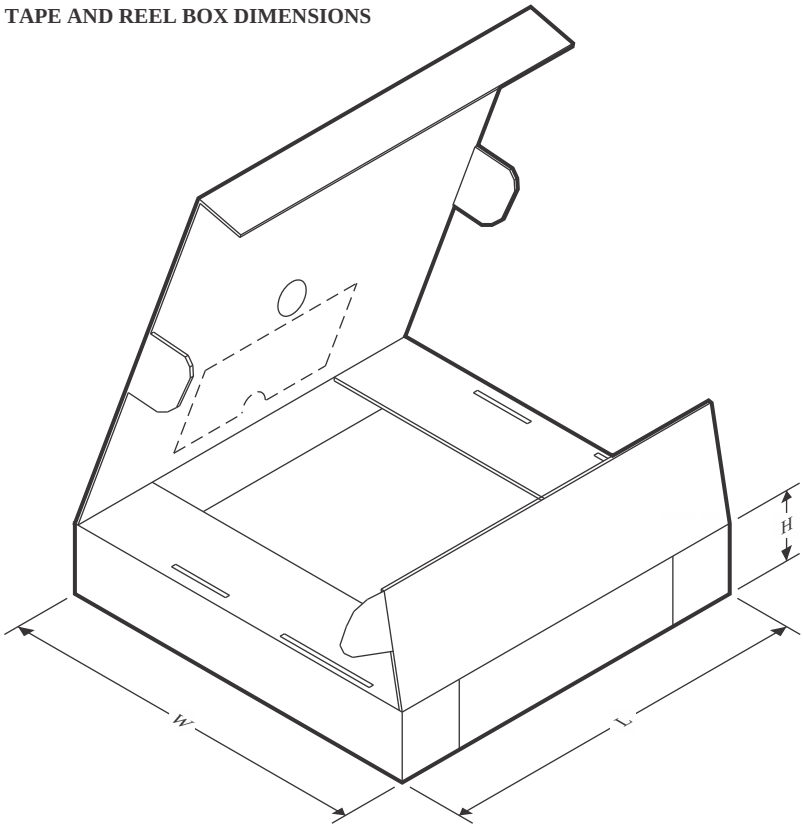
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV793MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV793MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV793MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV794MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV794MM/NOPB	VSSOP	DGK	8	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV794MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

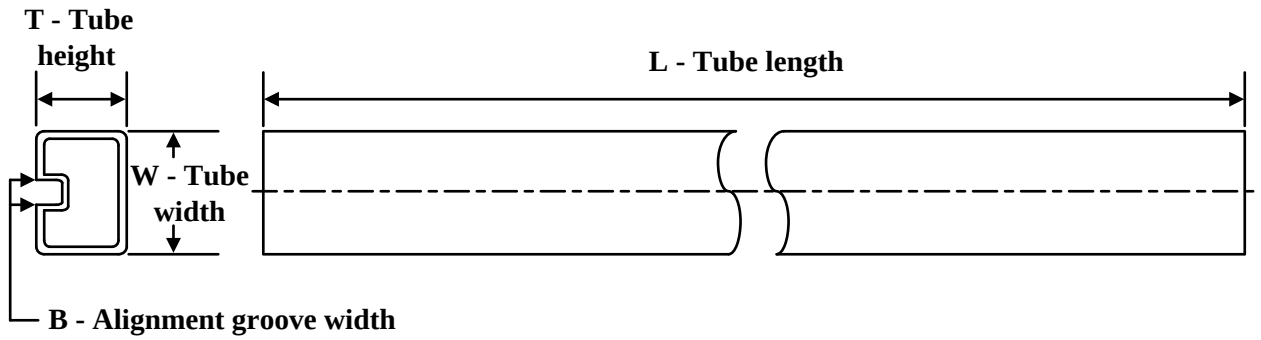
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

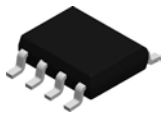
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV793MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV793MF/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LMV793MFX/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LMV794MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV794MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMV794MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMV793MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV793MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05
LMV794MA/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMV794MA/NOPB.A	D	SOIC	8	95	495	8	4064	3.05

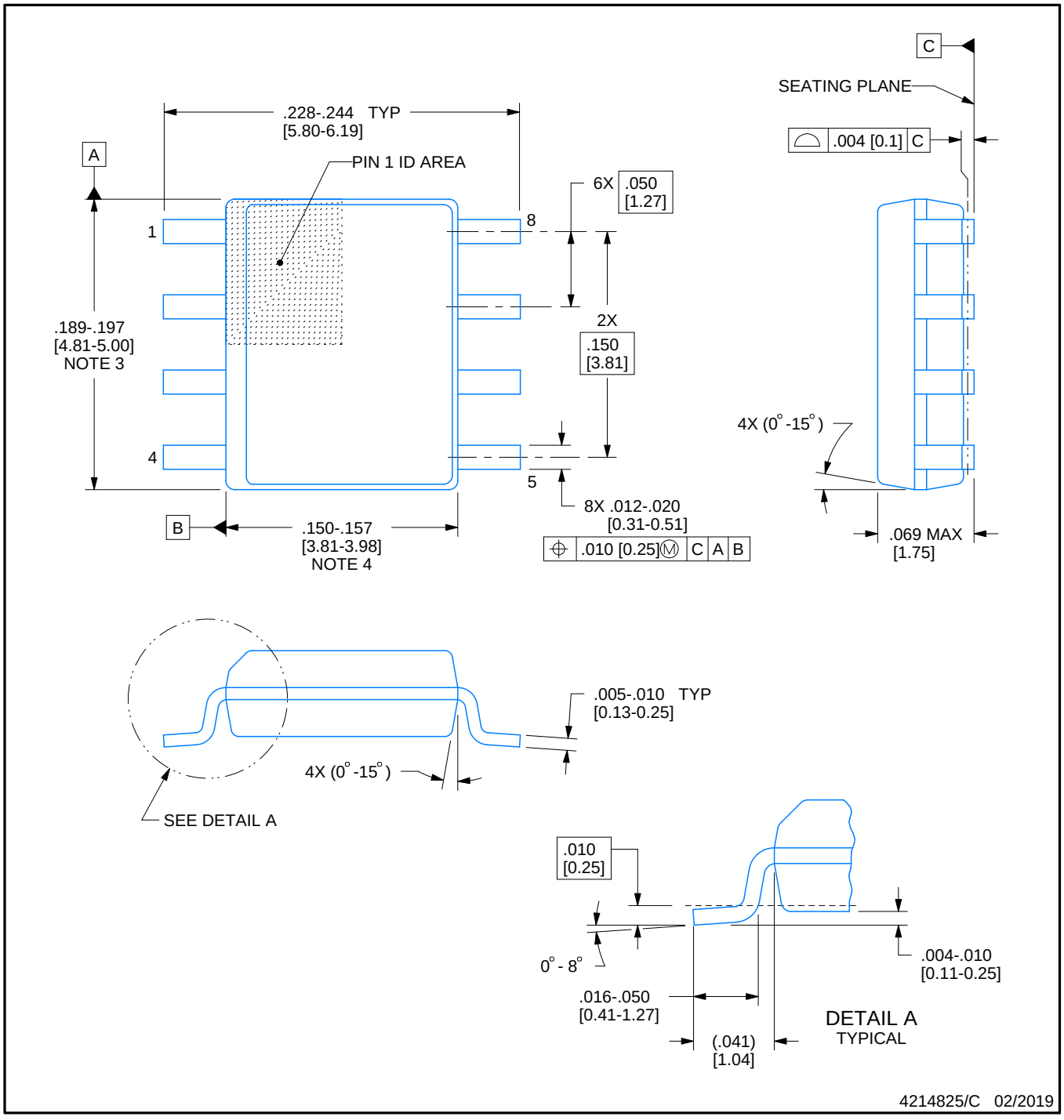


PACKAGE OUTLINE

D0008A

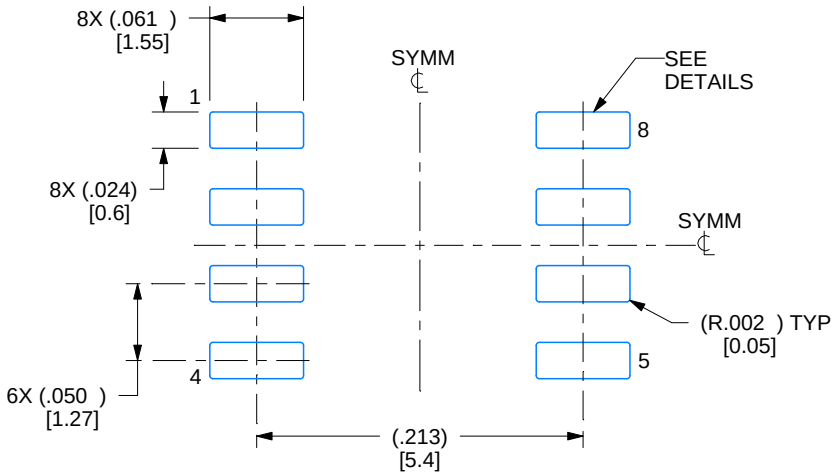
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

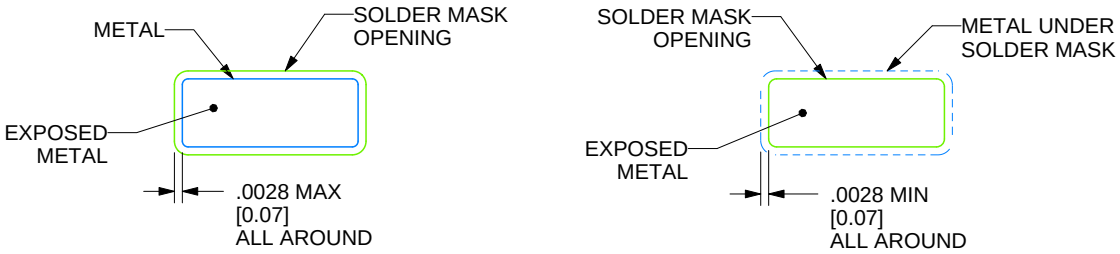


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

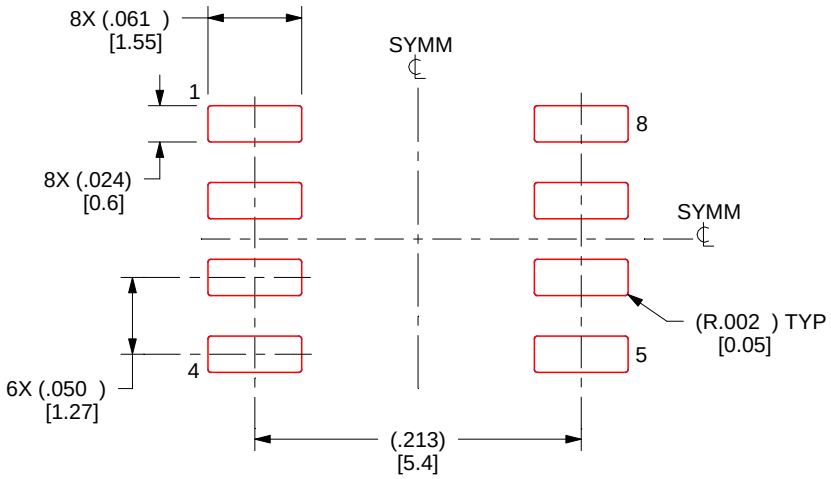
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

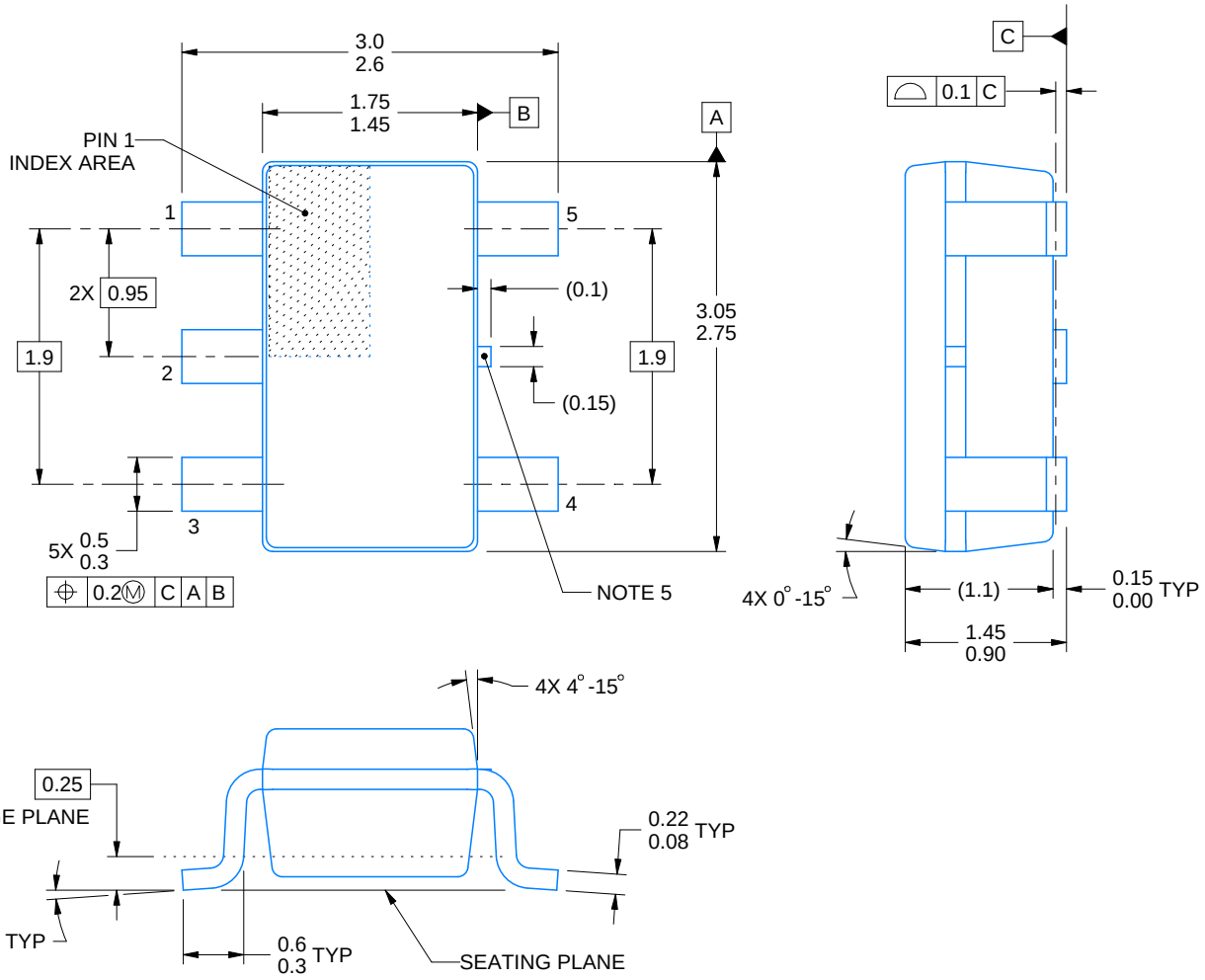
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

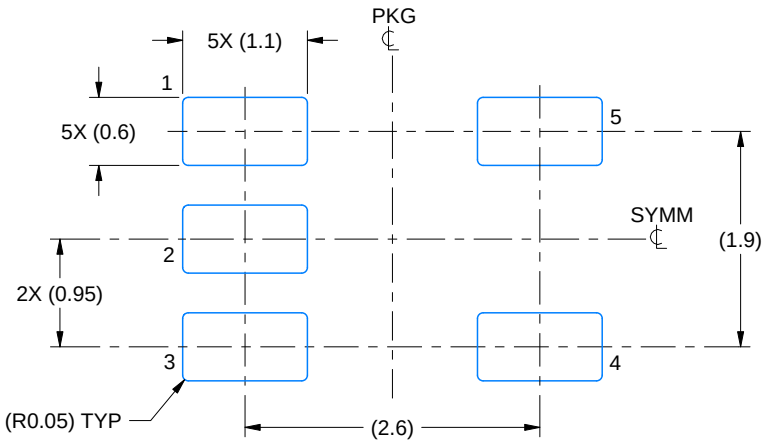
SMALL OUTLINE TRANSISTOR



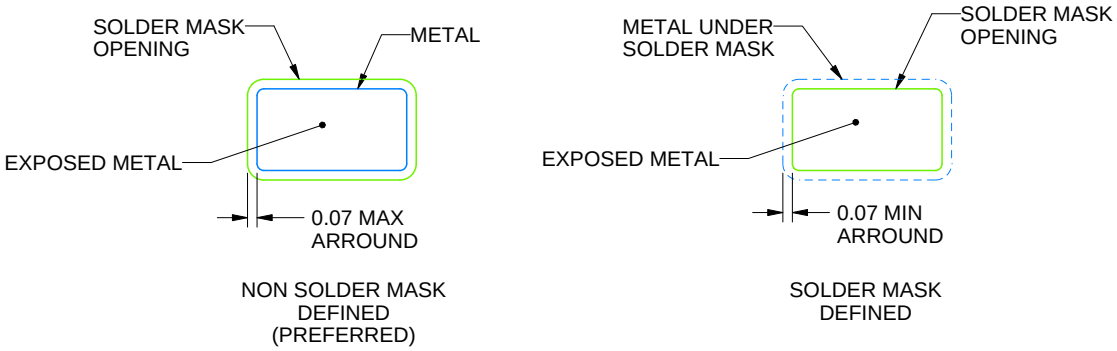
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

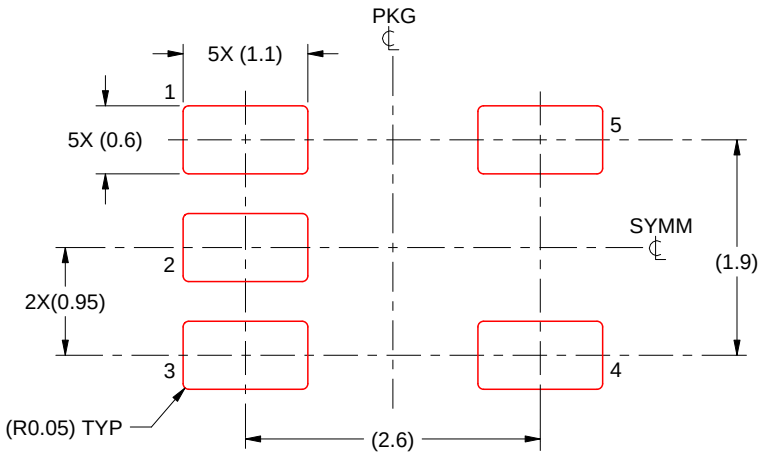


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

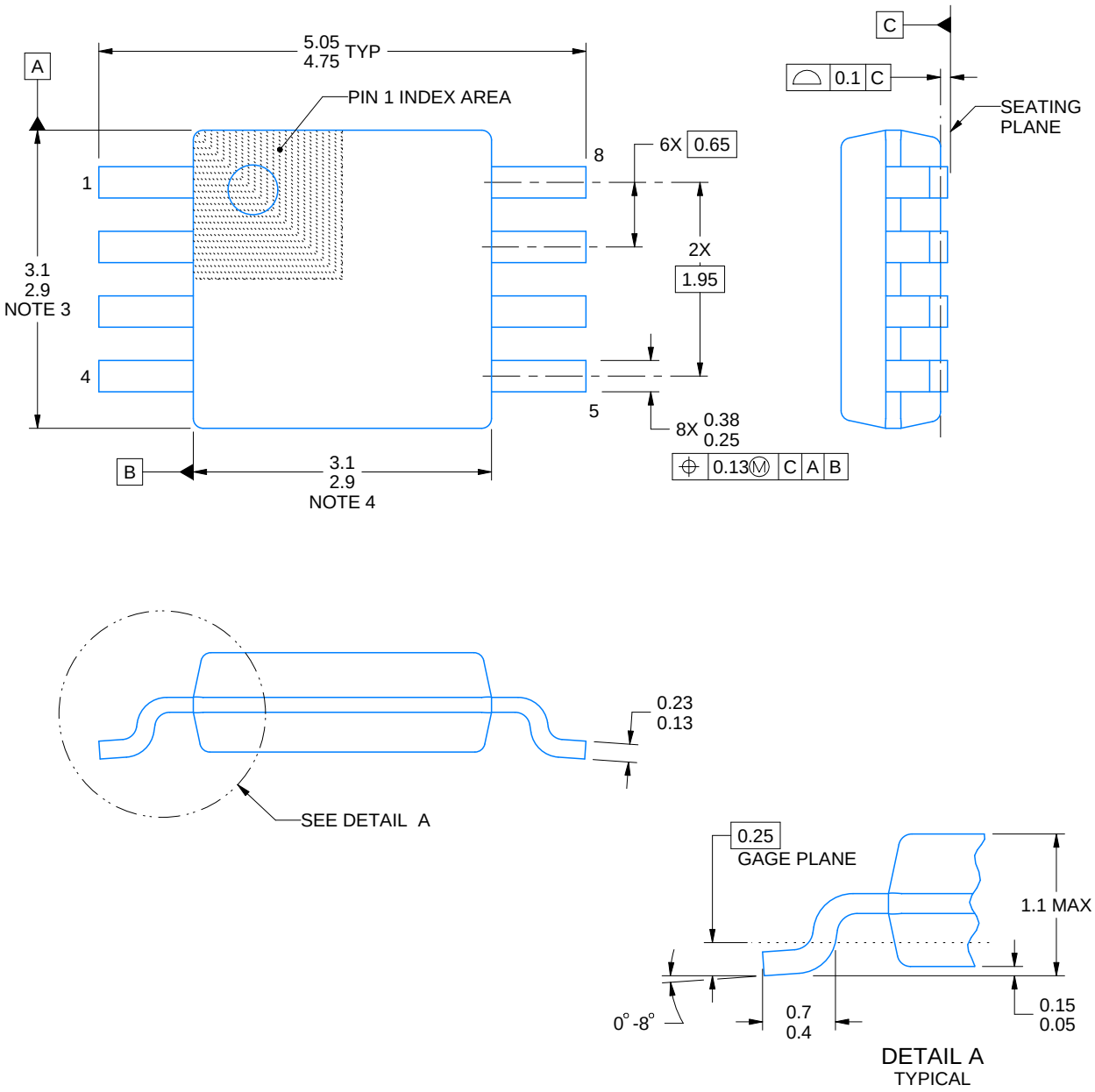
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

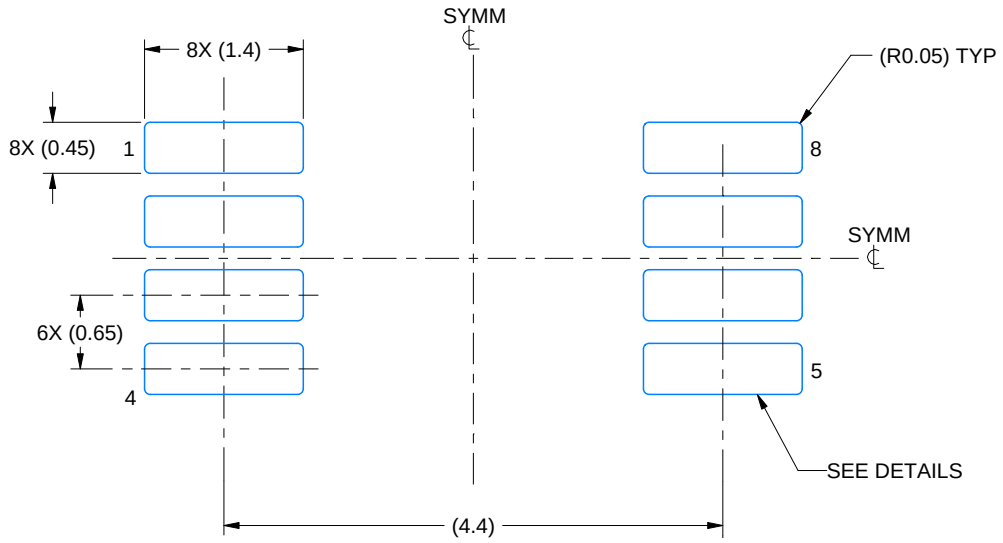
SMALL OUTLINE PACKAGE



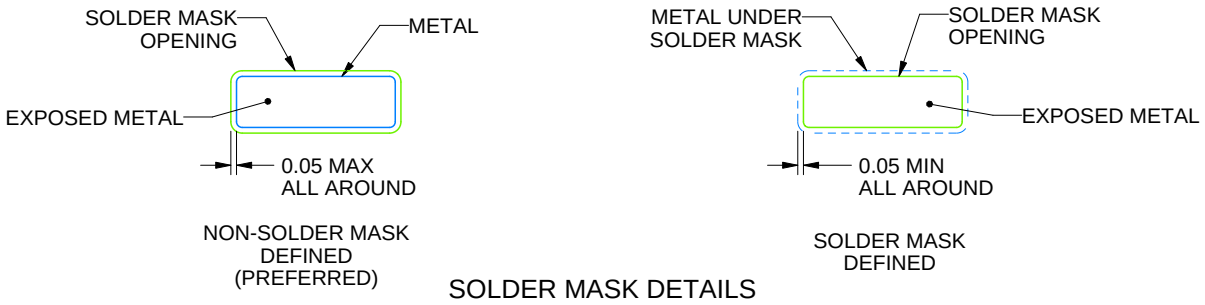
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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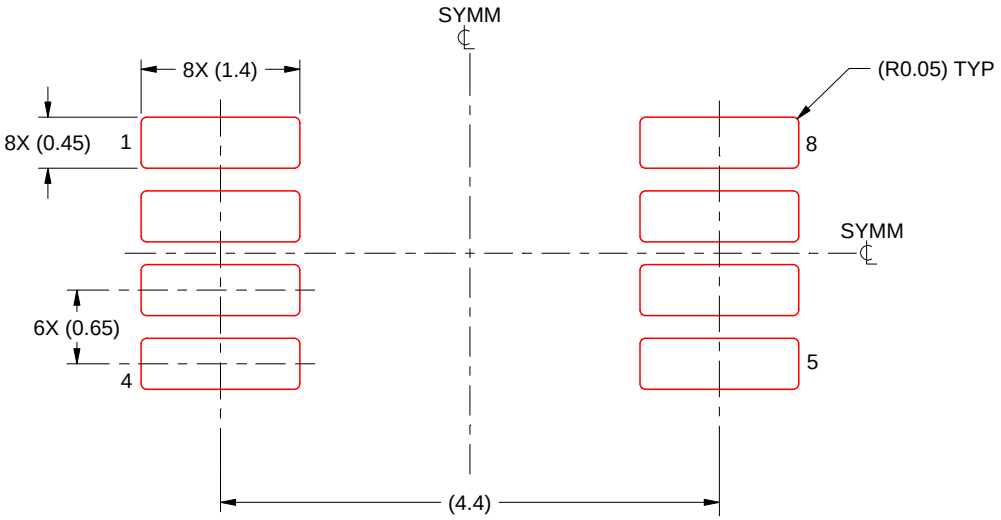
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265