TQP7M9101

¼ W High Linearity Amplifier

Applications

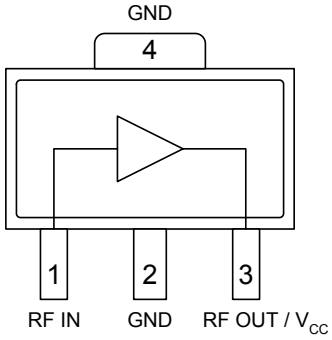
- Repeaters
- Mobile Infrastructure
- CDMA / WCDMA / LTE
- General Purpose Wireless

3 Pin SOT-89 Package

Product Features

- 400-4000 MHz
- +25 dBm P1dB
- +39.5 dBm Output IP3
- 17.5 dB Gain at 2140 MHz
- +5V Single Supply, 87 mA Current
- No output matching required
- Internal RF overdrive protection
- Internal DC overvoltage protection
- On chip ESD protection
- SOT-89 Package

Functional Block Diagram



General Description

The TQP7M9101 is a high-linearity driver amplifier in a standard SOT-89 surface mount package. This InGaP/GaAs HBT delivers high performance across a broad range of frequencies with +40 dBm OIP3 and with +25 dBm P1dB while only consuming 87 mA quiescent current. All devices are 100% RF and DC tested.

The TQP7M9101 incorporates on-chip features that differentiate it from other products in the market. The RF output is internally matched in to 50 ohms. Only input matching is required for optimal performance in specific frequency bands making the component easy for design engineers to implement in their systems. The amplifier integrates an on-chip DC over-voltage and RF over-drive protection. This protects the amplifier from electrical DC voltage surges and high input RF input power levels that may occur in a system. On-chip ESD protection allows the amplifier to have a very robust Class 2 HBM ESD rating.

The TQP7M9101 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. The device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G / 4G base stations.

Pin Configuration

Pin No.	Label
1	RF IN
3	RF OUT / V_{CC}
2, 4	GND

Ordering Information

Part No.	Description
TQP7M9101	¼ W High Linearity Amplifier
TQP7M9101-PCB900	869-960 MHz Evaluation Board
TQP7M9101-PCB2140	2.11-2.17 GHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel

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Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150°C
RF Input Power, CW, 50Ω, T=25°C	+23 dBm
Device Voltage (V_{CC})	+8 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{CC})	+3	+5	+5.25	V
T_{CASE}	-40		+85	°C
Tj for >10^6 hours MTTF			+170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC} =+5V, Temp= +25°C, matched 2140 MHz reference circuit

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		400		4000	MHz
Test Frequency			2140		MHz
Gain		15.6	17.5	18.6	dB
Input Return Loss			15		dB
Output Return Loss			13.5		dB
Output P1dB		+23.5	+25		dBm
Output IP3	Pout = +8 dBm/tone, Δf = 1 MHz	+36.5	+39.5		dBm
WCDMA Channel Power[1]	−55 dBc ACLR		+14.5		dBm
Noise Figure			3.9		dB
Device Voltage, V_{CC}			5		V
Quiescent Current, I_{CQ}	See Note 1	70	87	105	mA
Thermal Resistance, θ_{jc}	Junction to case			71	°C/W

Notes:
1. ACLR test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

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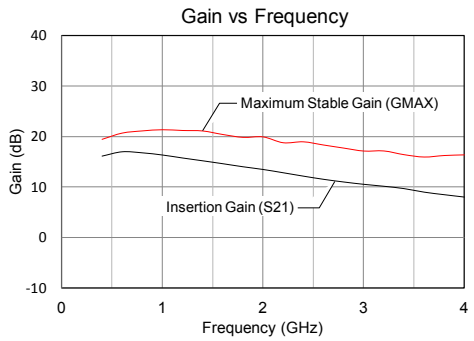
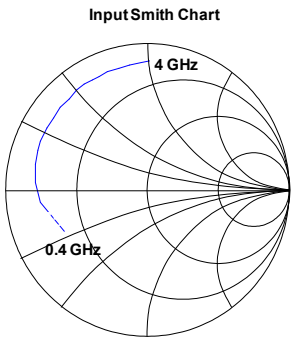
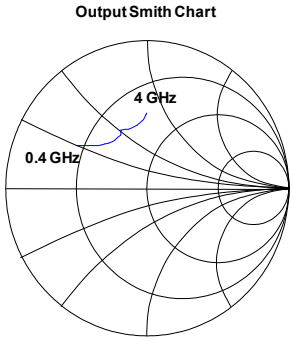
Device Characterization Data







Note: The gain for the unmatched device in a 50 ohm system is shown as the black trace labeled "Insertion Gain (S21)". In a circuit tuned for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown as the red trace [Gmax]. The impedance Smith chart plots are shown from 0.05 to 4 GHz.

S-Parameters

Test Conditions: V_{CC} = +5 V, I_{CQ} = 87 mA, T = +25°C, unmatched 50 Ohm system, reference plane at device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
400	-3.74	-154.94	16.08	172.65	-30.84	32.65	-4.47	155.03
600	-2.43	-174.00	16.93	152.42	-28.85	13.25	-6.02	149.89
800	-2.00	175.84	16.72	137.72	-28.64	3.42	-6.63	147.55
1000	-1.81	167.43	16.29	123.90	-28.38	-4.74	-7.05	144.48
1200	-1.71	160.50	15.71	112.48	-28.45	-10.23	-7.29	142.81
1400	-1.68	155.82	15.15	102.29	-28.29	-15.72	-7.67	139.67
1600	-1.66	149.16	14.58	91.96	-28.34	-19.66	-7.92	136.04
1800	-1.65	143.36	13.98	82.32	-28.40	-25.64	-8.05	132.86
2000	-1.56	137.28	13.45	72.43	-28.25	-30.76	-8.05	129.68
2200	-1.60	131.41	12.80	64.37	-28.52	-35.06	-7.96	125.67
2400	-1.43	126.29	12.14	56.45	-28.43	-39.47	-7.47	122.90
2600	-1.41	122.01	11.52	48.81	-28.73	-42.87	-7.49	122.21
2800	-1.43	117.57	10.99	41.39	-28.68	-47.17	-7.71	119.34
3000	-1.45	114.12	10.53	34.73	-28.78	-49.96	-7.92	116.57
3200	-1.36	109.38	10.15	27.42	-28.85	-52.90	-7.87	114.37
3400	-1.40	103.72	9.69	19.90	-29.00	-59.40	-7.85	106.77
3600	-1.32	98.51	8.99	12.40	-29.04	-63.10	-7.32	100.14
3800	-1.19	93.06	8.49	5.24	-29.04	-68.03	-6.75	96.77
4000	-1.11	89.37	8.02	-0.57	-29.02	-70.86	-6.53	95.94

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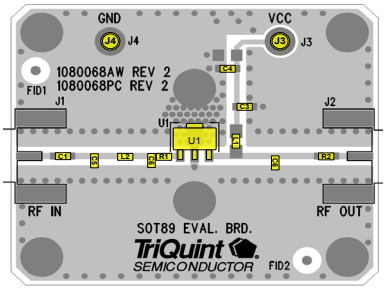
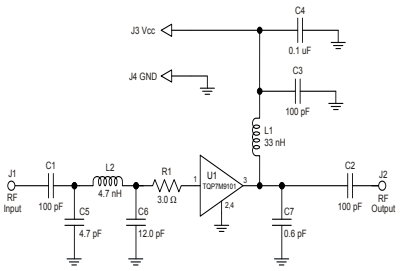
Reference Design − 700-1000 MHz





Notes:
1. See Evaluation Board PCB Information section for PCB material and stack-up
2. All components are 0603 size unless otherwise specified.
3. Critical component placement locations:
   Distance from U1 Pin 1 Pad (left edge) to R1 (right edge): 10 mils (0.5° at 900 MHz)
   Distance from R1 (left edge) to C6 (right edge): 5 mils (0.2° at 900 MHz)
   Distance from C6 (left edge) to L2 (right edge): 60 mils (2.8° at 900 MHz)
   Distance from L2 (left edge) to C5 (left edge): 60 mils (2.8° at 900 MHz)
   Distance from U1 Pin 3 Pad (right edge) to C7 (left edge): 250 mils (11.7° at 900 MHz)

Typical Performance − 700-1000 MHz

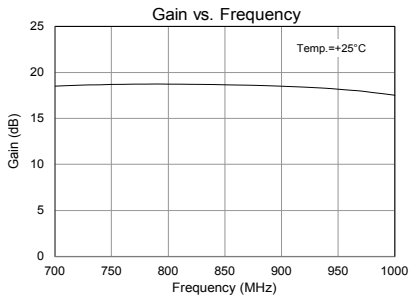
Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

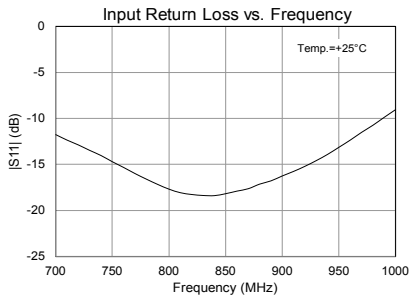
Parameter		Typical Value					
Frequency (MHz)		700	800	850	900	960	MHz
Gain		18.5	18.7	18.6	18.5	18.2	dB
Input Return Loss		11.8	17.7	18.2	16.2	13.1	dB
Output Return Loss		12.8	19.1	22.9	32.7	23.7	dB
Output P1dB		+24.1	+24.2	+24.4	+24.4	+24.6	dBm
Output IP3	Pout=+8 dBm/tone, Δf = 1 MHz	+39.6	+40.4	+41.2	+39.7	+39.8	dBm
WCDMA Chan. Power(1)	−55 dBc ACLR	+12.8	+13.2	+13.5	+14.0	+14.0	dBm
Noise Figure		5.0	5.0	5.1	5.2	5.9	dB

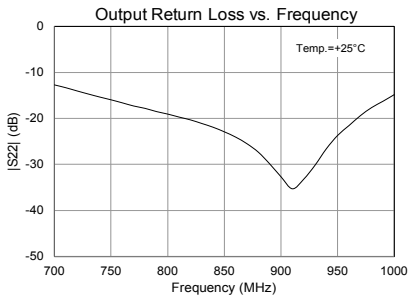
Notes:
1. ACLR test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

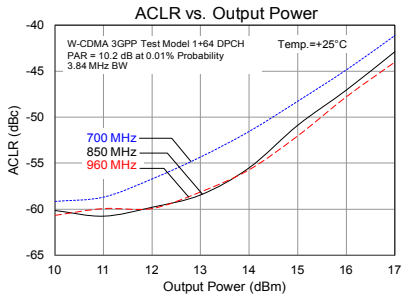
Performance Plots − 700-1000 MHz

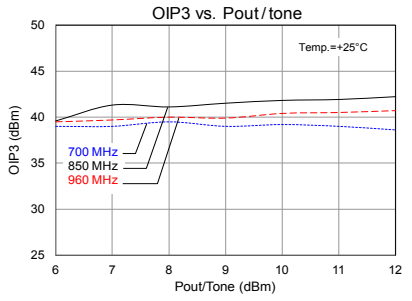
Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

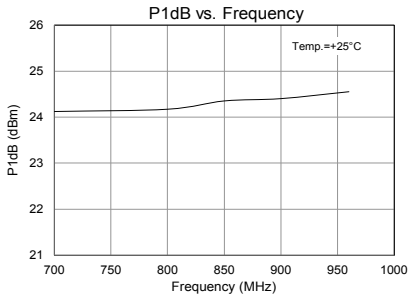












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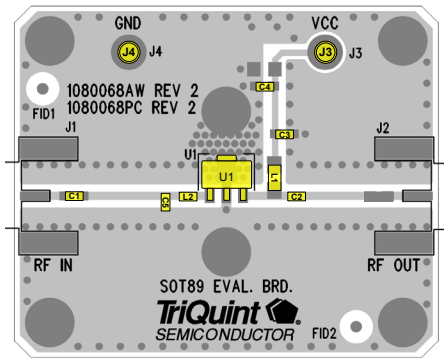
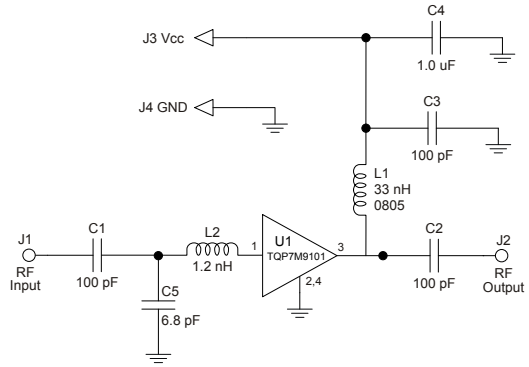
TQP7M9101-PCB900 Evaluation Board





Notes:
1. See Evaluation Board PCB Information section for PCB material and stack-up
2. Component (C2) is a blocking capacitor and its location is not critical to the matching network.
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement locations:
   Distance from U1 Pin 1 Pad (left edge) to L2 (right edge): 30 mils (1.6° at 920 MHz)
   Distance from L2 (left edge) to C5 (right edge): 40 mils (2.1° at 920 MHz)

Bill of Material – TQP7M9101-PCB900

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	TriQuint	1080068
U1	n/a	Amplifier, SOT-89 pkg.	TriQuint	TQP7M9101
L1	33 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-330XJLB
L2	1.2 nH	Inductor, Chip, 0603	various	
C1, C2, C3	100 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	
C5	6.8 pF	Cap., Chip, +/-0.1pF. 200V NPO/COG	AVX	
J1, J2	n/a	RF SMA Connector	Johnson	142-0701-851
J3, J4	n/a	Solder Turret	various	

Typical Performance – TQP7M9101-PCB900

Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

Parameter	Conditions	Typical Value			Units
Frequency		869	920	960	MHz
Gain		20.2	20.4	20.1	dB
Input Return Loss		12	17	14	dB
Output Return Loss		18	23	17	dB
Output P1dB		+24.3	+24.4	+24.4	dBm
OIP3	Pout= +8 dBm/tone, Δf=1 MHz	+39.2	+38.6	+38.2	dBm
WCDMA Channel Power(1)	−55 dBc ACLR	+12.7	+13.4	+13.5	dBm
Noise Figure		4.0	4.0	3.9	dB

Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

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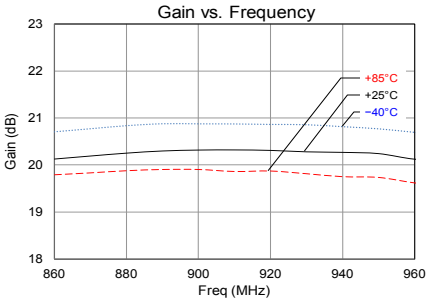
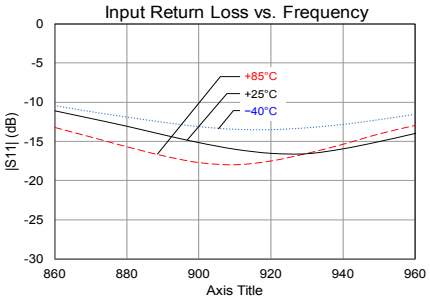
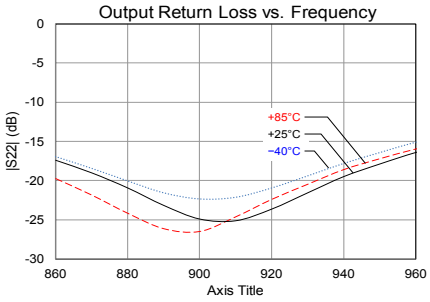
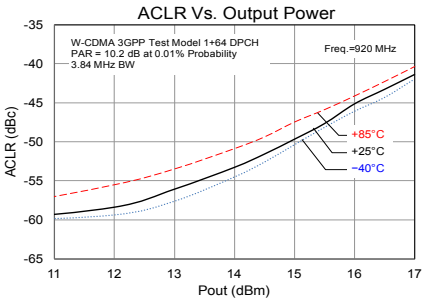
Performance Plots – TQP7M9101-PCB900

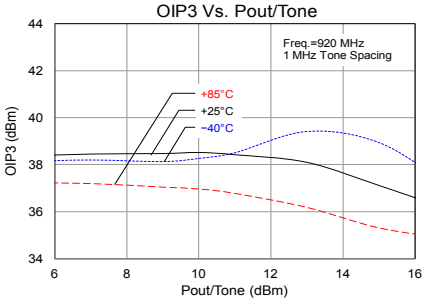
Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

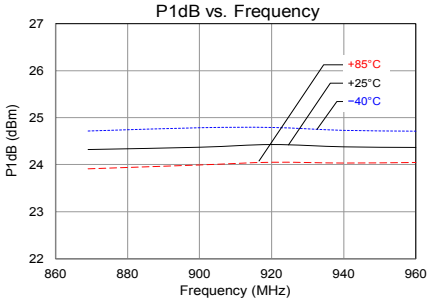


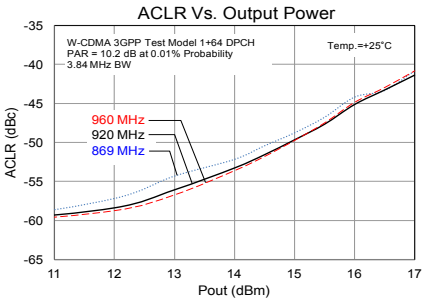


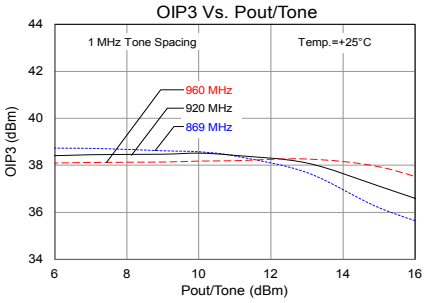


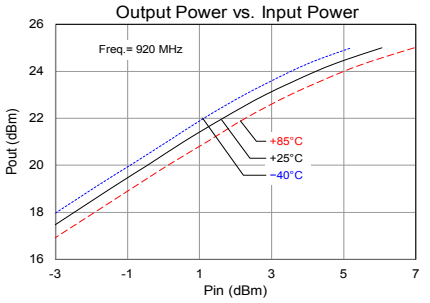


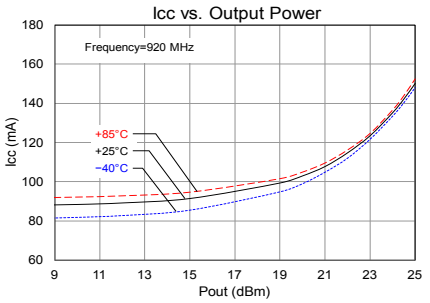












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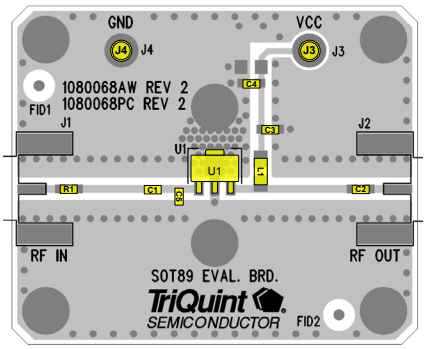
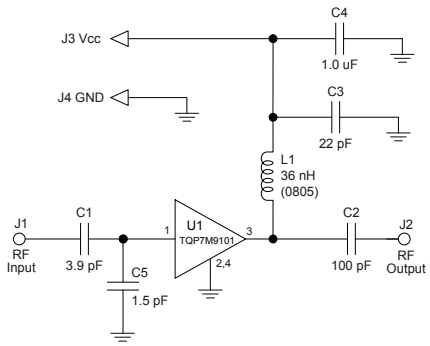
Reference Design − 1805-1990 MHz





Notes:
1. See Evaluation Board PCB Information section for PCB material and stack-up.
2. Component R1 on the PCB is a (0 Ω) Resistor and may be replaced by a copper trace
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement:
   Distance from U1 Pin 1 Pad (left edge) to C5 (right edge): 35 mils (3.5° at 1900 MHz)
   Distance from C5 (left edge) to C1 (right edge): 45 mils (4.5° at 1900 MHz)

Typical Performance − 1805-1990 MHz

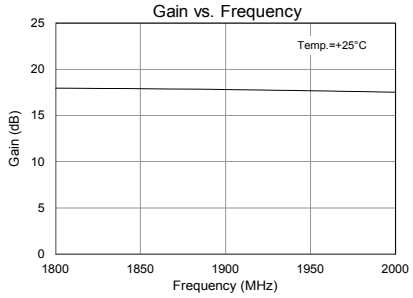
Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

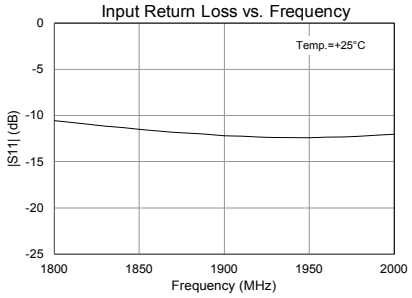
Parameter		Typical Value						Units
Frequency (MHz)		1805	1850	1880	1930	1960	1990	MHz
Gain		18.0	17.9	17.9	17.7	17.7	17.6	dB
Input Return Loss		10.7	11.5	11.9	12.4	12.4	12.2	dB
Output Return Loss		15.8	14.9	14.2	13.4	13.1	12.8	dB
Output P1dB		+25.0	+25.1	+25.1	+25.1	+25.1	+25.1	dBm
Output IP3	+8 dBm/tone, Δf = 1 MHz	+39.7	+39.6	+39.5	+39.2	+38.7	+39.1	dBm
WCDMA Channel Power(1)	−55 dBc ACLR	+14.5	+14.5	+14.4	+14.3	+14.0	+14.1	dBm

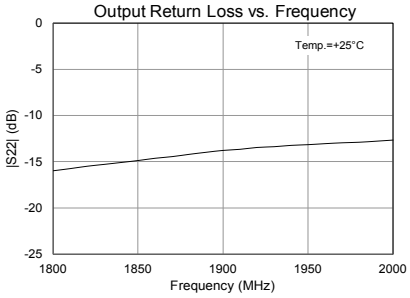
Notes:
ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Probability

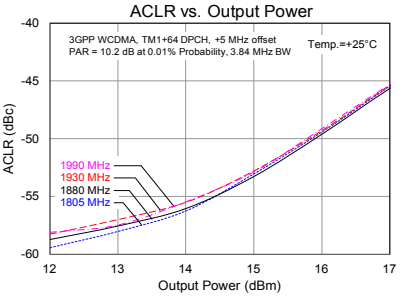
Performance Plots − 1805-1990 MHz

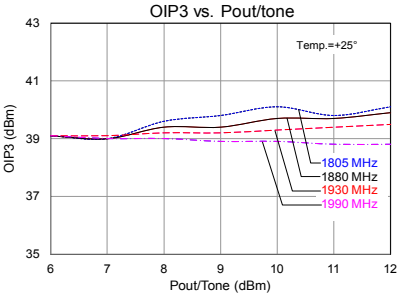
Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

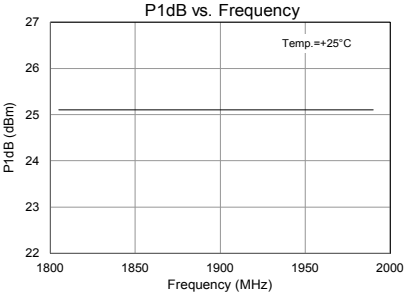












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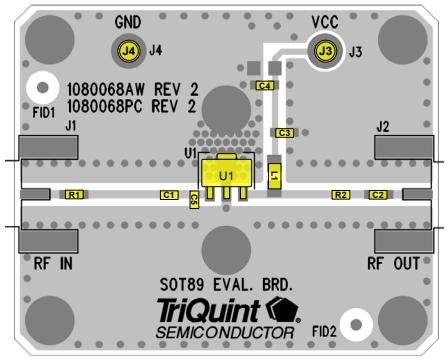
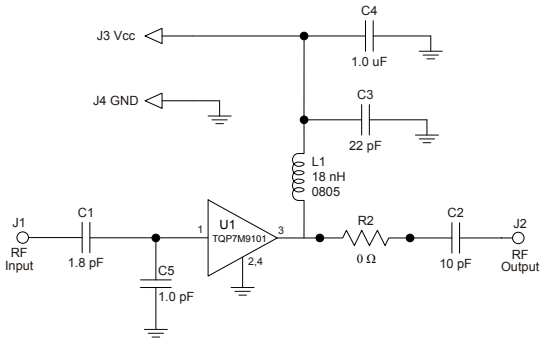
TQP7M9101-PCB2140 Evaluation Board





Notes:
1. See Evaluation Board PCB Information section for PCB material and stack-up.
2. Component (R1) is a 0 Ω resistor and may be replaced with copper trace in the target application layout.
3. All components are of 0603 size unless otherwise specified.
4. Critical component placement locations:
   Distance from U1 Pin 1 Pad (left edge) to C5 (right edge): 40 mils (4.5° at 2140 MHz)
   Distance from C5 (left edge) to C1 (right edge): 45 mils (5.0° at 2140 MHz)
   Distance from U1 Pin 3 (right edge) to R2 (left edge): 295 mils (32.9° at 2140 MHz)
   Distance from R2 (right edge) to C2 (left edge): 95 mils (10.6° at 2140 MHz

Bill of Material − TQP7M9101-PCB2140

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	TriQuint	1080068
U1	n/a	Amplifier, SOT-89 pkg.	TriQuint	TQP7M9101
R1, R2	0 Ω	Resistor, Chip, 0603, 5%, 1/16W	various	
L1	18 nH	Inductor, 0805, 5%, Coilcraft CS Series	Coilcraft	0805CS-180XJLB
C1	1.8 pF	Cap., Chip, 0603, +/-0.1pF. 200V.	AVX	06032U1R8BAT2A
C5	1.0 pF	Cap., Chip, 0603, +/-0.1pF. 200V.	AVX	06032U1R0BAT2A
C2	10 pF	Cap., Chip, 0603pan, +/-1%. 200V	AVX	06032U100FAT2A
C3	22 pF	Cap., Chip, 5%, 50V, NPO/COG	various	
C4	1.0 uF	Cap., Chip, 10%, 10V, X5R	various	

Typical Performance − TQP7M9101-PCB2140

Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

Parameter	Conditions	Typical Value			Units
Frequency		2110	2140	2170	MHz
Gain		17.6	17.5	17.4	dB
Input Return Loss		15	15	15	dB
Output Return Loss		14	13.5	13	dB
Output P1dB		+24.8	+24.8	+24.6	dBm
OIP3	Pout= +8 dBm/tone, Δf=1 MHz	+39.5	+39.5	+39.5	dBm
WCDMA Channel Power(1)	−55 dBc ACLR	+14.5	+14.5	+14.5	dBm
Noise Figure		4.0	3.9	4.1	dB

Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5 MHz offset, PAR = 10.2 dB at 0.01% Prob

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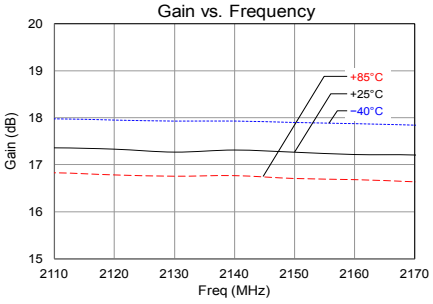
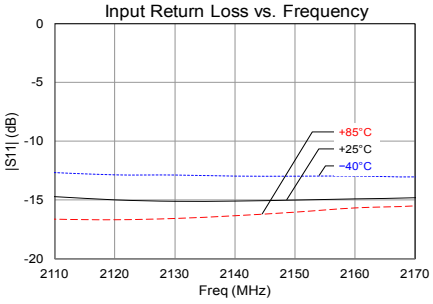
Performance Plots – TQP7M9101-PCB2140

Test conditions unless otherwise noted: V_{CC} =+5V, I_{CQ}=87 mA (typ.), Temp= +25°C

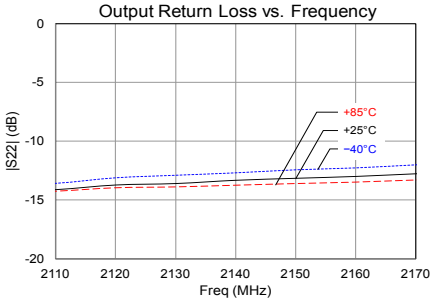
Gain vs. Frequency



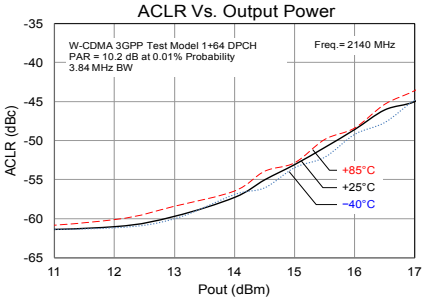
Input Return Loss vs. Frequency



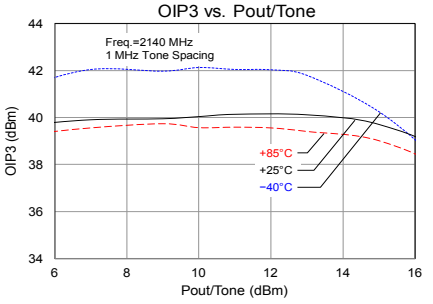
Output Return Loss vs. Frequency



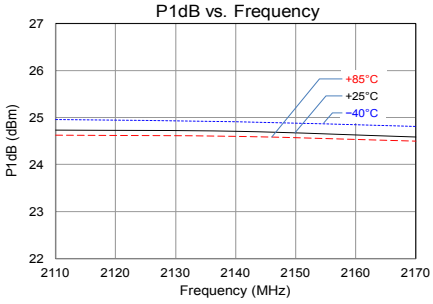
ACLR Vs. Output Power



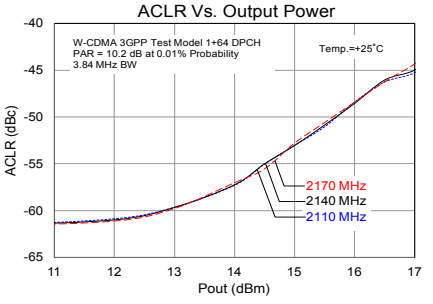
OIP3 vs. Pout/Tone



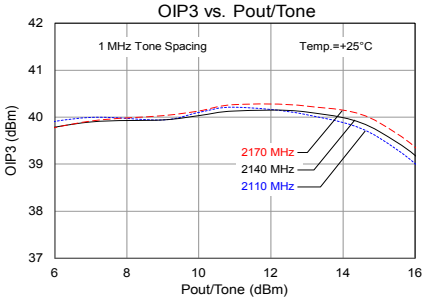
P1dB vs. Frequency



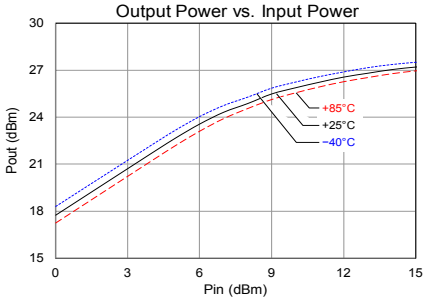
ACLR Vs. Output Power



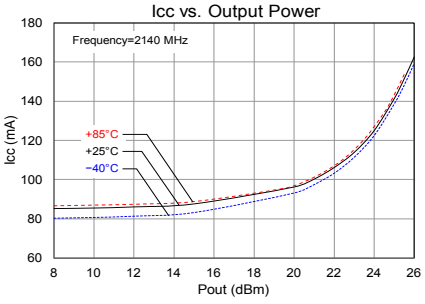
OIP3 vs. Pout/Tone



Output Power vs. Input Power



Icc vs. Output Power



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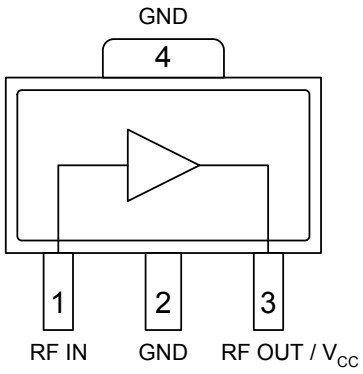
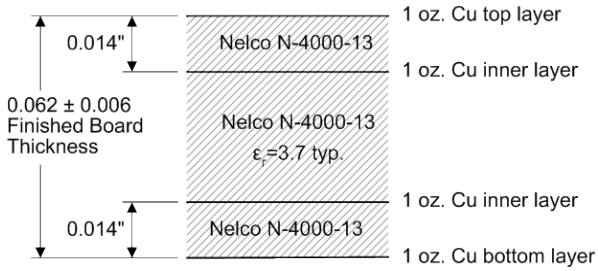
Pin Configuration and Description



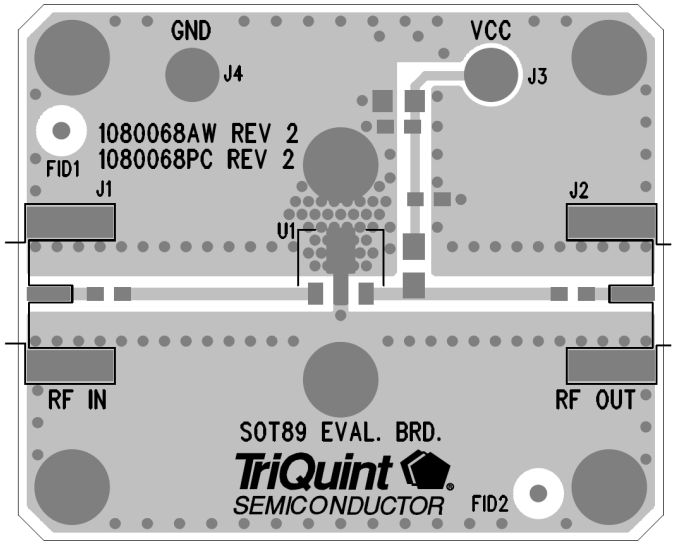
Pin No.	Label	Description
1	RF IN	RF Input. External DC Block required. Requires conjugate match for optimal performance.
2, 4	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.
3	RF OUT / V_{CC}	RF Output, matched to 50 ohms. External DC Block and bias voltage required.

Evaluation Board PCB Information

TriQuint PCB 1080068 Material and Stack-up



50 ohm line dimensions: width = .031”
spacing = .035”.



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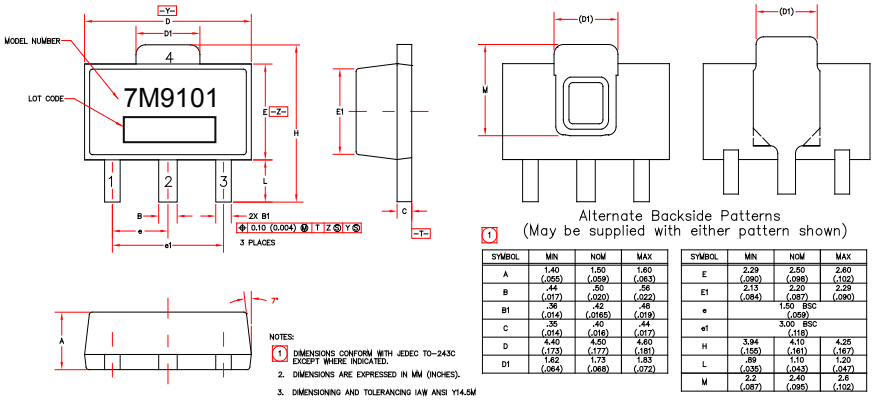
Package Marking and Dimensions

Marking: Part number – 7M9101
Lot code

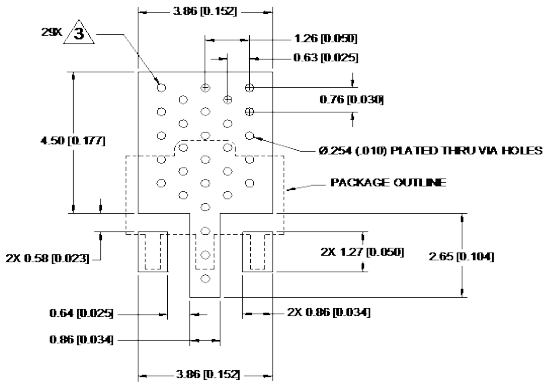


SYMBOL	MIN	NOM	MAX
A	1.40 (.055)	1.50 (.059)	1.60 (.063)
B	.44 (.017)	.50 (.020)	.56 (.022)
B1	.36 (.014)	.42 (.0165)	.48 (.019)
C	.35 (.014)	.40 (.016)	.44 (.017)
D	4.40 (.173)	4.50 (.177)	4.60 (.181)
D1	1.62 (.064)	1.73 (.068)	1.83 (.072)

SYMBOL	MIN	NOM	MAX
E	2.29 (.090)	2.50 (.098)	2.60 (.102)
E1	2.13 (.084)	2.20 (.087)	2.29 (.090)
e		1.50 BSC (.059)	
e1		3.00 BSC (.118)	
H	3.94 (.155)	4.10 (.161)	4.25 (.167)
L	.89 (.035)	1.10 (.043)	1.20 (.047)
M	2.2 (.087)	2.40 (.095)	2.6 (.102)

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Contact plating: NiPdAu

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation.
4. Do not remove or minimize via hole structure in the PCB. Thermal and RF grounding is critical.
5. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
6. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

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Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: Class 2
Value: ≥2000V to <4000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ≥ 2000 V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@triquint.com **Fax:** +1.503.615.8902

For technical questions and application information:

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