Audio Accessory ICs for Mobile Devices

Voice/Audio Mixer & Selector IC

BU7831KN

No.10087EAT02

●Description

BU7831KN is the sound path selector which include 3 stereo inputs, Stereo headphone amp, 600Ω driver amp, and 2stereooutputs. Each output have a mixer and an attenuator, you can set the variable audio path setting. The variable audio source can connect to Headphone and speaker through this LSI.

●Feature

1) It has 3stereo inputs.
2) It has analog mixer on each input.
3) It matches for the application used the Headphone because it has 16Ω audio driver.
4) 16Ω driver has the pop-noise less function.
5) The attenuator of 16Ω driver has soft changing and muting function.
6) It has 600Ω driver for external output.
7) It included stereo output for stereo speaker.
8) VQFN20 small package

●Applications

It is for portable equipments with audio player.

●Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～4.5	V
Power dissipation	Pd	530 *1	mW
Operating temperature range	Topr	-30～+85	℃
Storage temperature range	Tstg	-55～+125	℃

*1 Reduce by 5.3 mW/ ℃ over 25 ℃

●Recommended operating range

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Supply voltage	VDD	2.5	3.0	3.3	V

●Electric Characteristics

Unless otherwise specified, Ta=25 ℃,AVDD=DVDD=3.0V

・Analog Part

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Stand-by current	Istb	-	-	3	μA	Stand-by mode
Operation current 1	Idd1	-	0.26	0.42	mA	BIAS part. No signal
Operation current 2	Idd2	-	2.3	3.7	mA	ST1R, ST1L to HPR, HPL Exclude Idd1, No signal
Total harmonic distortion 1 (HPL, HPR)	THDhp1	-	0.05	0.5	%	Vo=-10dBV, 20kHzL PF
Output power 1(HPL, HPR)	PO1	-	10	-	mW	THD=10%, RL=16Ω
Output Noise Voltage 1 (HPL, HPR)	V_{NO}	-	-94	-80	dBV	JIS A weighting
Maximum output level 1 (SPL, SPR)	VO_{MAX1}	2.0	-	-	Vp-p	THD≦1%, RL=10kΩ
Maximum output level 2 (EXTO)	VO_{MAX2}	2.0	-	-	Vp-p	THD≦1%, RL=600Ω

・Digital input (DC)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Input L level voltage	V_{IL}	-	-	0.7	V	
Input H level voltage	V_{IH}	2.1	-	-	V	
Input current	I_{IN}	-	-	±2	μA	0V, 3V force

・CPU interface

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Cycle Time	tcyc	250	-	-	ns	
Input Data Hold Time	tdh	50	-	-	ns	
Input Data Setup Time	tds	50	-	-	ns	
Chip Select Setup Time	tcs	50	-	-	ns	
Chip Select Hold Time	tch	50	-	-	ns	

●**Reference Data** (Unless otherwise specified, Ta=25 ℃,AVDD=DVDD=3.0V)

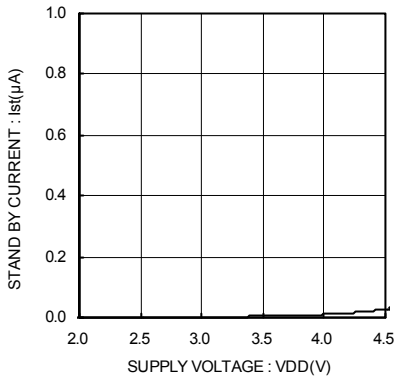


Fig.1 Stand-by current

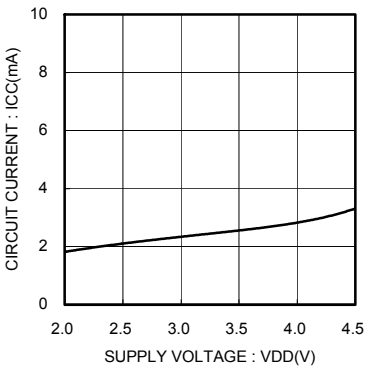


Fig.2 Operation current
At Headphone AMP part

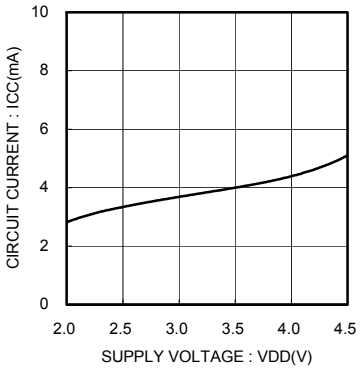


Fig.3 Operation current
Of All blocks

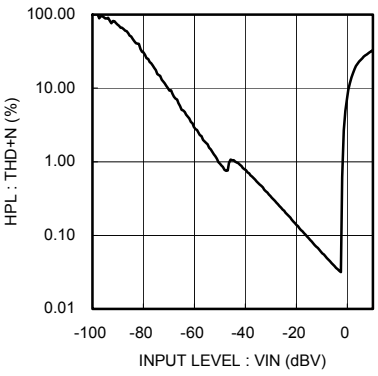


Fig.4 Total harmonic
Distortion (HPL)

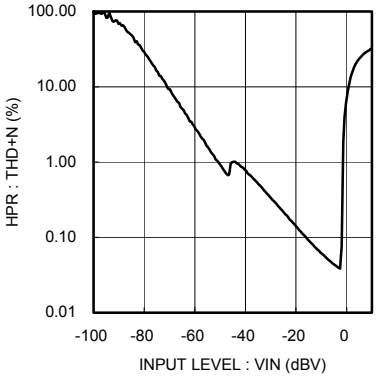


Fig.5 Total Harmonic
Distortion (HPR)

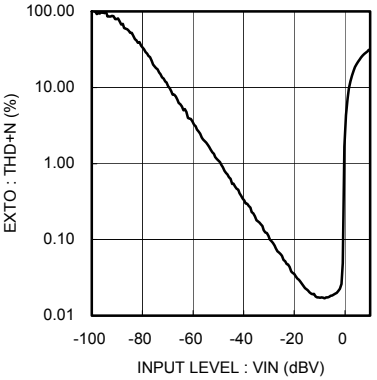


Fig.6 Total Harmonic
Distortion (EXTO)

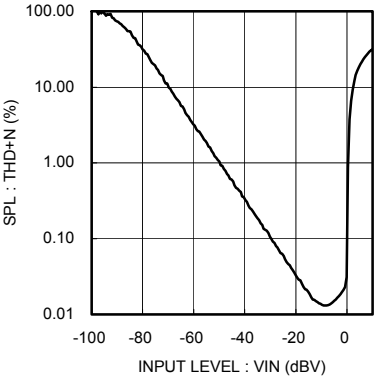


Fig.7 Total Harmonic
Distortion (SPL)

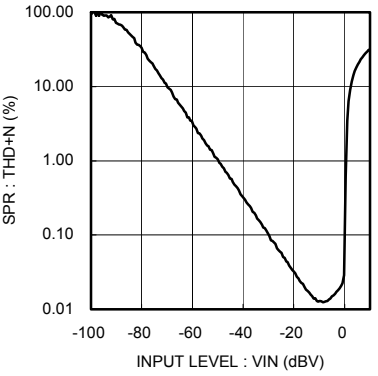


Fig.8 Total Harmonic
Distortion (SPR)

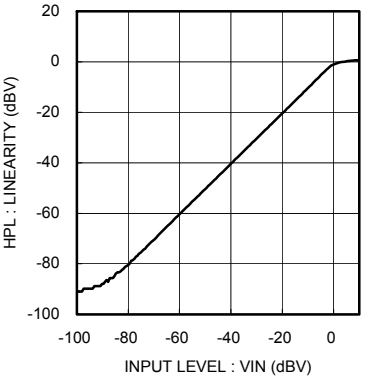


Fig.9 Linearity (HPL)

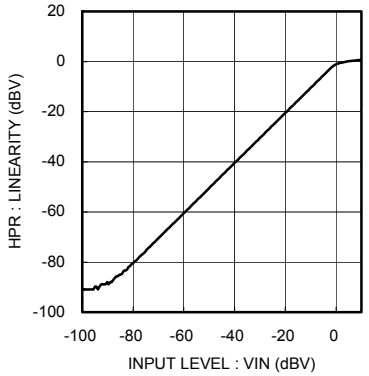


Fig.10 Linearity (HPR)

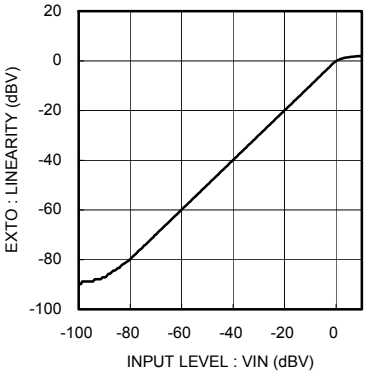


Fig.11 Linearity (EXTO)

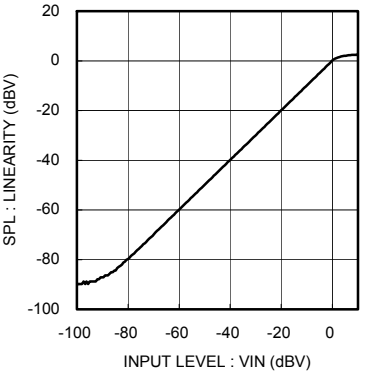


Fig.12 Linearity (SPL)

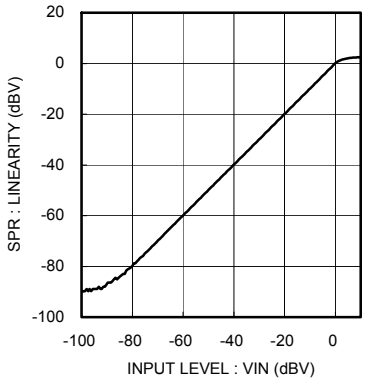


Fig.13 Linearity (SPR)

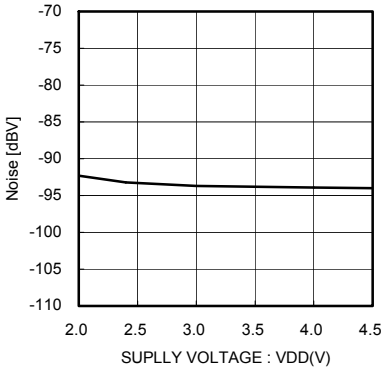


Fig.14 Output Noise (HPL)

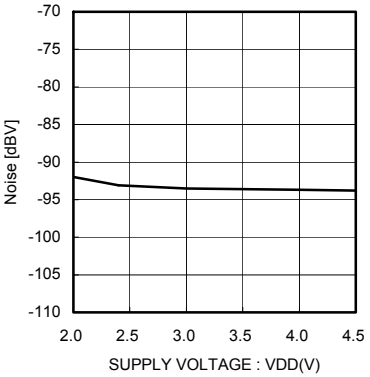


Fig.15 Output Noise (HPR)

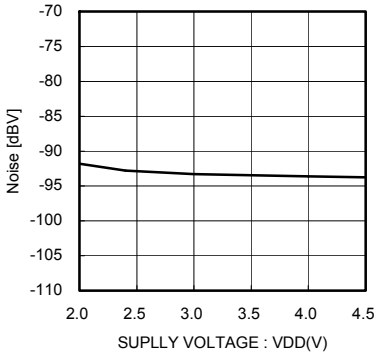


Fig.16 Output Noise (EXTO)

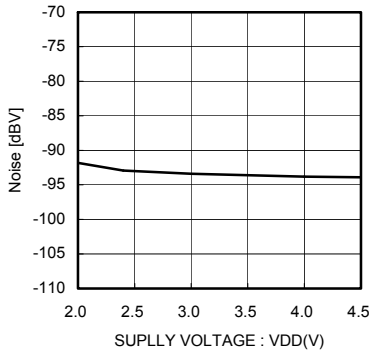


Fig.17 Output Noise (SPL)

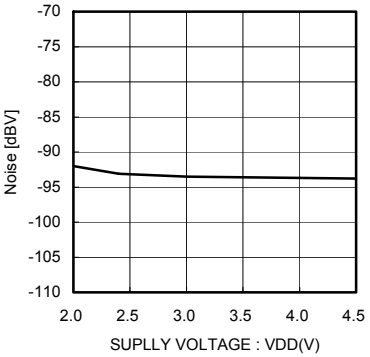


Fig.18 Output Noise (SPR)

●Block Diagram, Recommended application circuit, Pin assign

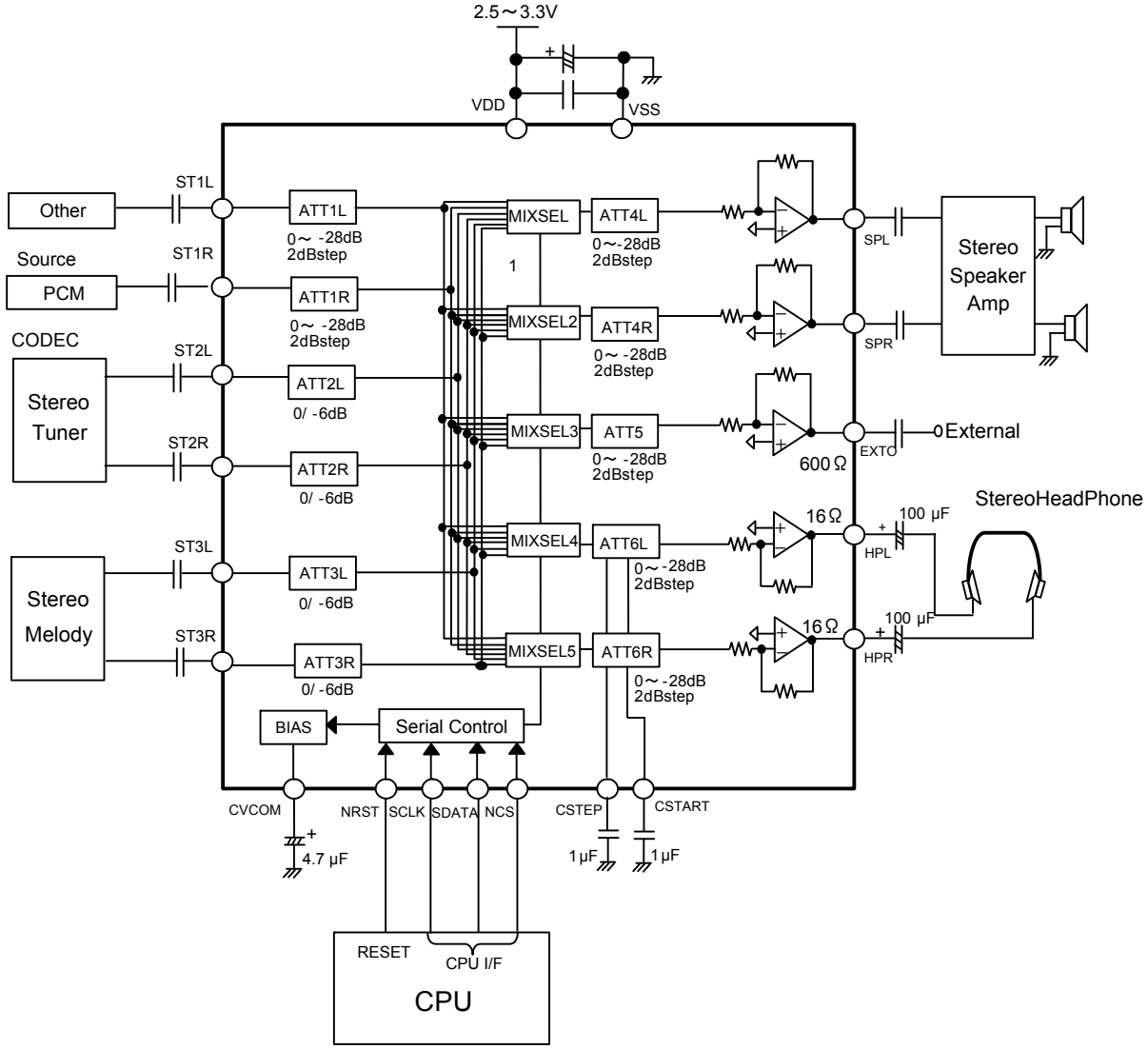


Fig.19 Application circuit example

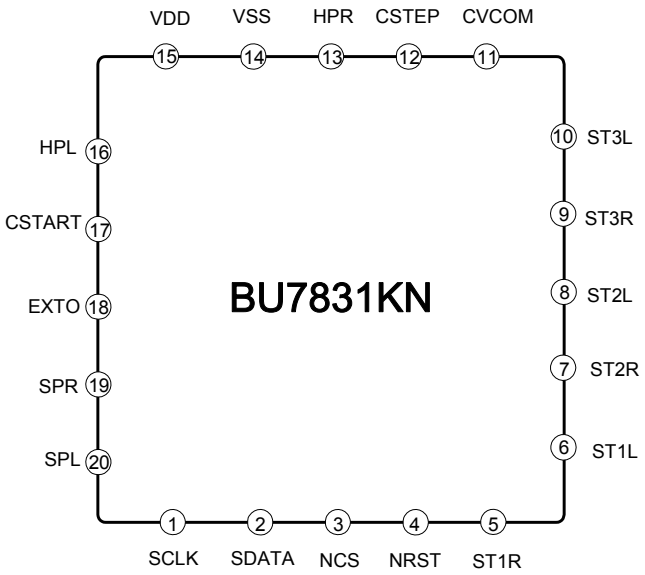
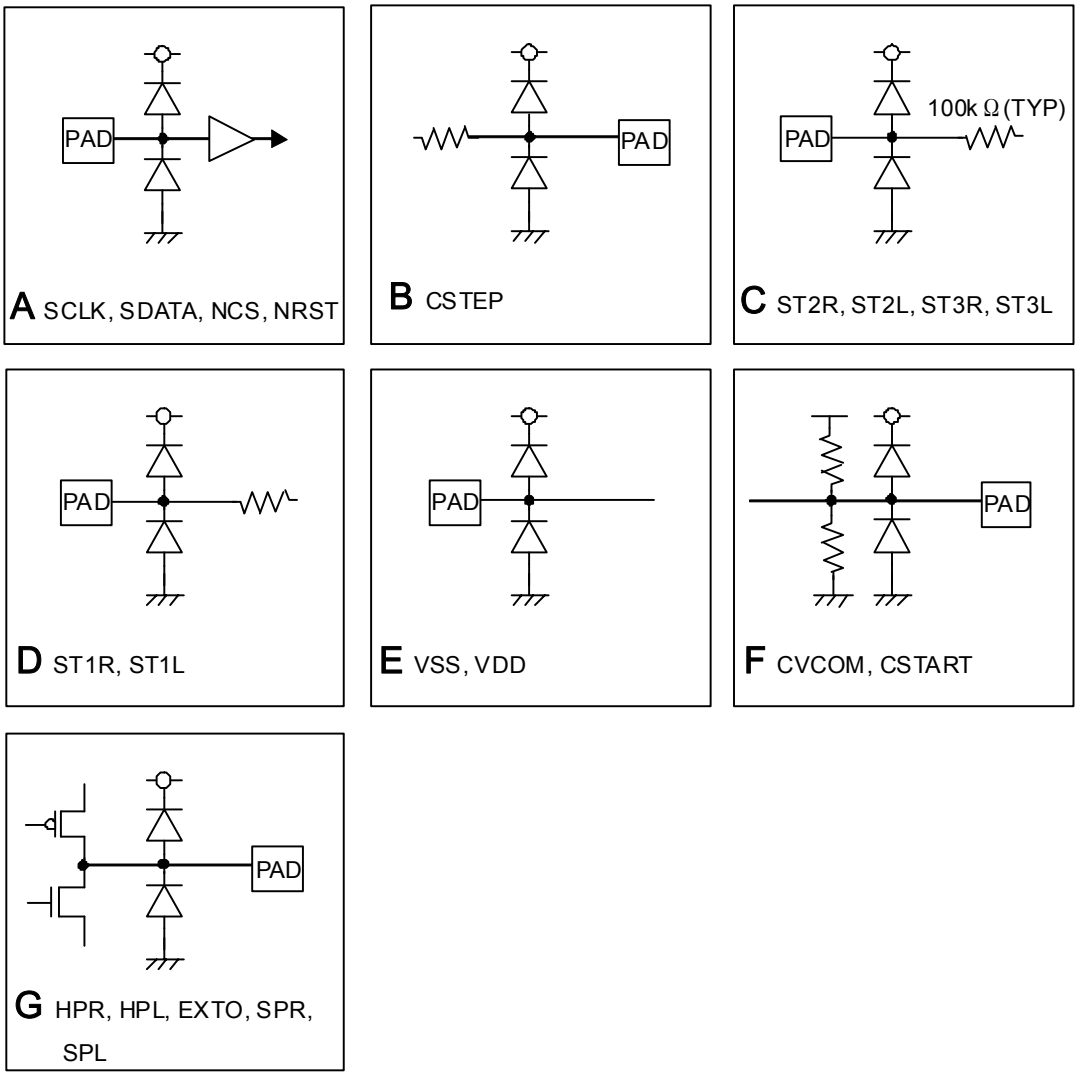


Fig.20 Pin Assign

●Input terminal equivalent circuit diagram



About Digital input (Type A): When you will have possibility to give Hi-z for input pin,
You must select from the under heads for protect the pin floated.

a) Pull down with less than 10kohm
b) Pull up
c) Give “L” signal just before Hi-Z.

Fig.21 Equivalent circuit diagram

No.	Name	Function
1	SCLK	Serial clock input of CPU I/F
2	SDATA	Serial data input of CPU I/F
3	NCS	Chip select input of CPU I/F
4	NRST	Reset input L=Reset
5	ST1R	Stereo 1 input for R channel
6	ST1L	Stereo 1 input for L channel
7	ST2R	Stereo 2 input for R channel
8	ST2L	Stereo 2 input for L channel
9	ST3R	Stereo 3 input for R channel
10	ST3L	Stereo 3 input for L channel

No.	Name	Function
11	CVCOM	Reference voltage
12	CSTEP	Connect capacitor for blocking pop-noise
13	HPR	Headphone R channel output
14	VSS	Ground
15	VDD	Power supply
16	HPL	Headphone L channel output
17	CSTART	Connect capacitor for blocking start up pop-noise
18	EXTO	600Ω driver output
19	SPR	Speaker R channel output
20	SPL	Speaker L channel output

●Detail explanation of each function blocks

・Reference Voltage (Bias part)

The reference voltage occurrence part that decides the operating point of a group of internal amplifiers is the following.
CVCOM_OUT, CSTART_OUT, all is about 1/2VDD[V], and therefore the level of internal signal becomes about 1/2VDD[V], too. CVCOM has a pre-charge function, and it is possible to shorten of rising time of the bias in ON.
(As for the CVCOM, ON/OFF of the pre-charge function is possible with a register bit.)
CSTART terminal is used as a reference voltage of the output amplifier of the headphone, and it included pop sound low stage function in headphone path ON/ OFF, too.
Capacitor value with the outside in the figure is recommended to make the PSRR character of both standard voltages the same. Choose the thing whose character is good in Capacitor with the outside because it becomes the reference voltage of the internal circuit.

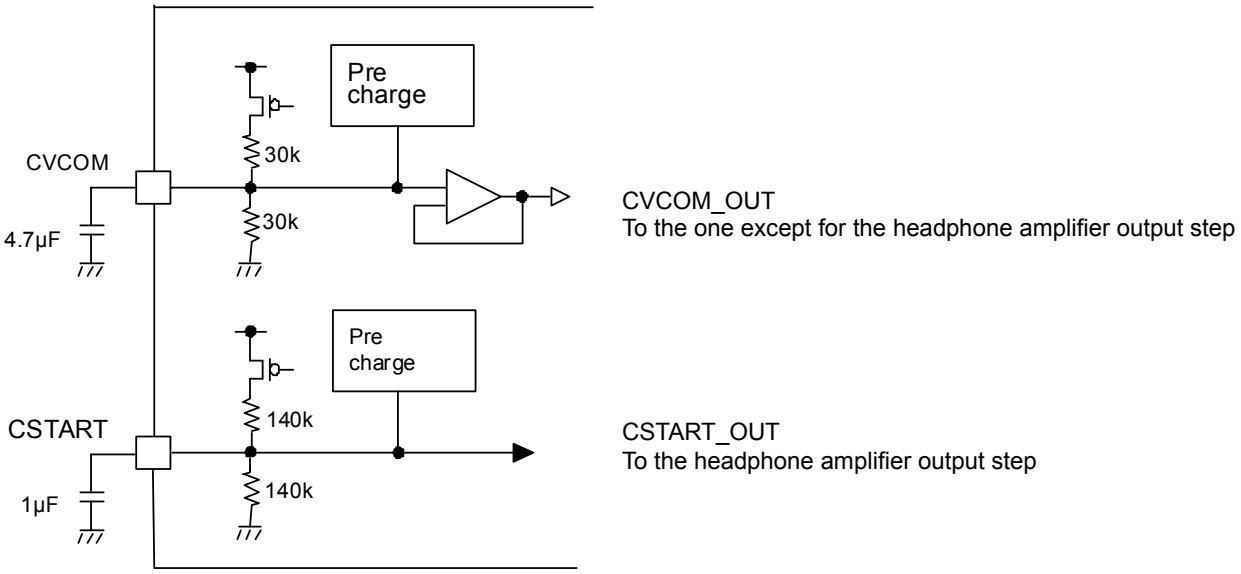


Fig.22 CVCOM, CSTRT equivalent circuit

・Analog input part

The following is about each analog. Input. Please use the coupling capacitor with the outside in consideration of frequency characteristic of input. Input DC level is about 1/2VDD[V]. Input impedance on off (input non-choice) becomes Hi-z. When an input terminal isn't used (when an input path isn't set up) is open, and there is no problem. But, be careful that noise from the outside and so on doesn't turn because it becomes Hi-z. When it is anxious, pull-down in about 100kΩ.
ST1L and ST1R inputs change input impedance by setting of ATT1L and ATT1R respectively.

ST1L(R) input impedance	ATT1 L (R) setting
200kΩ(TYP)	0dB setting
400kΩ(TYP)	Mute setting

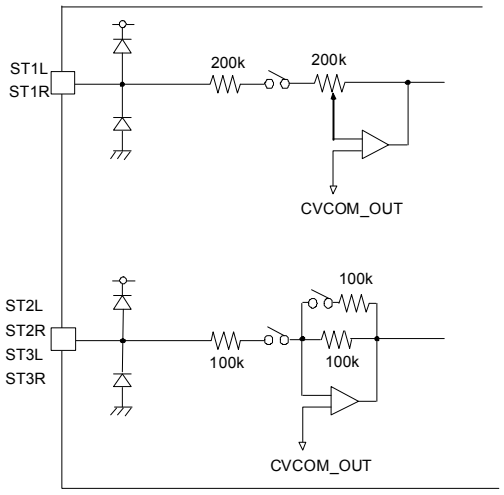


Fig.23 Input pins equivalent circui

・**Analog output part**

The following is about Analog output part (EXTO, SPL, SPR, HPL, HPR).
Each output amplifier is linked path select (MIXER1～5).
Because stereo output is presumed, HPL and HPR are turned ON/OFF at the same time, and with pop sound decrease function.

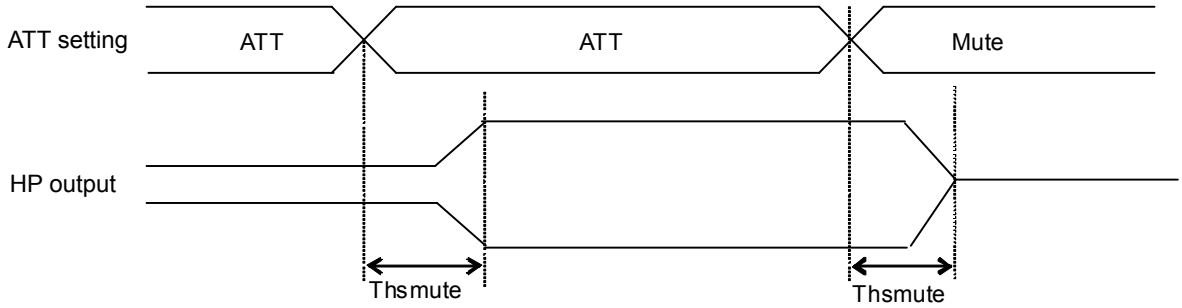
MIXER1	At the time of path choice	SPL output amplifier ON
MIXER2	At the time of path choice	SPR output amplifier ON
MIXER3	At the time of path choice	EXTO output amplifier ON
MIXER4 or MIXER5	At the time of path choice	HPL, HPR output amplifier ON

Be careful that noise from the outside and so on doesn't turn because it becomes Hi-z though the output that isn't used is open and there is no problem. When it is anxious, pull-down in about 100kΩ.

Output Port	Output impedance (DC) At ON	Output impedance (DC) At OFF
EXTO	1.4Ω	Hi-z
SPL SPR	2.2Ω	Hi-z
HPL	1.5Ω	GND short
HPR	0.6Ω	

・**Attenuator**

Each attenuator has 16 steps (4bit), which contains mute. ATT6L and ATT6R that is attenuator of the headphone output has soft mute that decreases pop sound in switching. (ATT1 - 5 don't have this function.)
The amount of software depends on a capacitor to connect to the CSTEP terminal. Decide the value of a capacitor to connect to the CSTEP terminal after you take pop volume and delay time into consideration because a fixed number becomes the bottom mostly at the time of that switching.



$$Thsmute = 200 \times 10^{3} \times CSTEP \ [S]$$

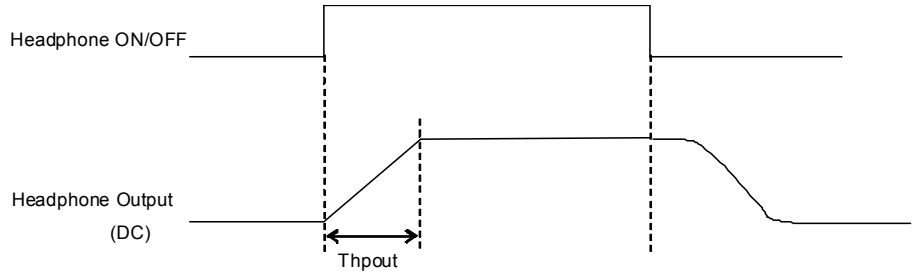
Fig.24

・**Analog path part**

About the internal pass circuit, the circuit that it has a path setting by the register turns it on. For example, when MIXSEL*_0 is chosen with either ATT, ST1R input is chosen, and a group of input amplifiers of ST1R turns it on. And a connected output amplifier is turned on when either input is chosen with MIXSEL* in the same way to the output circuit.

・Pop sound decrease circuit at the time of head phone output ON/ OFF

It has the function that decreases pop sound that occurs at the time of ON/ OFF of the headphone output (HPL and HPR). When headphone output is chosen/non-chosen, it is the function that the DC output of the headphone output goes down smoothly on falling/rising. Rising time is decided by the capacitor value that it is connected to the CSTART terminal. Falling time is decided by the CSTART terminal and the coupling capacitor. Pop sound decreases as much as to be here if rising/falling is smooth. Decide the value of a capacitor to connect to the CSTART terminal after you take pop sound, rising/falling time into consideration because a fixed number becomes the bottom mostly at the time of that switching.
And do settlement of timing in consideration of this time when you make it turn ON/OFF by the continuance.
Pop sound is made when it switches in the middle of the descent of rising/falling.



$$Thpout = 80.6 \times 10^3 \times CSTART[S]$$

Fig.25

・Digital part

Input such as clock, data is to input "H" or "L" properly about each digital input terminal to contain at the time of standing by as well. If you turn off the power (When Hi-z is input), a control side is to avoid an input terminal's becoming open in either following method It has the possibility that penetration electric current occurs because it becomes the input which isn't fixed as BU7831KN when it isn't avoided.

a） Terminal, in less than 10kΩ, pull-down
b） Terminal, pull-up
c） When it becomes input Hi-z, "L" is given to it.

・CPU interface

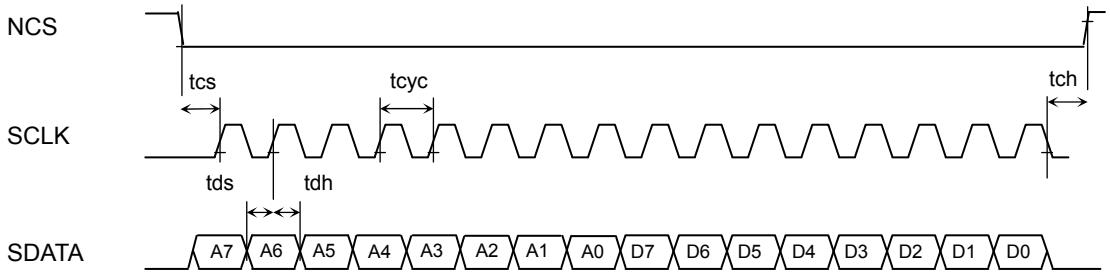


Fig.26

SDATA will be confirmed by 16th clock that is inputted after NCS falling edge, and then serial data reflect to internal register by NCS falling edge. The data format is 16bit rear.
CPU I/F is 1Byte=16bit. Because it doesn't cope with continuous data transmission, you must surely insert the section of NCS= "H" between 1st Byte and 2nd Byte. The following the is to secure time beyond the SCLK 1 clock. (th≧tcyc)

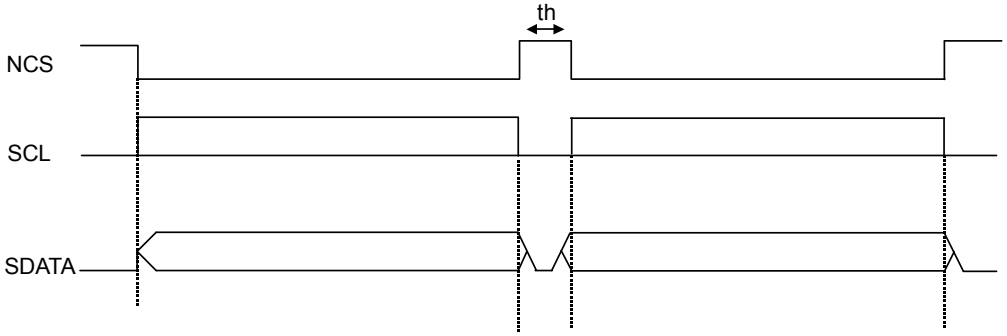


Fig.27

Using in the BU7831KN dedicated line is recommended with a CPU I/F.
Control it by a sequence like the bottom when you don't do special control.

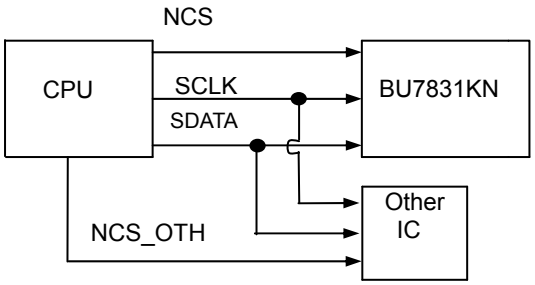


Fig.28

CPU I/F input signals waveforms

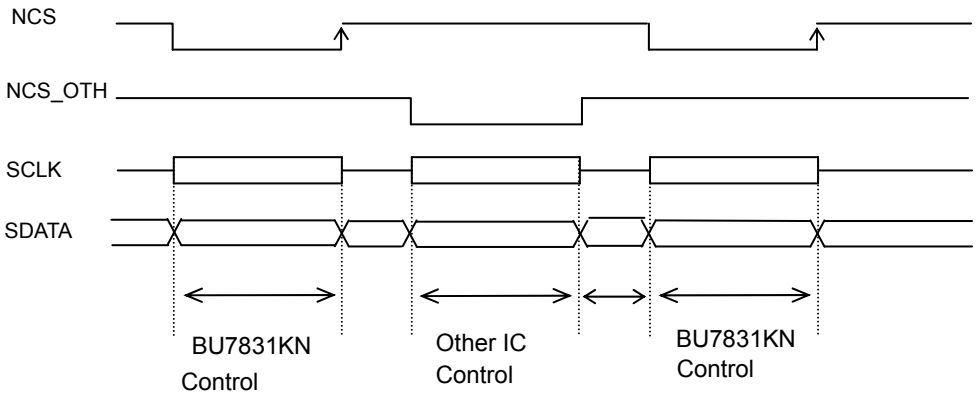


Fig.29

Please NCS of BU7831KN is set “H” when you control the other IC.
When NCS is "H", the register of BU7831KN can't write it.

note) NCS_OTH is based on the specifications of other IC's.

●Recommended operation sequence

VDD ON

NRST=L start. Rise up VDD first.
After the mode setting, input the audio signal.

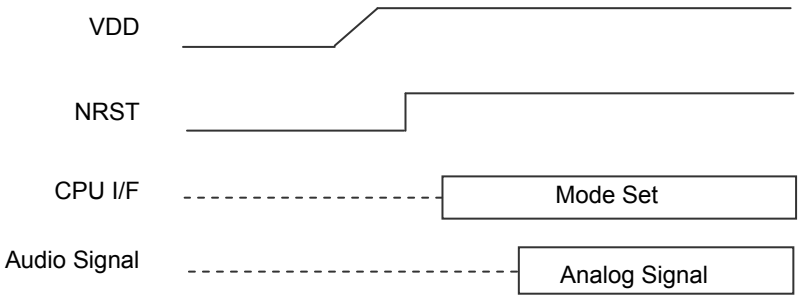


Fig. 30

VDD OFF

HPRST=0(82h=00h) is taken at the time of use of HPAMP first.
VDD OFF, after the mute on setting(88h=FFh), NRST=L at using HPAMP.
VDD OFF, after NRST=L at not using HPAMP.

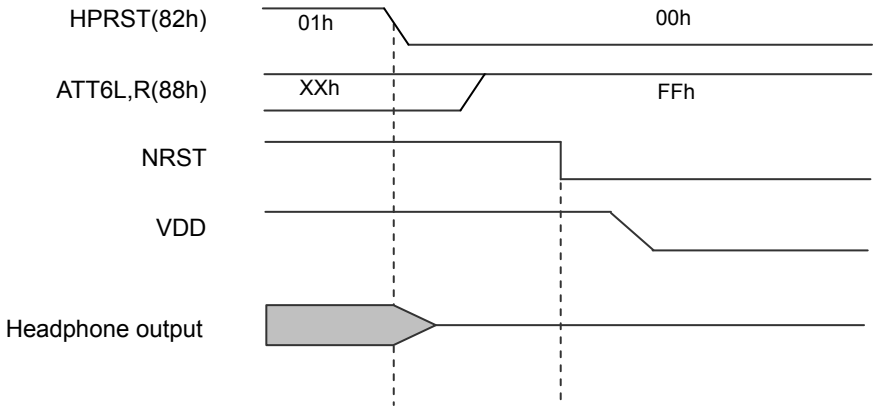


Fig. 31

HPAMP ON

Mute OFF (HPRST 82h bit0), after the mode setting.

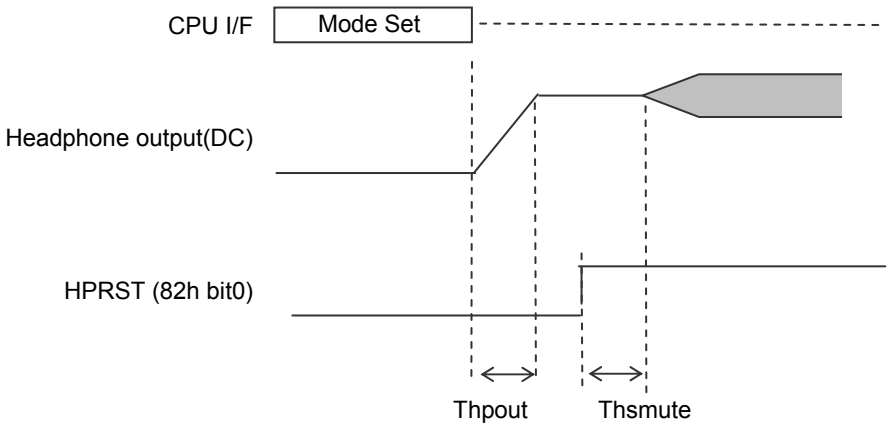


Fig. 32

・HPAMP OUTPUT rise time setting up expression
Thpout = 80.6 × 10^3 × CSTART [s] (typ)

・HSMUTE delay time setting up expression
Thsmute = 200 × 10^3 × CSTEP [s] (typ)

HPAMP OFF

HPRST=0(82h bit0) is set up first.
Other setups are canceled after ATT6L, R is set up in the mute(88h=ffh).

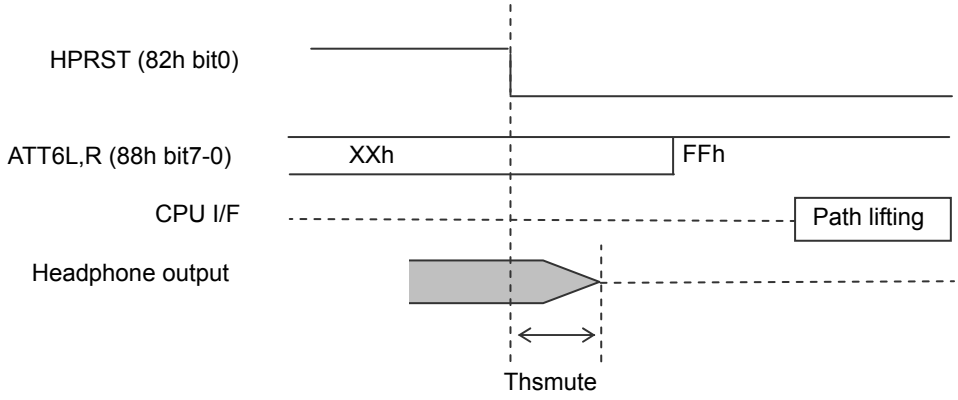


Fig. 33

HPAMP Volume Control

As the mute time is set by capacitor connected CSTEP pin,Volume control it is set after enough time.
The delay time is as same as Thsmute.

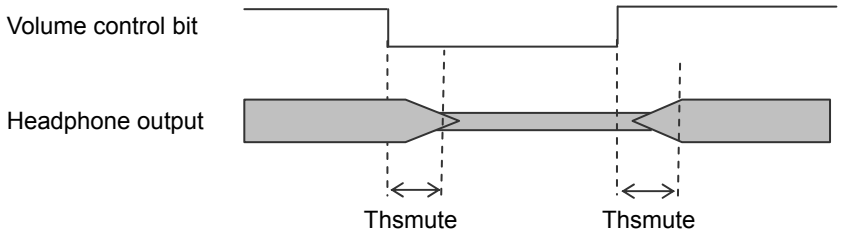
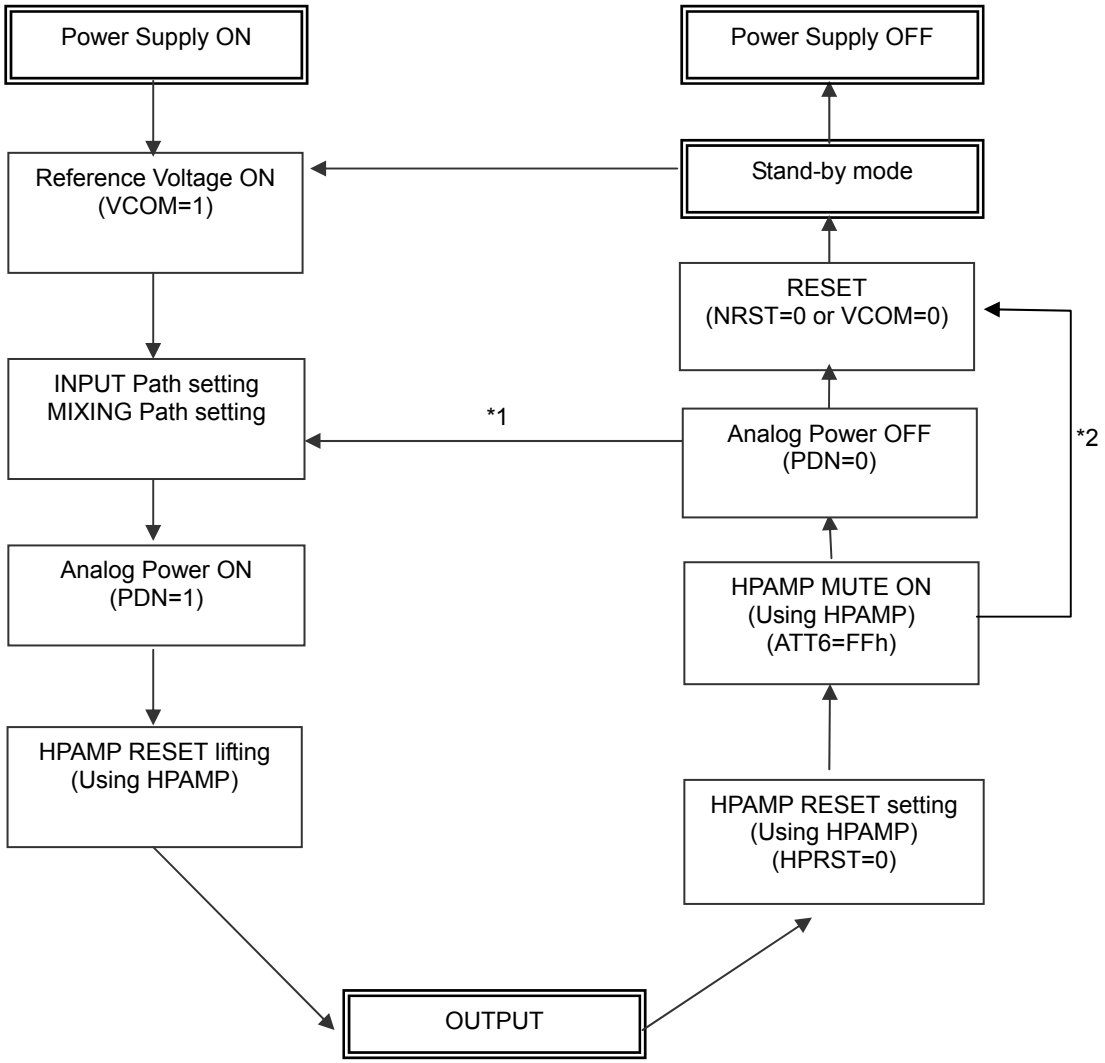


Fig. 34

Mode Setting Flow



*1 : When the analog path setting is not changed. (Repeat output)
*2 : When the Power supply OFF, after output.

Fig. 35

●Notes for use

1) Absolute maximum ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2) Operating conditions
Characteristics are guaranteed under the conditions of each specified parameter.

3) Reverse polarity connection of the power supply
Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

4) Power supply line
Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks.
Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, note that capacitance characteristic values are reduced at low temperatures.

5) GND voltage
GND potential should maintain at the minimum ground voltage level. Furthermore, no terminals should be lower than the GND potential voltage including electric transients.

6) Short circuit between terminals and GND or other devices
Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals to GND, or other components on the circuits, can damage the IC.

7) Operation in a strong electromagnetic field
Using the ICs in a strong electromagnetic field can cause operation malfunction.

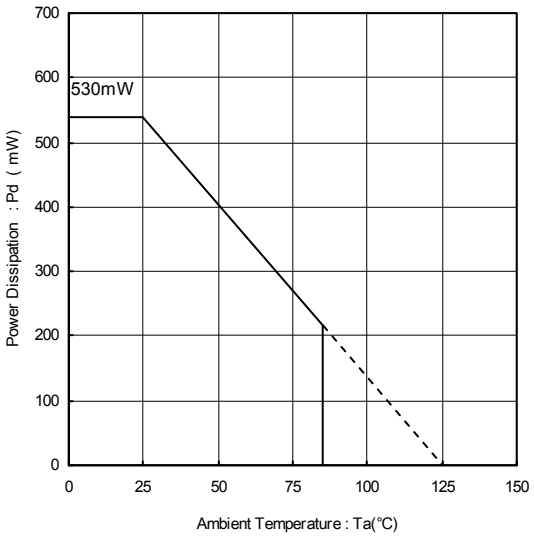
8) Inspection with set PCB
During testing, turn on or off the power before mounting or dismounting the board from the test board.
Do not power up the board without waiting for the output capacitors to discharge. The capacitors in the low output impedance terminal can stress the device. Pay attention to the electro static voltages during IC handling, transportation, and storage.

9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and breakdown of the input terminal. Therefore, pay thorough attention not to apply a voltage lower than the GND to the input terminals. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply a voltage lower than the power supply voltage to the input terminals, or a voltage within the guaranteed value of electrical characteristics.

10) Ground wiring patterns
The power supply and ground lines must be as short and thick as possible to reduce line impedance. Fluctuating voltage on the power ground line may damage the device.

11) External capacitor
When using external ceramic capacitors, consider degradation in the nominal capacitance value due to DC bias and changes in the capacitance with temperature.

●Power Dissipation



This value is the measurement value that was mounted on the PCB by ROHM
Material : Grass epoxy
Size : 70mm × 70mm × 1.6mm

Fig.36

●Ordering part number

B	U	7	8	3	1	K	N	-	E	2

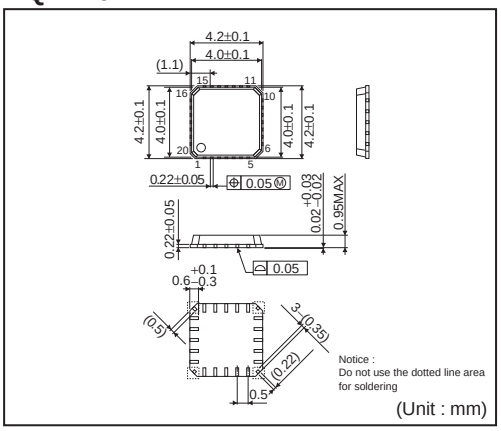
Part No.

Part No.
7831

Package
KN : VQFN20

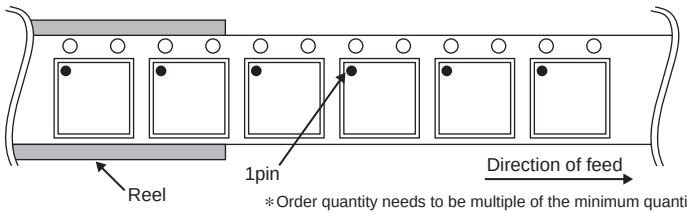
Packaging and forming specification
E2: Embossed tape and reel

VQFN20



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



＊Order quantity needs to be multiple of the minimum quantity.

Notes

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