

P-Channel 8-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 8	0.023 at $V_{GS} = - 4.5$ V	- 12 ^a	19 nC
	0.031 at $V_{GS} = - 2.5$ V	- 12 ^a	
	0.040 at $V_{GS} = - 1.8$ V	- 12 ^a	
	0.058 at $V_{GS} = - 1.5$ V	- 12 ^a	
	0.095 at $V_{GS} = - 1.2$ V	- 12 ^a	

FEATURES

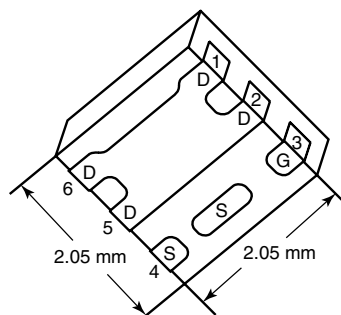
- Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance


RoHS
COMPLIANT

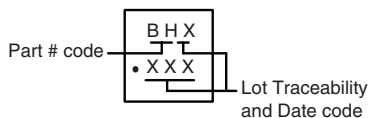
APPLICATIONS

- Load Switch, PA Switch for Portable Devices

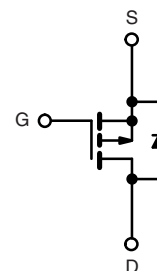
PowerPAK SC-70-6L-Single



Marking Code



Ordering Information: SiA417DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 8	V
Gate-Source Voltage	V_{GS}	± 5	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	- 12 ^a	A
	$T_C = 70^\circ\text{C}$	- 12 ^a	
	$T_A = 25^\circ\text{C}$	- 12 ^{a, b, c}	
	$T_A = 70^\circ\text{C}$	- 8.3 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 30	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	- 12 ^a	
	$T_A = 25^\circ\text{C}$	- 2.9 ^{b, c}	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	19	W
	$T_C = 70^\circ\text{C}$	12	
	$T_A = 25^\circ\text{C}$	3.5 ^{b, c}	
	$T_A = 70^\circ\text{C}$	2.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	28	36	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	5.3	6.5	

Notes:

a. Package limited

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 80 $^\circ\text{C}/\text{W}$.

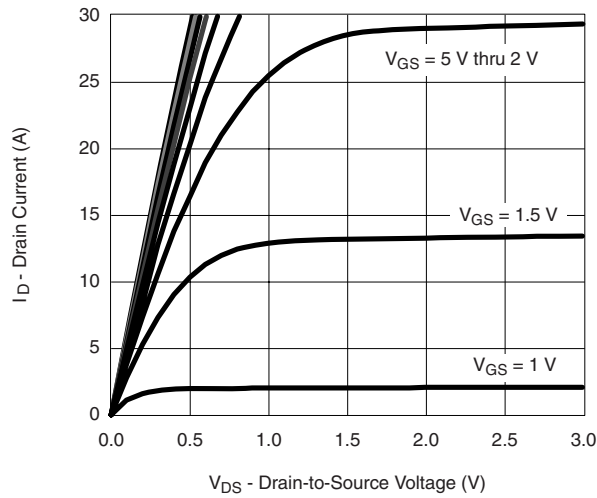
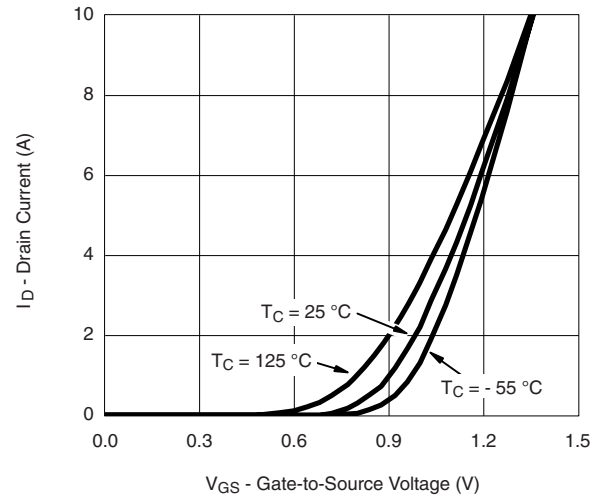
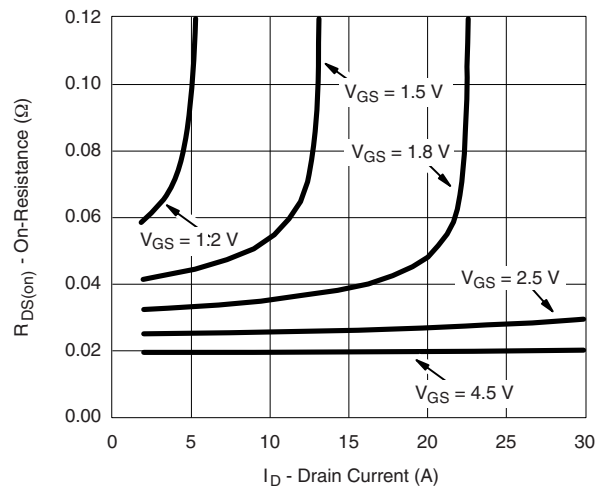
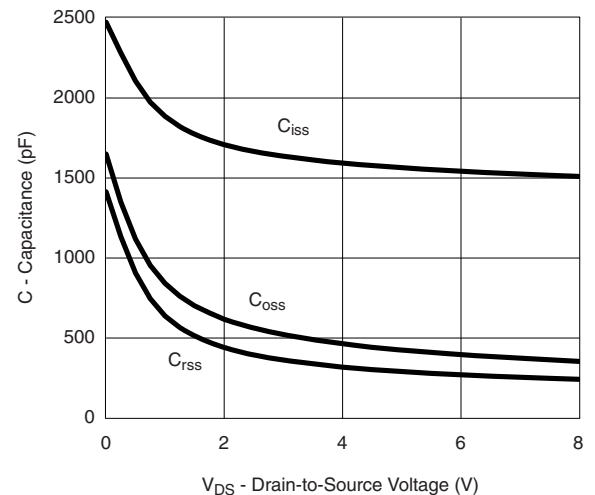
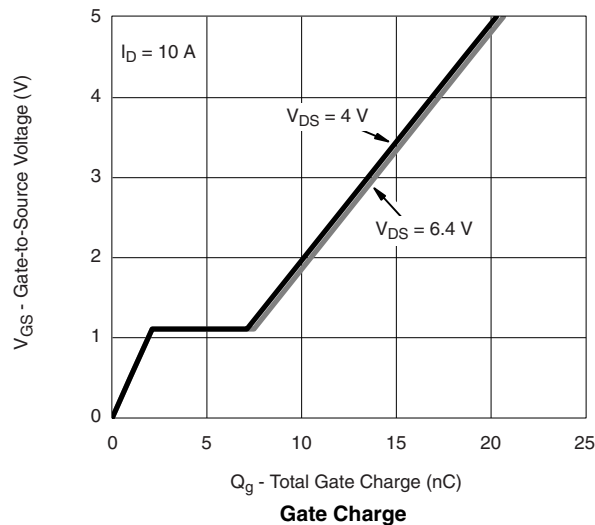
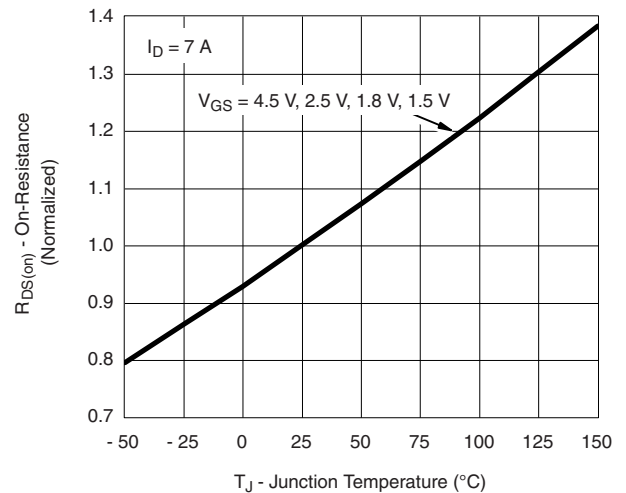
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 8			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 7.3		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.35		- 1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 5 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 8 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 8 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 7 A		0.019	0.023	Ω
		V _{GS} = - 2.5 V, I _D = - 6 A		0.026	0.031	
		V _{GS} = - 1.8 V, I _D = - 5.3 A		0.033	0.040	
		V _{GS} = - 1.5 V, I _D = - 1.7 A		0.043	0.058	
		V _{GS} = - 1.2 V, I _D = - 1.1 A		0.063	0.095	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 4 V, I _D = - 7 A		23		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 4 V, V _{GS} = 0 V, f = 1 MHz		1600		pF
Output Capacitance	C _{oss}			500		
Reverse Transfer Capacitance	C _{rss}			320		
Total Gate Charge	Q _g	V _{DS} = - 4 V, V _{GS} = - 5 V, I _D = - 10 A		21	32	nC
Gate-Source Charge	Q _{gs}	V _{DS} = - 4 V, V _{GS} = - 4.5 V, I _D = - 10 A		19	29	
Gate-Drain Charge	Q _{gd}			2.2		
Gate Resistance	R _g			5		
Gate Resistance	R _g	f = 1 MHz		8		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 4 V, R _L = 0.5 Ω I _D ≅ - 8.3 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		15	25	ns
Rise Time	t _r			25	38	
Turn-Off Delay Time	t _{d(off)}			80	120	
Fall Time	t _f			45	70	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 4 V, R _L = 0.5 Ω I _D ≅ - 8.3 A, V _{GEN} = - 5 V, R _g = 1 Ω		10	15	
Rise Time	t _r			12	20	
Turn-Off Delay Time	t _{d(off)}			80	120	
Fall Time	t _f			45	70	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 12	A
Pulse Diode Forward Current	I _{SM}				- 30	
Body Diode Voltage	V _{SD}	I _S = - 8.3 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 8.3 A, di/dt = 100 A/μs, T _J = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q _{rr}			33	50	nC
Reverse Recovery Fall Time	t _a			15		ns
Reverse Recovery Rise Time	t _b			45		

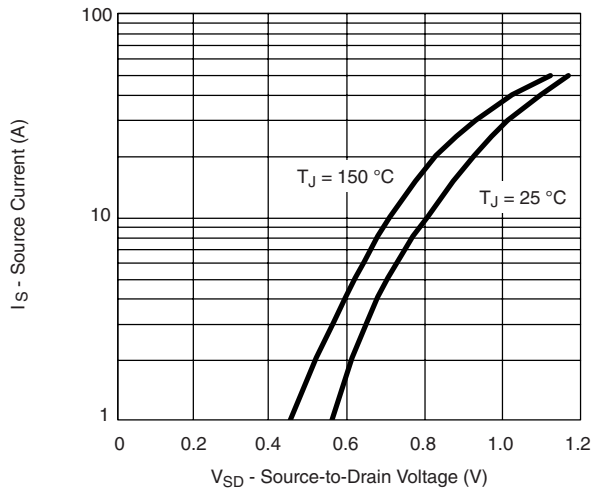
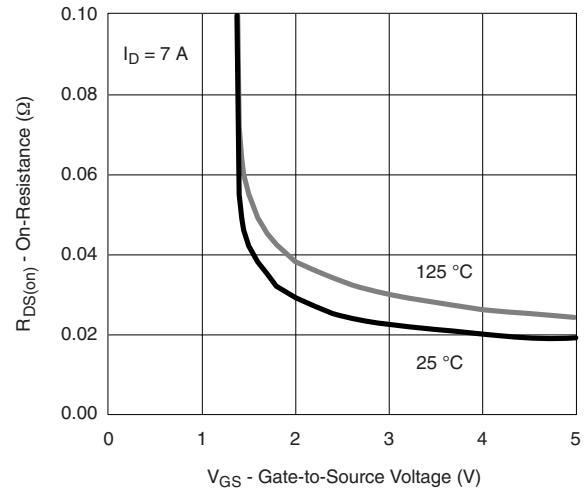
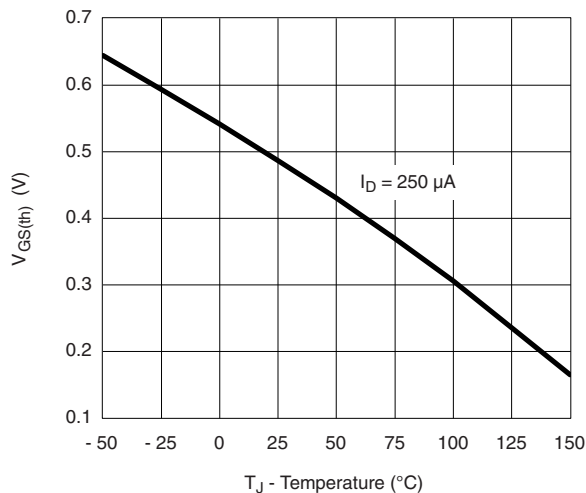
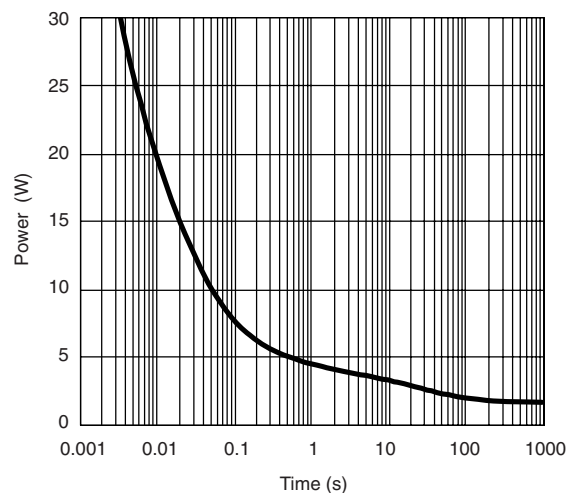
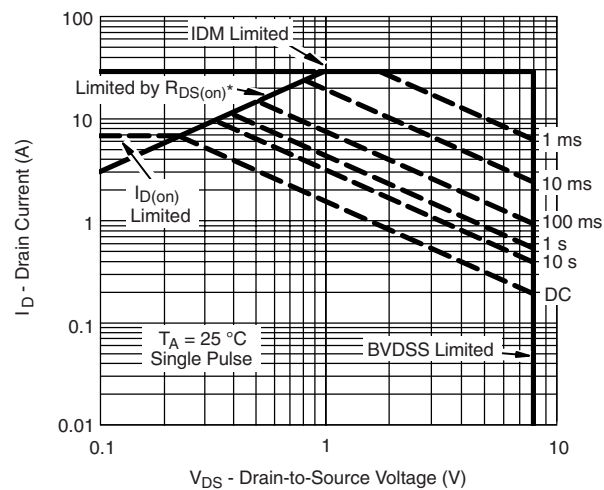
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

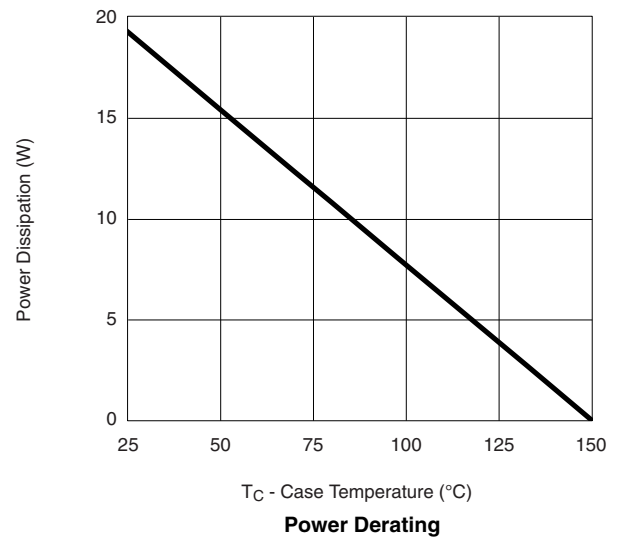
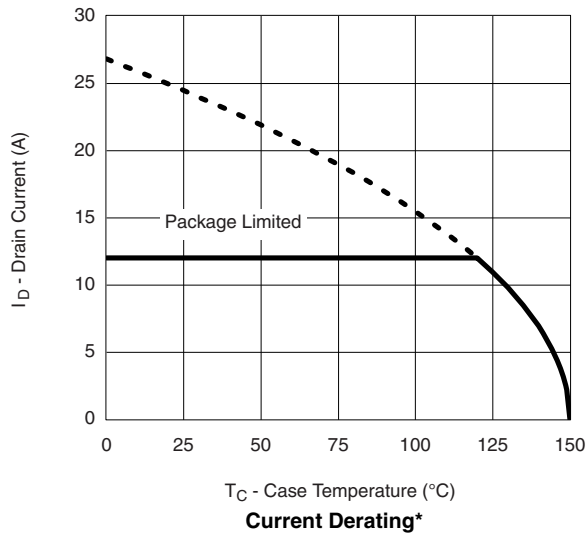
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**



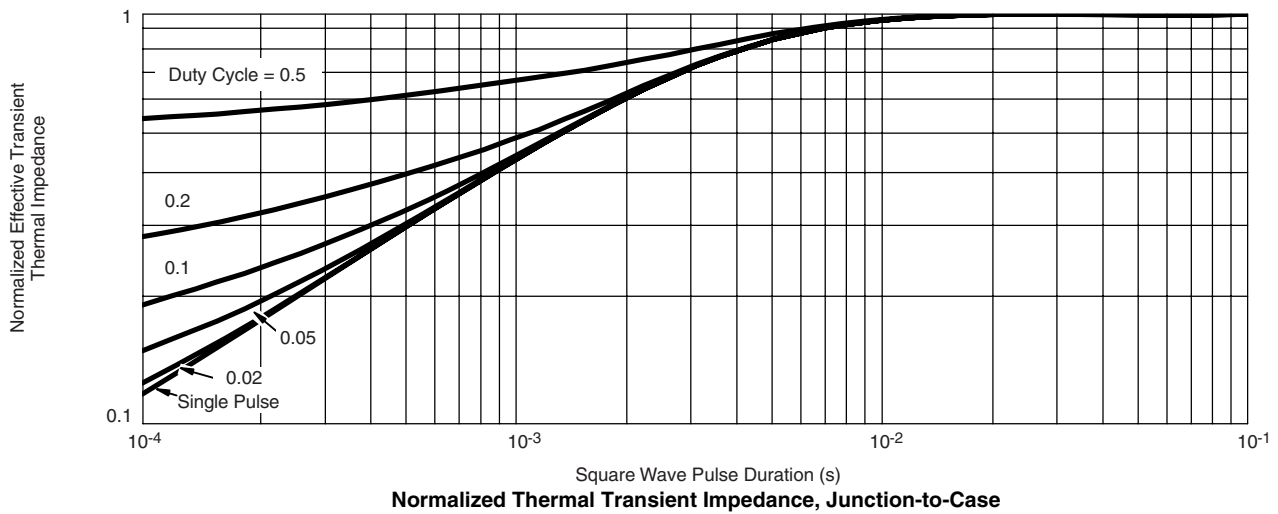
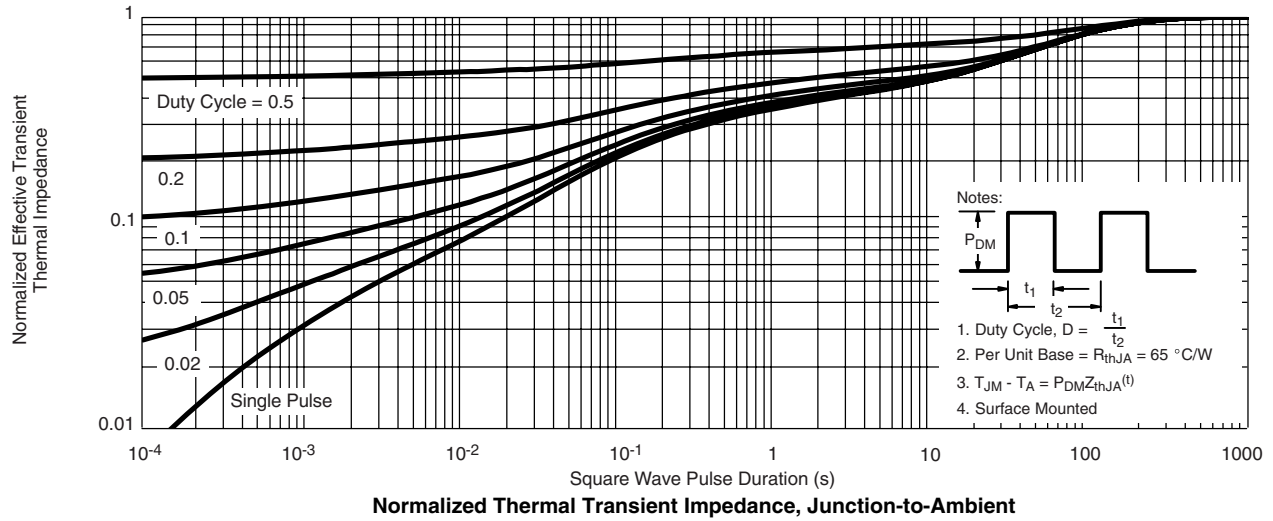
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiA417DJ

Vishay Siliconix

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

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