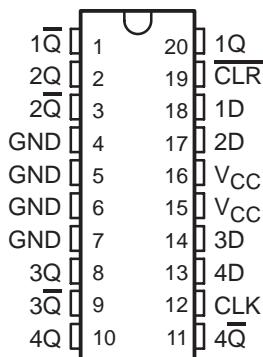


- Inputs Are TTL-Voltage Compatible
- Buffered Clock and Direct Clear Inputs
- Applications Include: Buffer/Storage Registers, Shift Registers, Pattern Generators
- Fully-Buffered Outputs for Maximum Isolation From External Disturbances
- Flow-Through Architecture to Optimize PCB Layout
- Center-Pin V<sub>CC</sub> and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR N PACKAGE  
(TOP VIEW)



### description

This device contains six D-type flip-flops and is positive-edge-triggered with a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The 74AC11175 is characterized for operation from – 40°C to 85°C.

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUTS	
CLR	CLK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q <sub>0</sub>	$\bar{Q}_0$

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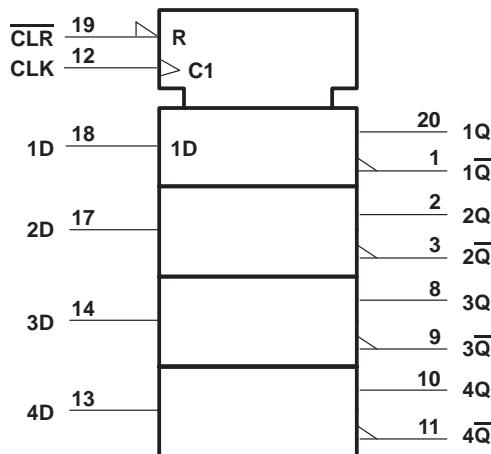
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# 74ACT11175

## QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

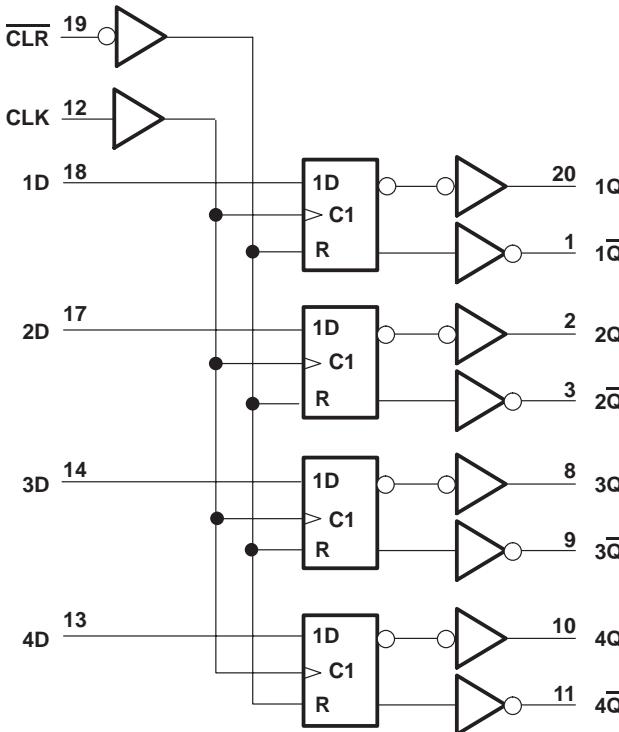
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	± 20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	± 50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	± 50 mA
Continuous current through $V_{CC}$ or GND .....	± 200 mA
Storage temperature range .....	-65°C to 150°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

74ACT11175  
QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

SCAS089 – D3385, DECEMBER 1989 – REVISED APRIL 1993

**recommended operating conditions**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		-24	mA
$I_{OL}$	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ C$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu A$	4.5 V	4.4		4.4	V		
		5.5 V	5.4		5.4			
	$I_{OH} = -24 mA$	4.5 V	3.94		3.8			
		5.5 V	4.94		4.8			
	$I_{OH} = -75 mA^\dagger$	5.5 V			3.85			
$V_{OL}$	$I_{OL} = 50 \mu A$	4.5 V		0.1	0.1	V		
		5.5 V		0.1	0.1			
	$I_{OL} = 24 mA$	4.5 V		0.36	0.44			
		5.5 V		0.36	0.44			
	$I_{OL} = 75 mA^\dagger$	5.5 V			1.65			
$I_I$	$V_I = V_{CC}$ or GND	5.5 V		$\pm 0.1$	$\pm 1$	$\mu A$		
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		8	80	$\mu A$		
$\Delta I_{CC}^\ddagger$	One input at 3.4 V, Other inputs at GND or $V_{CC}$	5.5 V		0.9	1	mA		
$C_i$	$V_I = V_{CC}$ or GND	5 V		4		pF		

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .

**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5 V \pm 0.5 V$  (unless otherwise noted) (see Figure 1)**

		$T_A = 25^\circ C$		MIN	MAX	UNIT
		MIN	MAX			
$f_{clock}$	Clock frequency	0	100	0	100	MHz
$t_w$	Pulse duration	$\overline{CLR}$ low	5	5		ns
		CLK high or low	5	5		
$t_{su}$	Setup time before CLK↑	Data	5	5		ns
		$\overline{CLR}$ inactive	5	5		
$t_h$	Hold time, data after CLK↑		0.5	0.5		ns

# 74ACT11175 QUADRUPLE D-TYPE FLIP-FLOP WITH CLEAR

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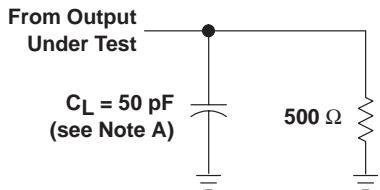
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TA = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f <sub>max</sub>			100	130	100	100	100	MHz
t <sub>PLH</sub>	CLR	Any Q	2.5	5.4	7.4	2.5	8.1	ns
		Any $\bar{Q}$	2.5	5.4	7.4	2.5	8.1	
t <sub>PHL</sub>	CLR	Any Q	3.1	7.6	9.9	3.1	10.9	ns
		Any $\bar{Q}$	3.1	7.6	9.9	3.1	10.9	
t <sub>PLH</sub>	CLK	Any Q	3	5.3	6.9	3	7.5	ns
		Any $\bar{Q}$	3	5.3	6.9	3	7.5	
t <sub>PHL</sub>	CLK	Any Q	3.3	7.2	9.2	3.3	10.1	ns
		Any $\bar{Q}$	3.3	7.2	9.2	3.3	10.1	

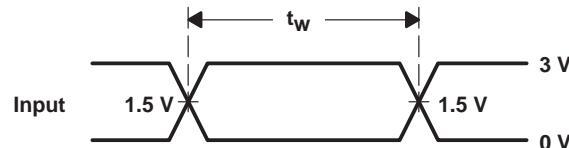
operating characteristics, V<sub>CC</sub> = 5 V, TA = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	C <sub>L</sub> = 50 pF, f = 1 MHz	42	pF

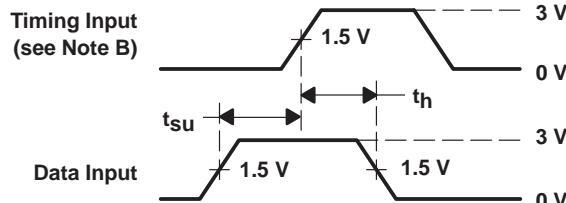
## PARAMETER MEASUREMENT INFORMATION



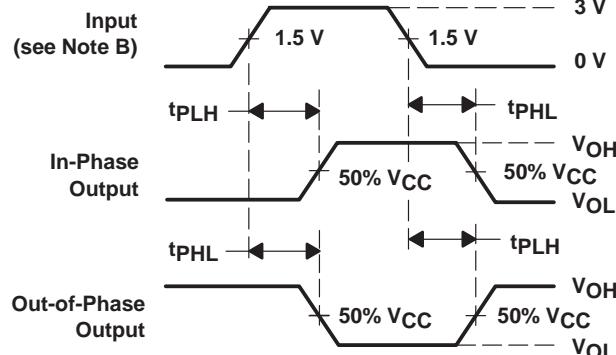
LOAD CIRCUIT



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , t<sub>r</sub> = 3 ns, t<sub>f</sub> = 3 ns.  
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ACT11175DW	OBsolete	SOIC	DW	20		TBD	Call TI	Call TI
74ACT11175N	OBsolete	PDIP	N	20		TBD	Call TI	Call TI
74ACT11175N	OBsolete	PDIP	N	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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