71M6543FT/71M6543HT/ 71M6543GT/71M6543GHT

Energy Meter ICs

General Description

The 71M6543FT/71M6543HT/71M6543GT/71M6543GHT (71M654xT) are 4th-generation three-phase metering systems-on-chips (SoCs) with a 5MHz, 8051-compatible MPU core, low-power RTC with digital temperature compensation, flash memory, and LCD driver. Our Single Converter Technology® with a 22-bit delta-sigma ADC, seven analog inputs, digital temperature compensation, precision voltage reference, and a 32-bit computation engine (CE) support a wide range of metering applications with very few external components.

The 71M654xT devices support optional interfaces to the Maxim Integrated 71M6x03 series of isolated sensors offering BOM cost reduction, immunity to magnetic tamper, and enhanced reliability. Other features include an SPI interface, advanced power management, ultra-low-power operation in active and battery modes, 5KB shared RAM, and 64KB/128KB flash memory that can be programmed in the field with code and/or data during meter operation and the ability to drive up to six LCD segments per SEG driver pin. High processing and sampling rates combined with differential inputs offer a powerful platform for residential meters.

A complete array of code development tools, demonstration code, and reference designs enable rapid development and certification of meters that meet all ANSI and IEC electricity metering standards worldwide.

The 71M654xT family operates over the industrial temperature range and comes in a 100-pin lead(Pb)-free LQFP package.

Applications

- Three-Phase Residential, Commercial, and Industrial Energy Meters

***Ordering Information* and *Typical Operating Circuit* appear at end of data sheet.**

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MICROWIRE is a registered trademark of National Semiconductor Corp.

Benefit and Features

- SoC Integration and Unique Isolation Technique Reduces BOM Cost Without Sacrificing Performance
  - 0.1% Typical Accuracy Over 2000:1 Current Range
  - Exceeds IEC 62053/ANSI C12.20 Standards
  - Four-Quadrant Metering
  - 46-64Hz Line Frequency Range with the Same Calibration
  - Phase Compensation (±10º)
  - Independent 32-Bit Compute Engine
  - 64KB Flash, 5KB RAM (71M6543FT/71M6543HT)
  - 128KB Flash, 5KB RAM (71M6543GT/71M6543GHT)
  - Built-In Flash Security
  - SPI Interface with Flash Program Capability
  - Up to Four Pulse Outputs with Pulse Count
  - 8-Bit MPU (80515), Up to 5 MIPS
  - Full-Speed MPU Clock in Brownout Mode
  - LCD Driver Allows Up to 6 Commons/Up to 56 Pins
  - Up to 51 Multifunction DIO Pins
  - Hardware Watchdog Timer (WDT)
  - Two UARTs for IR and AMR
  - IR LED Driver with Modulation
  - I²C/MICROWIRE® EEPROM Interface
- Innovative Isolation Technology (Requires Companion 71M6xxx Sensor, also from Maxim Integrated) Eliminates Current Transformers
  - Four Current Sensor Inputs with Selectable Differential Mode
  - Selectable Gain of 1 or 8 for One Current Input to Support Neutral Current Shunt
  - High-Speed Wh/VARh Pulse Outputs with Programmable Width
- Digital Temperature Compensation Improves System Performance
  - Metrology Compensation
  - Accurate RTC for TOU Functions with Automatic Temperature Compensation for Crystal in All Power Modes
- Power Management Extends Battery Life During Power Outages
  - Three Battery-Backup Modes:
    Brownout Mode (BRN)
    LCD Mode (LCD)
    Sleep Mode (SLP)
  - Wake-Up on Pin Events and Wake-On Timer
  - 1µA in Sleep Mode

19-6720; Rev 6; 1/15

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Absolute Maximum Ratings

(All voltages referenced to GNDA.)

Supplies and Ground Pins

$V_{V3P3SYS}$, V_{V3P3A}.....-0.5V to +4.6V
V_{BAT}, V_{BAT_RTC}.....-0.5V to +4.6V
GNDD.....-0.1V to +0.1V

Analog Output Pins

V_{REF}.....-10mA to +10mA, -0.5V to (V_{V3P3A} + 0.5V)
V_{DD}.....-10mA to +10mA, -0.5V to +3.0V
V_{V3P3D}.....-10mA to +10mA, -0.5V to +4.6V
V_{LCD}.....-10mA to +10mA, -0.5V to +6.0V

Analog Input Pins

IADC0-7, VADC8-10.....-10mA to +10mA, -0.5V to (V_{V3P3A} + 0.5V)
XIN, XOUT.....-10mA to +10mA, -0.5V to +3.0V

SEG and SEGDIO Pins

Configured as SEG or COM Drivers..-1mA to +1mA, -0.5V to +6.0V
Configured as Digital Inputs....-10mA to +10mA, -0.5V to +6.0V
Configured as Digital Outputs.....-10mA to +10mA, -0.5V to (V_{V3P3D} + 0.5V)

Digital Pins

Inputs (PB, RESET, RX, ICE_E, TEST).....-10mA to +10mA, -0.5V to +6.0V
Outputs (TX)..... -10mA to +10mA, -0.5V to (V_{V3P3D} + 0.5V)

Temperature

Operating Junction Temperature (peak, 100ms).....+140°C
Operating Junction Temperature (continuous).....+125°C
Storage Temperature..... -45°C to +140°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS					
$V_{V3P3SYS}$ and V_{V3P3A} Supply Voltage	Precision metering operation	3.0		3.6	V
V_{BAT}	PLL_FAST = 1	2.65		3.8	V
	PLL_FAST = 0	2.40		3.8	
V_{BAT_RTC}		2.0		3.8	V
Operating Temperature		-40		+85	°C
INPUT LOGIC LEVELS					
Digital High-Level Input Voltage (V_{IH})		2			V
Digital Low-Level Input Voltage (V_{IL})				0.8	V
Input Pullup Current, (I_{IL}) E_RTXT, E_RST, E_TCLK		10		100	µA
Input Pullup Current, (I_{IL}) OPT_RX, OPT_TX		10		100	µA
Input Pullup Current, (I_{IL}) SPI_CSZ (SEGDIO36)		10		100	µA
Input Pullup Current, (I_{IL}) Other Digital Inputs		-1		+1	µA
Input Pulldown Current (I_{IH}), ICE_E, RESET, TEST		10		100	µA
Input Pulldown Current, (I_{IH}) Other Digital Inputs		-1		+1	µA

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT LOGIC LEVELS					
Digital High-Level Output Voltage (V_{OH})	I_{LOAD} = 1mA	V_{V3P3D} - 0.4			V
	I_{LOAD} = 15mA (Note 1)	V_{V3P3D} - 0.8			V
Digital Low-Level Output Voltage (V_{OL})	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 15mA (Note 1)	0		0.8	V
BATTERY MONITOR **Battery Voltage Equation: 3.3 + (BSENSE - BNOM3P3) x 0.0252 + STEMP x 2.79E-5 V**					
Measurement Error	V_{BAT} = 2.0V	-3.5		+3.5	%
	V_{BAT} = 2.5V	-3.5		+3.5	
	V_{BAT} = 3.0V	-3.0		+3.0	
	V_{BAT} = 3.8V	-3.0		+3.0	
Input Impedance		260			kΩ
Passivation Current	I_{BAT}(BCURR = 1) - I_{BAT}(BCURR = 0)	50	100	165	µA
TEMPERATURE MONITOR					
Temperature Measurement Equation		22.15 + STEMP x 0.085 - 0.0023 x STEMP x [(STEMP$_{T85P}$ -STEMP$_{T22P}$) /(T_{85P} - T_{22P}) - 12.857]			°C
Temperature Error (Note 1)	T_A = +85°C	-3.2		+3.2	°C
	T_A = 0°C to +70°C	-2.65		+2.65	
	T_A = -20°C	-3.4		+3.4	
	T_A = -40°C	-3.8		+3.8	
V_{BAT_RTC} Charge per Measurement			2		µC
Duration of Temperature Measurement after TEMP_START			22	40	ms
SUPPLY CURRENT					
V_{V3P3A} + $V_{V3P3SYS}$ Supply Current (Note 1)	V_{V3P3A} = $V_{V3P3SYS}$ = 3.3V; MPU_DIV = 3 (614kHz MPU clock); PLL_FAST = 1; PRE_E = 0		7.2	8.5	mA
	PLL_FAST = 0		2.9	3.8	
	PRE_E = 1		7.3	8.7	
	PLL_FAST = 0, PRE_E = 1		3.0	3.9	
Dynamic Current			0.4	0.6	mA/MHz

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BAT} Current	Mission mode		-300		+300	nA
	Brownout mode			2.4	3.2	mA
	LCD mode (external V_{LCD})			0.4	108	nA
	LCD mode (internal V_{LCD} from DAC)			3.0	16	µA
	LCD mode (V_{BAT})			1.4	3.8	µA
	Sleep mode		-300		+300	nA
V_{BAT_RTC} Current	Brownout mode			400	650	nA
	LCD mode			1.8	4.1	µA
	Sleep mode, $T_A \le 25°C$			0.7	1.7	µA
	Sleep mode, T_A = 85°C (Note 1)			1.5	3.2	µA
Flash Write Current	Maximum flash write rate			7.1	9.3	mA
V_{V3P3D} SWITCH						
On-Resistance	$V_{V3P3SYS}$ to V_{V3P3D}, $I_{V3P3D} \le 1mA$				11	Ω
	V_{BAT} to V_{V3P3D}, $I_{V3P3D} \le 1mA$				11	
I_{OH}			9			mA
INTERNAL POWER FAULT COMPARATOR						
Response Time	100mV overdrive, falling		20		200	µs
	100mV overdrive, rising				200	
Falling Threshold, 3.0V Comparator			2.83	2.93	3.03	V
Falling Threshold, 2.8V Comparator			2.71	2.81	2.91	V
Difference between 3.0V and 2.8V comparators			47	136	220	mV
Falling Threshold, 2.25V Comparator			2.14	2.33	2.51	V
Falling Threshold, 2.0V Comparator			1.90	2.07	2.23	V
Difference between 2.25V and 2.0V Comparators			0.15	0.25	0.365	V
Hysteresis	T_A = +22°C	3.0V comparator	13	45	81	mV
		2.8V comparator	17	42	79	
		2.25V comparator	7	33	71	
		2.0V comparator	4	28	83	
2.5V REGULATOR						
V_{V2P5} Output Voltage	V_{V3P3} = 3.0V to 3.8V, I_{LOAD} = 0mA		2.55	2.65	2.75	V
V_{V2P5} Load Regulation	V_{BAT} = 3.3V, V_{V3P3} = 0V, I_{LOAD} = 0mA to 1mA				40	mV
Dropout Voltage	I_{LOAD} = 5mA				440	mV
	I_{LOAD} = 0mA				200	
PSSR	I_{LOAD} = 0mA			5		mV/V

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR					
Maximum Output Power to Crystal				1	µW
PLL					
PLL Settling Time	Power-up		3		ms
	PLL_FAST transition, low to high		3		
	PLL_FAST transition, high to low		3		
	Mode transition, sleep to mission		3		
LCD					
V_{LCD} Current	V_{LCD} = 3.3V, LCD frequency = 512Hz, all segments on		8.1		µA
	V_{LCD} = 3.3V, LCD frequency = 256Hz, all segments on		4.6		
	V_{LCD} = 3.3V, all segments off			2.1	
	V_{LCD} = 5.0V, LCD frequency = 512Hz, all segments on		12.0		
	V_{LCD} = 5.0V, LCD frequency = 256Hz, all segments on		4.6		
	V_{LCD} = 5.0V, all segments off			3.0	
V_{REF}					
V_{REF} Output Voltage	T_A = +22°C	1.193	1.195	1.197	V
V_{REF} Output Impedance	I_{LOAD} = -10µA to +10µA			3.2	kΩ
V_{REF} Power Supply Sensitivity	V_{V3P3A} = 3.0V to 3.6V	-1.5		+1.5	mV/V
V_{REF} Temperature Sensitivity (Note 1)		$V_{REFT} = V_{REF22} + (T-22)TC_1 + (T-22)^2TC_2$			V
	71M6543FT/71M6543GT	TC_1 = 151 - 2.77 x TRIMT			µV/°C
	71M6543HT/71M6543GHT	TC_1 = 33.264 + 0.08 x TRIMT + 1.587 x (TRIMBGB - TRIMBGD)			µV/°C
		TC_2 = -0.528 - 0.00128 x TRIMT			µV/°C²
V_{REF} Error (Note 1)	71M6543FT/71M6543GT (-40°C to +85°C)	-40		+40	ppm/°C
	71M6543HT/71M6543GHT (-40°C to -20°C)	-16		+16	
	71M6543HT/71M6543GHT (-20°C to +85°C)	-10		+10	
ADC					
Recommended Input Range (All Analog Inputs, Relative to V_{V3P3A})		-250		+250	mV Peak
Recommended Input Range, IADC0-IADC1, Preamp Enabled		-31.25		+31.25	mV Peak
Input Impedance	f_{IN} = 65Hz	40		100	kΩ
ADC Gain Error vs. Power Supply	V_{IN} = 200mV peak, 65Hz, V_{V3P3A} = 3.0V to 3.6V	-30		+70	ppm/%

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	Differential or single-ended modes	-10		+10	mV
THD	250mV peak, 65Hz, 64k points, Blackman-Harris window, FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		-93		dB
	20mV peak, 65Hz, 64k points, Blackman-Harris window, FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		-90		
LSB Size	FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		151		nV
Digital Full Scale	FIR_LEN = 2, ADC_DIV = 1, PLL_FAST = 1, MUX_DIV = 2		±2,097,152		LSB
PREAMPLIFIER					
Differential Gain		7.88	7.98	8.08	V/V
Gain Variation vs. Temperature	T_A = -40°C to +85°C (Note 1)	-30	-10	+15	ppm/°C
Gain Variation vs. V3P3	V_{V3P3} = 2.97V to 3.63V (Note 1)	-100		+100	ppm/%
Phase Shift	(Note 1)	+10		+22	m°
Preamp Input Current		3	6	9	µA
THD, Preamp + ADC	V_{IN} = 30mV		-88		dB
	V_{IN} = 15mV		-88		
Preamp Input Offset Voltage	IADC0 = IADC1 = V_{V3P3} + 30mV		-0.63		mV
	IADC0 = IADC1 = V_{V3P3} + 15mV		-0.57		
	IADC0 = IADC1 = V_{V3P3}		-0.56		
	IADC0 = IADC1 = V_{V3P3} - 15mV		-0.56		
	IADC0 = IADC1 = V_{V3P3} - 30mV		-0.55		
Phase Shift Over Temperature	(Note 1)	-0.03		+0.03	m°/C
FLASH MEMORY					
Endurance		20,000			Cycles
Data Retention	T_A = +25°C	100			Years
Byte Writes Between Erase Operations				2	Cycles
Write Time, per byte	Per 2 bytes if using SPI			50	µs
Page Erase Time				22	ms
Mass Erase Time				22	ms
SPI					
Data-to-Clock Setup Time		10			ns
Data Hold Time From Clock		10			ns
Output Delay, Clock to Data				40	ns

Electrical Characteristics (continued)

(Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

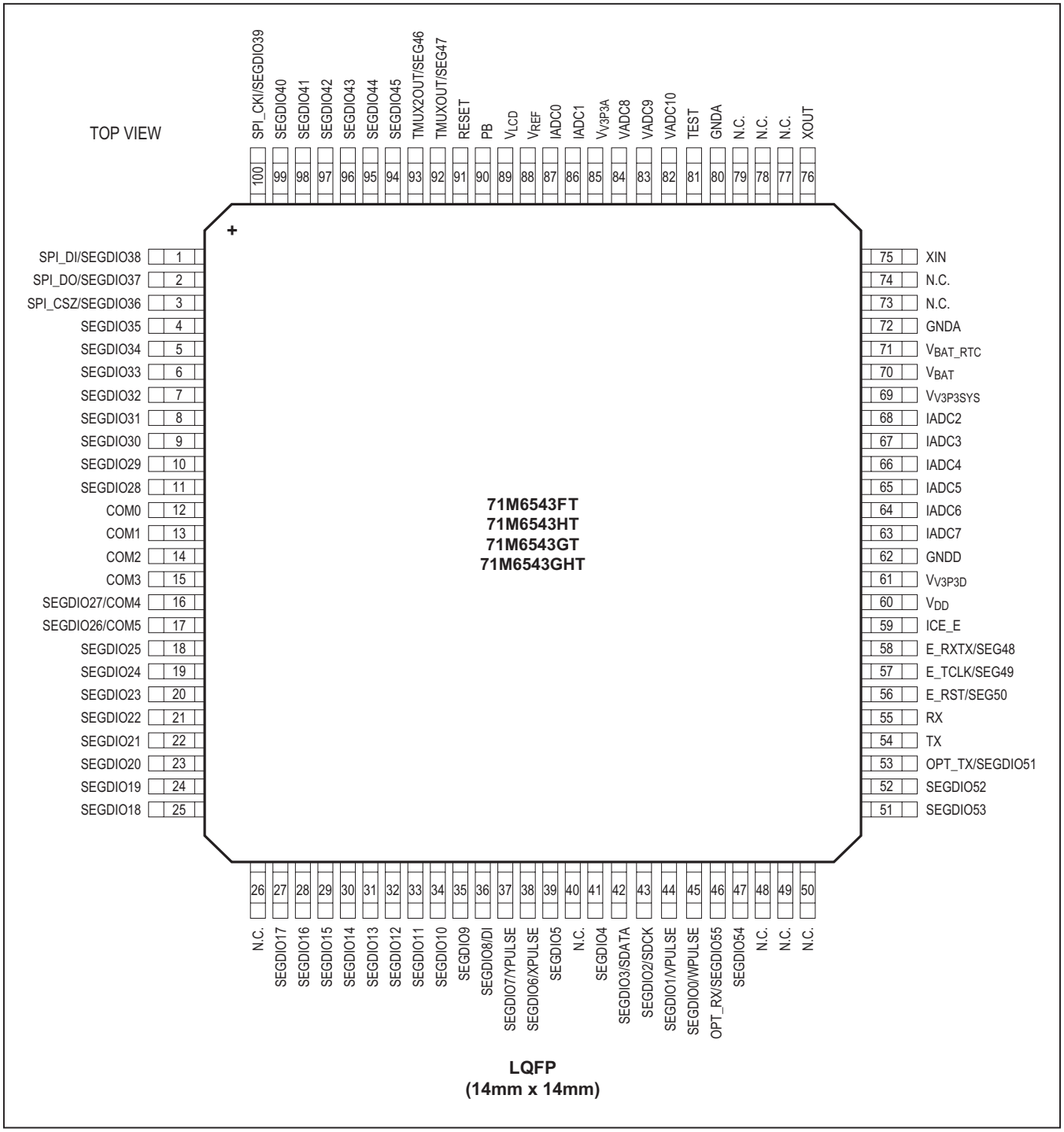
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CS-to-Clock Setup Time		10			ns
Hold Time, CS to Clock		15			ns
Clock High Period		40			ns
Clock Low Period		40			ns
Clock Frequency (as a multiple of CPU frequency)				2.0	MHz/MHz
Space between SPI Transactions		4.5			CPU Cycles
EEPROM INTERFACE					
I2C SCL Frequency	MPU clock = 4.9MHz, using interrupts		310		kHz
	MPU clock = 4.9MHz, bit-banging DIO2-DIO3		100		
3-Wire Write Clock Frequency	MPU clock = 4.9MHz, PLL_FAST = 0		160		kHz
	MPU clock = 4.9MHz, PLL_FAST = 1		490		
RESET					
Reset Pulse Width	(Note 1)	5			µs
Reset Pulse Fall Time	(Note 1)			1	µs
INTERNAL CALENDAR					
Year Date Range		2000		2255	Years

Recommended External Components

NAME	FROM	TO	FUNCTION	VALUE	UNITS
C1	V_{V3P3A}	GNDA	Bypass capacitor for 3.3V supply	≥ 0.1 ±20%	µF
C2	V_{V3P3D}	GNDD	Bypass capacitor for 3.3V output	0.1 ±20%	µF
CSYS	$V_{V3P3SYS}$	GNDD	Bypass capacitor for $V_{V3P3SYS}$	≥ 1.0 ±30%	µF
CVDD	V_{DD}	GNDD	Bypass capacitor for V_{DD}	0.1 ±20%	µF
CVLCD	V_{LCD}	GNDD	Bypass capacitor for V_{LCD} pin	≥ 0.1 ±20%	µF
XTAL	XIN	XOUT	32.768 kHz crystal; electrically similar to ECS .327-12.5-17X, Vishay XT26T or Suntsu SCP6–32.768kHz TR (load capacitance 12.5pF)	32.768	kHz
CXS (Note 2)	XIN	GNDA	Load capacitor values for crystal depend on crystal specifications and board parasitics. Nominal values are based on 3pF allowance for the sum of board and chip capacitances.	22 ±10%	pF
CXL (Note 2)	XOUT	GNDA		22 ±10%	pF

Note 1: Parameter not tested in production, guaranteed by design to six-sigma.
Note 2: If the capacitor values of CXS = 15pF and CXL = 10pF have already been installed, then changing the CXL value to 33pF and leaving CXS = 15pF would minimize rework.

Pin Configuration



Pin Descriptions

PIN 100	NAME	TYPE	CIRCUIT	FUNCTION
POWER AND GROUND PINS				
72, 80	GNDA	P	—	Analog Ground. This pin should be connected directly to the ground plane.
62	GNDD	P	—	Digital Ground. This pin should be connected directly to the ground plane.
85	V_{V3P3A}	P	—	Analog Power Supply. A 3.3V power supply should be connected to this pin. V_{V3P3A} must be the same voltage as $V_{V3P3SYS}$.
69	$V_{V3P3SYS}$	P	—	System 3.3V supply. This pin should be connected to a 3.3V power supply.
61	V_{V3P3D}	O	13	Auxiliary Voltage Output of the Chip. In mission mode, this pin is connected to $V_{V3P3SYS}$ by the internal selection switch. In BRN mode, it is internally connected to V_{BAT}. V_{V3P3D} is floating in LCD and sleep mode. A 0.1µF bypass capacitor to ground must be connected to this pin.
60	V_{DD}	O	—	Output of the 2.5V Regulator. This pin is powered in MSN and BRN modes. A 0.1µF bypass capacitor to ground should be connected to this pin.
89	V_{LCD}	O	—	Output of the LCD DAC. A 0.1µF bypass capacitor to ground should be connected to this pin.
70	V_{BAT}	P	12	Battery Backup Pin to Support the Battery Modes (BRN, LCD). A battery or super capacitor is to be connected between V_{BAT} and GNDD. If no battery is used, connect V_{BAT} to $V_{V3P3SYS}$.
71	V_{BAT_RTC}	P	12	RTC and Oscillator Power Supply. A battery or super capacitor is to be connected between V_{BAT} and GNDD. If no battery is used, connect V_{BAT_RTC} to $V_{V3P3SYS}$.
ANALOG PINS				
87, 86	IADC0 IADC1	I	6	Differential or Single-Ended Line Current Sense Inputs. These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. Unused pins must be tied to V_{V3P3A}. Pins IADC2-IADC3, IADC4-IADC5 and IADC6-IADC7 may be configured for communication with the remote sensor interface (71M6x03).
68, 67	IADC2 IADC3			
66, 65	IADC4 IADC5			
64, 63	IADC6 IADC7			
84, 83, 82	VADC8 (VA), VADC9 (VB), VADC10 (VC)	I	6	Line Voltage Sense Inputs. These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor-dividers. Unused pins must be tied to V_{V3P3A}.
88	V_{REF}	O	9	Voltage Reference for the ADC. This pin should be left unconnected (floating).
75	XIN	I	8	Crystal Inputs. A 32.768kHz crystal should be connected across these pins. Typically, a 22pF capacitor is also connected from XIN to GNDA and a 22pF capacitor is connected from XOUT to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer data sheet for details. If an external clock is used, a 150mV_{P-P} clock signal should be applied to XIN, and XOUT should be left unconnected.
76	XOUT	O		

Pin Descriptions (continued)

PIN 100	NAME	TYPE	CIRCUIT	FUNCTION
DIGITAL PINS				
12–15	COM0–COM3	O	5	LCD Common Outputs. These four pins provide the select signals for the LCD display.
45	SEGDIO0/WPULSE	I/O	3, 4, 5	Multiple-Use Pins. Configurable as either LCD segment driver or DIO. Alternative functions with proper selection of associated I/O RAM registers are: SEGDIO0 = WPULSE SEGDIO1 = VPULSE SEGDIO2 = SDCK SEGDIO3 = SDATA SEGDIO6 = XPULSE SEGDIO7 = YPULSE SEGDIO8 = DI SEGDIO16 = RX3 SEGDIO17 = TX3 Unused pins must be configured as outputs or terminated to V3P3/GNDD.
44	SEGDIO1/VPULSE			
43	SEGDIO2/SDCK			
42	SEGDIO3/SDATA			
41	SEGDIO4			
39	SEGDIO5			
38	SEGDIO6/XPULSE			
37	SEGDIO7/YPULSE			
36	SEGDIO8/DI			
35–30	SEGDIO[9:14]			
29–27	SEGDIO[15:17]			
25	SEGDIO[18]			
24–18	SEGDIO[19:25]			
11–4	SEGDIO[28:35]			
95–94	SEGDIO[44:45]			
99–96	SEGDIO[40:43]			
52	SEGDIO52			
51	SEGDIO53			
47	SEGDIO54			
17	SEGDIO26/COM5	I/O	3, 4, 5	Multiple-Use Pins. Configurable as either LCD segment driver or DIO with alternative function (LCD common drivers).
16	SEGDIO27/COM4			
3	SPI_CSZ/SEGDIO36	I/O	3, 4, 5	Multiple-Use Pins. Configurable as either LCD segment driver or DIO with alternative function (SPI interface).
2	SPI_DO/SEGDIO37			
1	SPI_DI/SEGDIO38			
100	SPI_CKI/SEGDIO39			
53	OPT_TX/SEGDIO51	I/O	3, 4, 5	Multiple-Use Pins, configurable as either LCD segment driver or DIO with alternative function (optical port/UART1)
46	OPT_RX/SEGDIO55			
58	E_RXTX/SEG48	I/O	1, 4, 5	Multiuse Pins. Configurable as either emulator port pins (when ICE_E pulled high) or LCD segment drivers (when ICE_E tied to GND).
56	E_RST/SEG50			
57	E_TCLK/SEG49	O	4, 5	
59	ICE_E	I	2	ICE Enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG50, SEG49, and SEG48, respectively. For production units, this pin should be pulled to GND to disable the emulator port.
92	TMUXOUT/SEG47	O	4, 5	Multiple-Use Pins. Configurable as either multiplexer/clock output or LCD segment driver using the I/O RAM registers.
93	TMUX2OUT/SEG46			
91	RESET	I	2	Chip Reset. This input pin is used to reset the chip into a known state. For normal operation, this pin is pulled low. To reset the chip, this pin should be pulled high. This pin has an internal 30FA (nominal) current source pulldown. No external reset circuitry is necessary.

Pin Descriptions (continued)

PIN 100	NAME	TYPE	CIRCUIT	FUNCTION
55	RX	I	3	UART0 Input. If this pin is unused it must be terminated to V_{V3P3D} or GNDD.
54	TX	O	4	UART0 Output
81	TEST	I	7	Enables Production Test. This pin must be grounded in normal operation.
90	PB	I	3	Pushbutton Input. This pin must be at GNDD when not active or unused. A rising edge sets the WF_PB flag. It also causes the part to wake up if it is in SLP or LCD mode. PB does not have an internal pullup or pulldown resistor.
26, 40, 48, 49, 50, 73, 74, 77, 78, 79, 84	N.C.	N.C.	—	No Connection. Do not connect these pins.

I = Input, O = Output, P = Power

I/O Equivalent Circuits

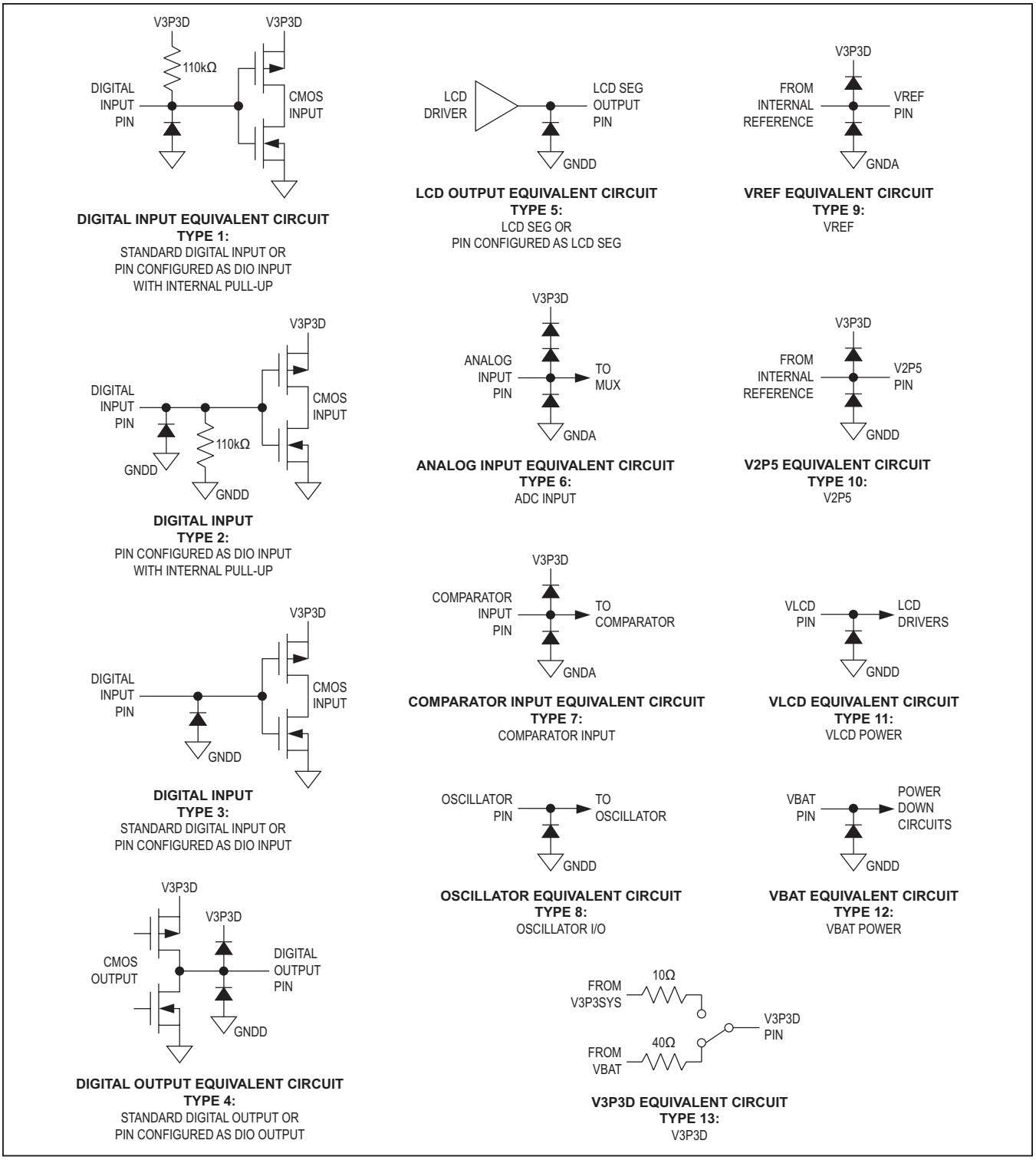
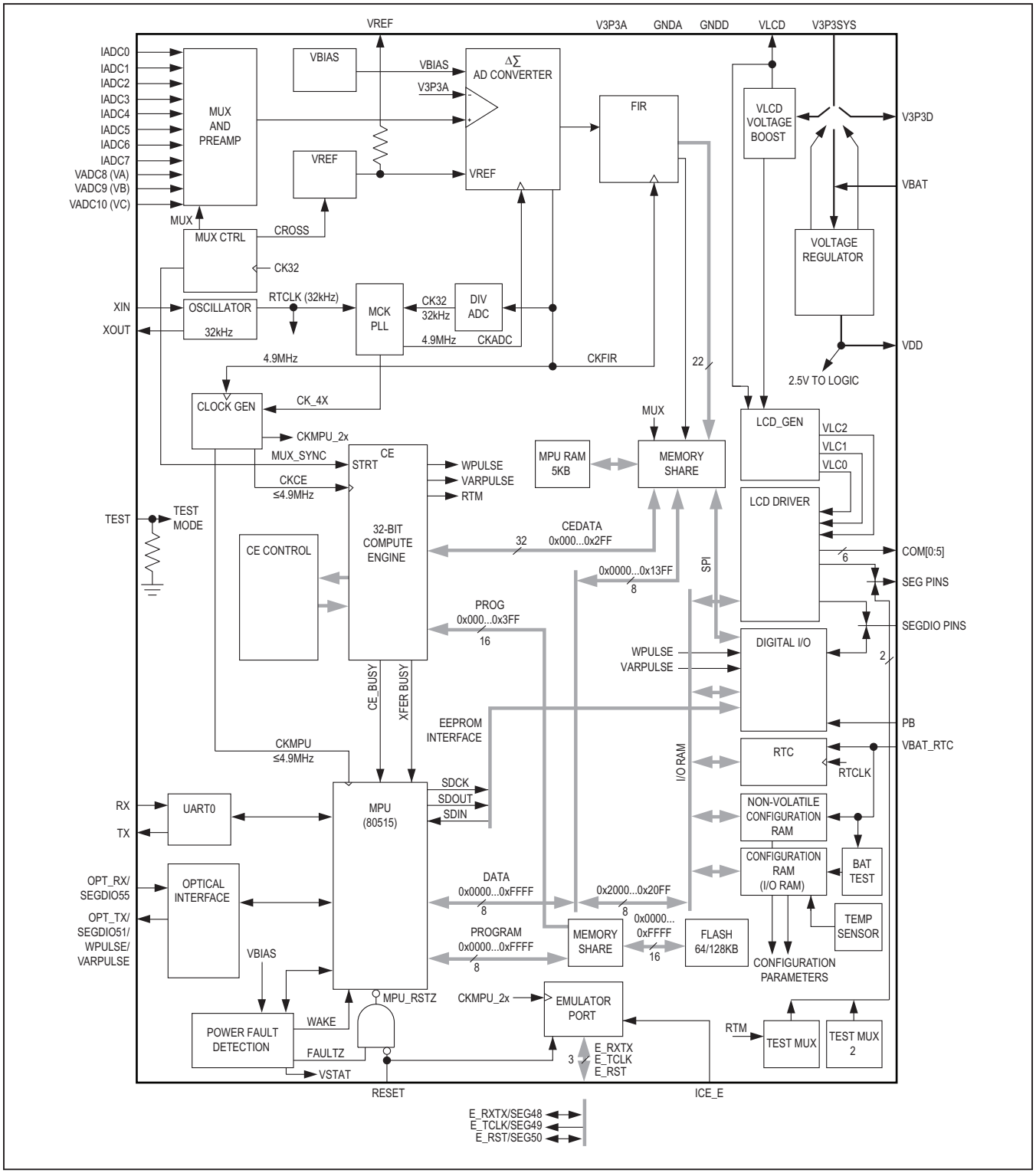


Figure 1. I/O Equivalent Circuits

Block Diagram



Hardware Description

The 71M6543FT/HT/GT/GHT single-chip energy meter ICs integrate all primary functional blocks required to implement a solid-state residential electricity meter. Included on the chip are the following:

- An analog front-end (AFE) featuring a 22-bit second-order sigma-delta ADC
- An independent 32-bit digital computation engine (CE) to implement DSP functions
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A precision voltage reference (V_{REF})
- A temperature sensor for digital temperature compensation:
  - Metrology digital temperature compensation (MPU)
  - Automatic RTC digital temperature compensation operational in all power states
- LCD drivers
- RAM and flash memory
- A real-time clock (RTC)
- A variety of I/O pins
- A power-failure interrupt
- A zero-crossing interrupt
- Selectable current sensor interfaces for locally-connected sensors as well as isolated sensors (i.e., using the 71M6x03 companion IC with a shunt resistor sensor)
- Resistive shunt and current transformers are supported

Resistive shunts and current transformer (CT) current sensors are supported. Resistive shunt current sensors may be connected directly to the 71M654xT device or isolated using a companion 71M6x03 isolator IC in order to implement a variety of metering configurations. An inexpensive, small pulse transformer is used to isolate the 71M6x03 isolated sensor from the 71M654xT. The 71M654xT performs digital communications bidirectionally with the 71M6x03 and also provides power to the 71M6x03 through the isolating pulse transformer. Isolated (remote) shunt current sensors are connected to the differential input of the 71M6x03. Included on the 71M6x03 companion isolator chip are:

- Digital isolation communications interface
- An analog front-end (AFE)
- A precision voltage reference (V_{REF})
- A temperature sensor (for digital temperature compensation)
- A fully differential shunt resistor sensor input
- A preamplifier to optimize shunt current sensor performance
- Isolated power circuitry obtains dc power from pulses sent by the 71M654xT

In a typical application, the 32-bit compute engine (CE) of the 71M654xT sequentially processes the samples from the voltage inputs on analog input pins and from the external 71M6x03 isolated sensors and performs calculations to measure active energy (Wh) and reactive energy (VARh), as well as A^2h, and V^2h for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the clock function allows the 71M6543FT/HT/GT/GHT to record time-of-use (TOU) metering information for multi-rate applications and to time-stamp tamper or other events. Measurements can be displayed on 3.3V LCDs commonly used in low-temperature environments. Flexible mapping of LCD display segments facilitate integration of existing custom LCDs. Design trade-off between the number of LCD segments and DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy, e.g., to meet the requirements of ANSI and IEC standards. Temperature-dependent external components such as crystal oscillator, resistive shunts, current transformers (CTs) and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce electricity meters with exceptional accuracy over the industrial temperature range.

One of the two internal UARTs is adapted to support an Infrared LED with internal drive and sense configuration and can also function as a standard UART. The optical output can be modulated at 38kHz. This flexibility makes it possible to implement AMR meters with an IR interface. A block diagram of the IC is shown in Figure 1.

Analog Front-End (AFE)

The AFE functions as a data acquisition system, controlled by the MPU. When used with locally connected sensors, as shown in Figure 2, the analog input signals (IADC0-IADC7, VADC8-VADC10) are multiplexed to the ADC input and sampled by the ADC.

The ADC output is decimated by the FIR filter and stored in CE RAM where it can be accessed and processed by the CE.

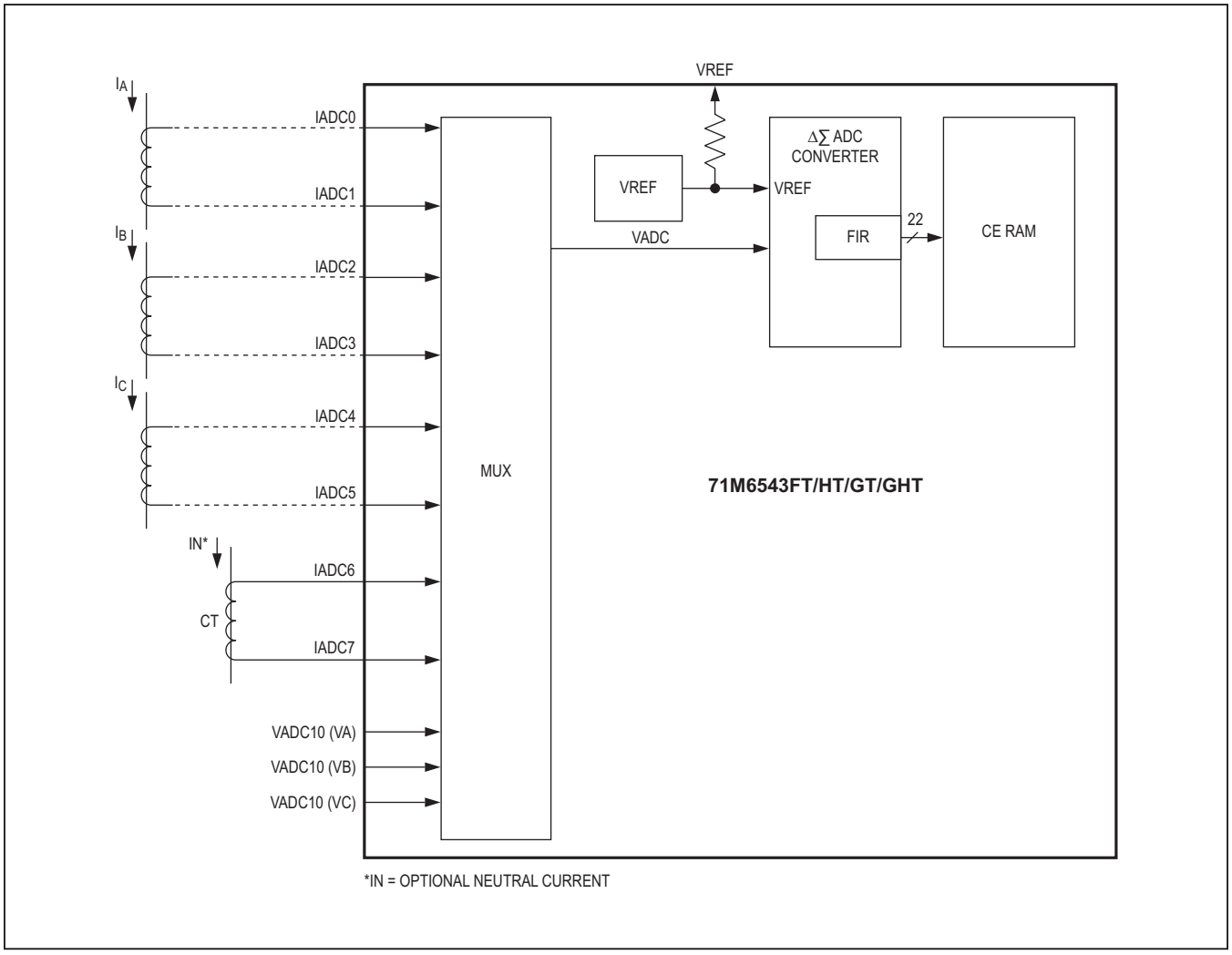


Figure 2. 71M6543FT/HT/GT/GHT Operating with Local Sensors

When remote isolated sensors are connected to the 71M6543FT/HT/GT/GHT using 71M6x03 remote sensor interfaces, the input multiplexer is bypassed. Instead, the extracted modulator bit stream is passed directly to a dedicated decimation filter. The output of the decimation filter is then directly stored in the appropriate CE RAM location without making use of a multiplexer cycle.

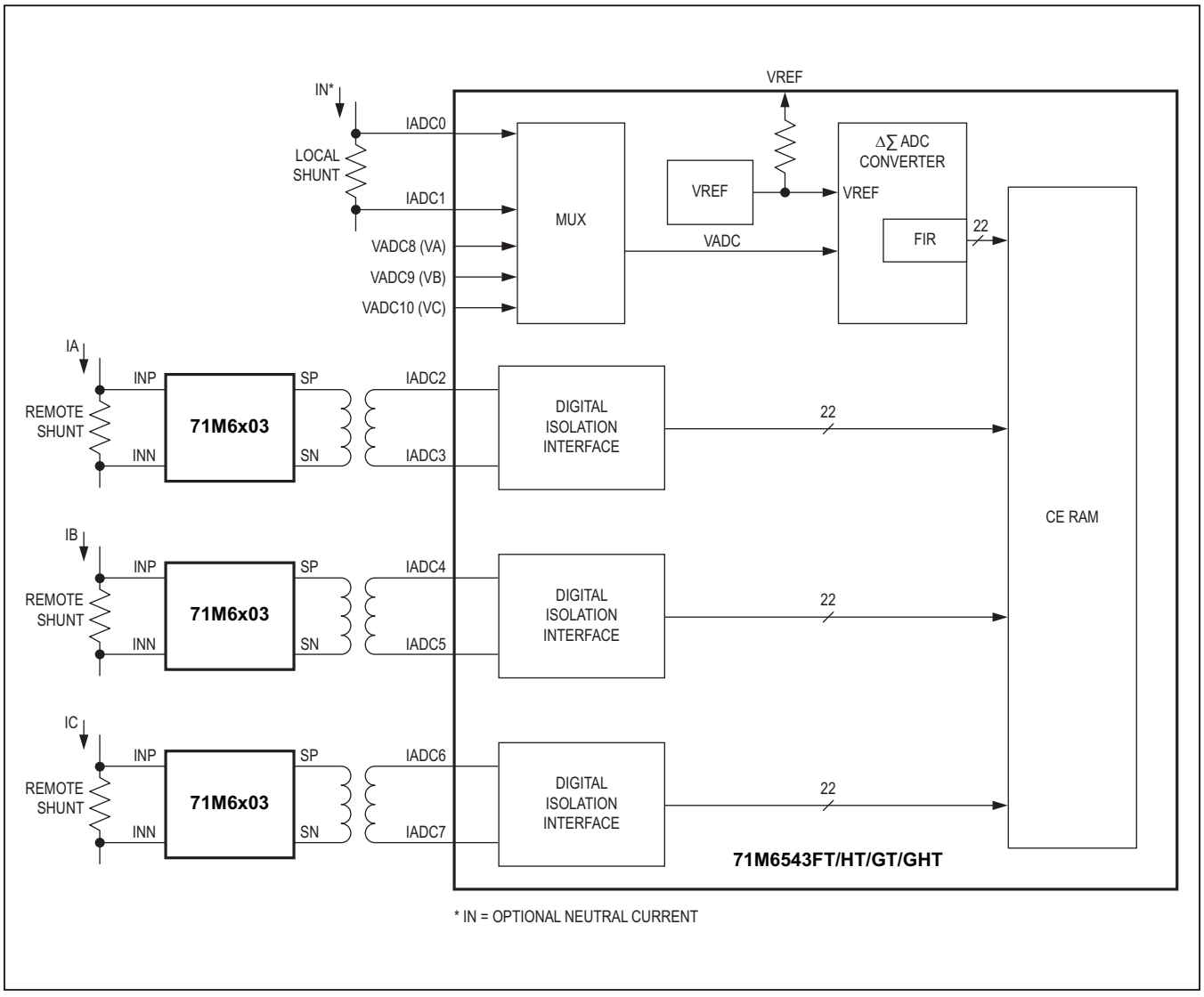


Figure 3. 71M6543FT/HT/GT/GHT Operating with Remote Sensor for Neutral Current

Signal Input Pins

The 71M6543FT/HT/GT/GHT features eleven ADC inputs.

IADC0-IADC7 are intended for use as current sensor inputs. These eight current sensor inputs can be configured as four single-ended inputs, or (more frequently) can be paired to form four differential inputs. For best performance, it is recommended to configure the current sensor inputs as differential inputs. The first differential input (IADC0-IADC1) features a preamplifier with a selectable gain of 1 or 8, and is intended for direct connection to a shunt resistor sensor, and can also be used with a current transformer (CT). The remaining differential pairs may be used with CTs, or may be enabled to interface to a remote 71M6x03 isolated current sensor providing isolation for a shunt resistor sensor using a low cost pulse transformer.

The remaining inputs (VADC8-VADC10) are single-ended and sense line voltage. These single-ended inputs are referenced to the V_{V3P3A} pin.

All analog signal input pins measure voltage. In the case of shunt current sensors, currents are sensed as a voltage drop in the shunt resistor sensor. Referring to Figure 2, shunt sensors can be connected directly to the 71M654xT (referred to as a 'local' shunt sensor) or connected via an isolated 71M6x03 (referred to as a 'remote' shunt sensor) (Figure 3). In the case of current transformers, the current is measured as a voltage across a burden resistor that is connected to the secondary winding of the CT. Meanwhile, line voltages are sensed through resistive voltage dividers.

Pins IADC0-IADC1 can be programmed individually to be differential or single-ended. For most applications IADC0-IADC1 are configured as a differential input to work with a shunt or CT directly interfaced to the IADC0-IADC1 differential input with the appropriate external signal conditioning components.

The performance of the IADC0-IADC1 pins can be enhanced by enabling a preamplifier with a fixed gain of 8. When the PRE_E bit = 1, IADC0-IADC1 become the inputs to the 8x preamplifier, and the output of this amplifier is supplied to the multiplexer. The 8x amplification is useful when current sensors with low sensitivity, such as shunt resistors, are used. With PRE_E set, the IADC0-IADC1 input signal amplitude is restricted to 31.25 mV peak.

When shunt resistors are used as current sense elements on all current inputs, the IADC0-IADC1 pins are configured for differential mode to interface to a local shunt by setting the DIFFA_E control bit. Meanwhile, the IADC2-IADC7 pins are re-configured as digital balanced pair to communicate with a 71M6x03 isolated sensor interface by setting the RMT_E control bit. The 71M6x03 communicates with the 71M654xT using a bidirectional digital data stream through an isolating low-cost pulse transformer. The 71M654xT also supplies power to the 71M6x03 through the isolating transformer.

When using current transformers the IADC2-IADC7 pins are configured as local analog inputs (RMT_E = 0). The IADC0-IADC1 pins cannot be configured as a remote sensor interface.

Input Multiplexer

When operating with local sensors, the input multiplexer sequentially applies the input signals from the analog input pins to the input of the ADC. One complete sampling sequence is called a multiplexer frame. The multiplexer of the 71M6543FT/HT/GT/GHT can select up to seven input signals (three voltage inputs and four current inputs) per multiplexer frame. The multiplexer always starts at state 1 and proceeds until as many states as determined by MUX_DIV[3:0] have been converted.

The 71M6543FT/HT/GT/GHT requires CE code that is written for the specific application. Moreover, each CE code requires specific AFE and MUX settings in order to function properly. Contact Maxim Integrated for specific information about alternative CE codes.

For a polyphase configuration with neutral current sensing using shunt resistor current sensors and the 71M6xx3 isolated sensors, as shown in Figure 3, the IADC0-IADC1 input must be configured as a differential input, to be connected to a local shunt. The local shunt connected to the IADC0-IADC1 input is used to sense the Neutral current. The voltage sensors (VADC8-VADC10) are also directly connected to the 71M6543FT/HT/GT/GHT and are also routed though the multiplexer. Meanwhile, the IADC2-IADC7 current inputs are configured as remote sensor digital interfaces and the corresponding samples are not routed through the multiplexer.

For a polyphase configuration with optional neutral current sensing using Current Transformer (CTs) sensors, all four current sensor inputs must be configured as differential inputs. IADC2-IADC3 is connected to phase A, IADC4-IADC5 is connected to phase B, and IADC6-IADC7 is connected to phase C. The IADC0-IADC1 current sensor input is optionally used to sense the Neutral current for anti-tampering purposes. The voltage sensors (VADC8-VADC10), typically resistive dividers, are directly connected to the 71M6543FT/HT/GT/GHT. No 71M6xx3 isolated sensors are used in this configuration and all signals are routed though the multiplexer.

The multiplexer sequence shown in Figure 4 corresponds to the configuration shown in Figure 3. The frame duration is 13 CK32 cycles (where CK32 = 32,768Hz), therefore, the resulting sample rate is 32,768 Hz/13 = 2,520.6Hz. Note that Figure 4 only shows the currents that pass through the 71M6543FT/HT/GT/GHT multiplexer, and does not show the currents that are copied directly into CE RAM from the remote sensors (see Figure 3), which are sampled during the second half of the multiplexer frame. The two unused conversion slots shown are necessary to produce the desired 2,520.6Hz sample rate.

The multiplexer sequence shown in Figure 5 corresponds to the CT configuration shown in Figure 2. Since in this case all current sensors are locally connected to the 71M6543FT/HT/GT/GHT, all currents are routed through the multiplexer, as seen in Figure 2. For this multiplexer sequence, the frame duration is 15 CK32 cycles (where CK32 = 32,768Hz), therefore, the resulting sample rate is 32,768 Hz/15 = 2,184.5Hz.

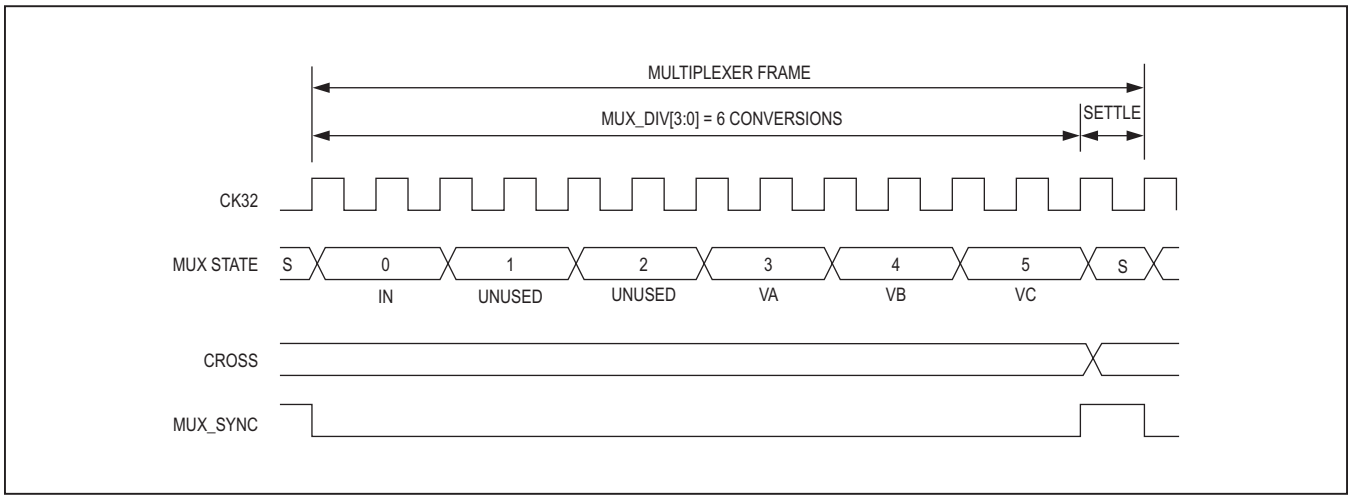


Figure 4. Multiplexer Sequence with Neutral Channel and Remote Sensors

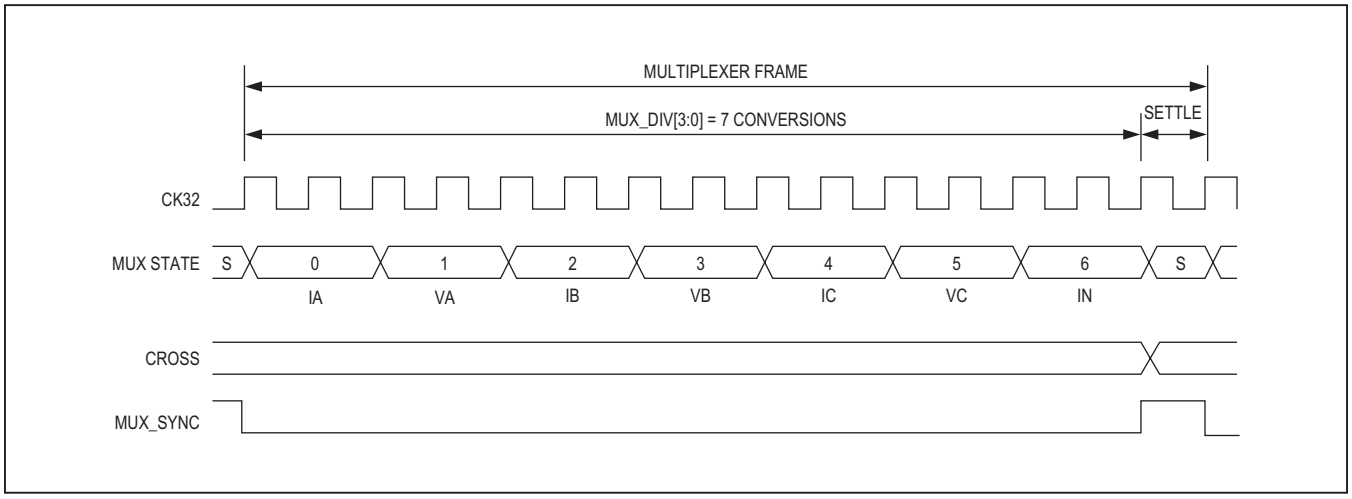


Figure 5. Multiplexer Sequence with Neutral Channel and Current Transformers

Table 1. ADC Input Configuration

PIN	REQUIRED SETTING	COMMENT
IADC0	DIFFx_E = 1	Differential mode must be selected with DIFFx_E = 1. The ADC results are stored in ADC0 and ADC1 is not disturbed.
IADC1		
IADC2	DIFFx_E = 1 or RMT_E = 1	For locally connected sensors the differential input must be enabled. For the remote sensor RMT_E must be set. ADC results are stored in ADC2 and ADC3 is not disturbed.
IADC3		
IADC4	DIFFx_E = 1 or RMT_E = 1	For locally connected sensors the differential input must be enabled. For the remote sensor RMT_E must be set. ADC results are stored in ADC4 and ADC5 is not disturbed.
IADC5		
IADC6	DIFFx_E = 1 or RMT_E = 1	For locally connected sensors the differential input must be enabled. For the remote sensor RMT_E must be set. ADC results are stored in ADC6 and ADC7 is not disturbed.
IADC7		
VADC8	—	Phase A voltage. Single ended mode only. ADC result stored in ADC8.
VADC9	—	Phase B voltage. Single ended mode only. ADC result stored in ADC9.
VADC10	—	Phase A voltage. Single ended mode only. ADC result stored in ADC10.

Delay Compensation

When measuring the energy of a phase (i.e., Wh and VARh) in a service, the voltage and current for that phase must be sampled at the same instant. Otherwise, the phase difference, Φ, introduces errors.

$$\varphi = \frac{t_{delay}}{T} \cdot 360° = t_{delay} \cdot f \cdot 360°$$

Where f is the frequency of the input signal, T = 1/f and t_{delay} is the sampling delay between current and voltage.

Traditionally, sampling is accomplished by using two A/D converters per phase (one for voltage and the other one for current) controlled to sample simultaneously. Our Single Converter Technology, however, exploits the 32-bit signal processing capability of its CE to implement “constant delay” allpass filters. The allpass filter corrects for the conversion time difference between the voltage and the corresponding current samples that are obtained with a single multiplexed A/D converter.

The “constant delay” allpass filter provides a broad-band delay 360° – θ, which is precisely matched to the difference in sample time between the voltage and the current of a given phase. This digital filter does not affect the amplitude of the signal, but provides a precisely controlled phase response.

The recommended ADC multiplexer sequence samples the current first, immediately followed by sampling of the corresponding phase voltage, thus the voltage is delayed by a phase angle Φ relative to the current. The delay compensation implemented in the CE aligns the voltage samples with their corresponding current samples by first delaying the current samples by one full sample interval (i.e., 360°), then routing the voltage samples through the allpass filter, thus delaying the voltage samples by 360o - θ, resulting in the residual phase error between the current and its corresponding voltage of B – Φ. The residual phase error is negligible, and is typically less than ±1.5 milli-degrees at 100Hz, thus it does not contribute to errors in the energy measurements.

When using remote sensors, the CE performs the same delay compensation described above to align each voltage sample with its corresponding current sample. Even though the remote current samples do not pass through the 71M654xT multiplexer, their timing relationship to their corresponding voltages is fixed and precisely known.

ADC Preamplifier

The ADC preamplifier is a low-noise differential amplifier with a fixed gain of 8 available only on the IADC0-IADC1 sensor input pins. A gain of 8 is enabled by setting PRE_E = 1. When disabled, the supply current of the preamplifier is < 10 nA and the gain is unity. With proper settings of the PRE_E and DIFFA_E (I/O RAM 0x210C[4]) bits, the preamplifier can be used whether or not differential mode is selected. For best performance, the differential mode is recommended. In order to save power, the bias current of the preamplifier and ADC is adjusted according to the ADC_DIV control bit (I/O RAM 0x2200[5]).

Analog-to-Digital Converter (ADC)

A single 2nd-order delta-sigma ADC digitizes the voltage and current inputs to the device. The resolution of the ADC, including the sign bit, is 21 bits (FIR_LEN[1:0] = 1), or 22 bits (FIR_LEN[1:0] = 2).

Initiation of each ADC conversion is controlled by MUX_CTRL internal circuit. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location determined by the multiplexer selection. FIR data is stored LSB justified, but shifted left 9 bits.

FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the fixed CE RAM location determined by the multiplexer selection.

Voltage References

A bandgap circuit provides the reference voltage to the ADC. The V_{REF} band-gap amplifier is chopper-stabilized to remove the dc offset voltage. This offset voltage is the most significant long-term drift mechanism in voltage reference circuits.

Isolated Sensor Interface

Nonisolating sensors, such as shunt resistors, can be connected to the inputs of the 71M654x via a combination of a pulse transformer and a 71M6x03 isolated sensor interface. The 71M6x03 receives power directly from the 71M654xT through a pulse transformer and does not require a dedicated power supply circuit. The 71M6x03 establishes 2-way communication with the 71M654xT, supplying current samples and auxiliary information such as sensor temperature via a serial data stream.

Up to three 71M6x03 isolated sensors can be supported by the 71M6543FT/HT/GT/GHT. When a remote sensor interface is enabled, the two analog current inputs become reconfigured as a digital remote sensor interface. Each 71M6x03 isolated sensor consists of the following building blocks:

- Power supply for power pulses received from the 71M654xT
- Digital communications interface
- Shunt signal preamplifier
- Delta-sigma ADC converter with precision bandgap reference (chopping amplifier)
- Temperature sensor
- Fuse system containing part-specific information

During an ordinary multiplexer cycle, the 71M654xT internally determines which other channels are enabled. At the same time, it decimates the modulator output from the 71M6x03 isolated sensors. Each result is written to CE RAM during one of its CE access time slots.

The ADC of the 71M6x03 derives its timing from the power pulses generated by the 71M654xT and as a result, operates its ADC slaved to the frequency of the power pulses. The generation of power pulses, as well as the communication protocol between the 71M654xT and 71M6x03 isolated sensor is automatic and transparent to the user.

The 71M654xT can read data and status from, and can write control information to the 71M6x03 isolated sensor. With hardware and trim-related information on each connected 71M6x03 isolated sensor available to the 71M6543FT/HT/GT/GHT, the MPU can implement temperature compensation of the energy measurement based on the individual temperature characteristics of the 71M6x03 isolated sensor.

Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all four channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.
- Scaling of samples based on temperature compensation information.

Meter Equations

The 71M6543FT/HT/GT/GHT provides hardware assistance to the CE in order to support various meter equations. The compute engine firmware for industrial configurations can implement the equations listed in Table 2. EQU[2:0] specifies the equation to be used based on the meter configuration and on the number of phases used for metering.

Table 2. Inputs Selected in Multiplexer Cycles

EQU	DESCRIPTION	Wh AND VARh FORMULA			RECOMMENDED MULTIPLEXER SEQUENCE
		ELEMENT 0	ELEMENT 1	ELEMENT 2	
2	2-element, 3W 3ph Delta	VA x IA	VA x IB	N/A	IA VA IB VB
3	2-element, 4W 3ph Delta	VA (IA-IB)/2	VC x IC	N/A	IA VA IB VB IC VC
4	2-element, 4W 3ph Wye	VA (IA-IB)/2	VB (IC-IB)/2	N/A	IA VA IB VB IC VC
5	3-element, 4W 3ph Wye	VA x IA	VB x IA	VC x IC	IA VA IB VB IC VC (ID)

Note: *Only EQU = 5 is supported by currently available CE code versions for the 71M6543FT/HT/GT/GHT. Contact your Maxim Integrated representative for CE codes that support equations 2, 3 and 4.*

Real-Time Monitor

The CE contains a real-time monitor (RTM), which can be programmed to monitor four selectable XRAM locations at full sample rate. The four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM can be enabled and disabled with control bit RTM_E. The RTM output is clocked by CKTEST. Each RTM word is clocked out in 35 CKCE cycles (1 CKCE cycle is equivalent to 203ns) and contains a leading flag bit.

Pulse Generators

The 71M6543FT/HT/GT/GHT provides four pulse generators, VPULSE, WPULSE, XPULSE and YPULSE, as well as hardware support for the VPULSE and WPULSE pulse generators. The pulse generators can be used to output CE status indicators (for example, voltage sag) to DIO pins. All pulses can be configured to generate interrupts to the MPU.

The polarity of the pulses may be inverted with control bit PLS_INV. When this bit is set, the pulses are active high, rather than the more usual active low. PLS_INV inverts all four pulse outputs.

The function of each pulse generator is determined by the CE code and the MPU code must configure the corresponding pulse outputs in agreement with the CE code. For example, standard CE code produces a mains zero-crossing pulse on XPULSE and a SAG pulse on YPULSE.

A common use of the zero-crossing pulses is to generate interrupt in order to drive real-time clock software in places where the mains frequency is sufficiently accurate to do so and also to adjust for crystal aging. A common use for the SAG pulse is to generate an interrupt that alerts the MPU when mains power is about to fail, so that the MPU code can store accumulated energy and other data to EEPROM before the $V_{V3P3SYS}$ supply voltage actually drops.

XPULSE and YPULSE

Pulses generated by the CE may be exported to the XPULSE and YPULSE pulse output pins. Pins SEGDIO6 and SEGDIO7 are used for these pulses, respectively. Generally, the XPULSE and YPULSE outputs can be updated once on each pass of the CE code.

VPULSE and WPULSE

By default, WPULSE emits a pulse proportional to real energy consumed, and VPULSE emits a pulse proportional to reactive energy. During each CE code pass the hardware stores exported WPULSE and VPULSE sign bits in an 8-bit FIFO and sends the buffered sign bits to the output pin at a specified, known interval. This permits the CE code to calculate the VPULSE and WPULSE outputs at the beginning of its code pass and to rely on hardware to spread them over the multiplexer frame.

80515 MPU Core

The 71M6543FT/HT/GT/GHT includes an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle: a 4.9MHz clock results in a processing throughput of 4.9 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally, a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single machine cycle (MPU clock cycle). This leads to an 8x average performance improvement (in terms of MIPS) over the 8051 device running at the same clock frequency.

The CKMPU frequency is a function of the MCK clock (19.6608MHz) divided by the MPU clock divider which is set in the I/O RAM control field MPU_DIV[2:0]. Actual processor clocking speed can be adjusted to the total processing demand of the application (metering calculations, AMR management, memory management, LCD driver management and I/O management) using MPU_DIV[2:0], as shown in Table 3.

Memory Organization and Addressing

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces. Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: program memory (flash, shared by MPU and CE), external RAM (data RAM, shared by the CE and MPU, configuration or I/O RAM), and internal data memory (internal RAM).

Table 3. CKMPU Clock Frequencies

MPU_DIV [2:0]	CKMPU FREQUENCY
000	4.9152MHz
001	2.4576MHz
010	1.2288MHz
011	614.4kHz
100	307.2kHz
101	
110	
111	

Program Memory

The 80515 can address up to 64KB of program memory space (0x0000 to 0xFFFF). Program memory is read when the MPU fetches instructions or performs a MOVC operation.

After reset, the MPU starts program execution from program memory location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from code space location 0x0003.

MPU External Data Memory (XRAM)

Both internal and external memory is physically located on the 71M654xT device. The external memory referred in this documentation is only external to the 80515 MPU core.

3KB of RAM starting at address 0x0000 is shared by the CE and MPU. The CE normally uses the first 1KB, leaving 2KB for the MPU. Different versions of the CE code use varying amounts. Consult the documentation for the specific code version being used for the exact limit.

Table 4. Memory Map

ADDRESS (hex)	MEMORY TECHNOLOGY	MEMORY TYPE	NAME	TYPICAL USAGE	MEMORY SIZE (BYTES)
0000-FFFF (64K) 0000-1FFFF (128K)	Flash Memory	Nonvolatile	Program memory for MPU and CE	MPU program and nonvolatile data	128/64K*
				CE program (on 1KB boundary)	3K max
0000-0BFF	Static RAM	Volatile	External RAM (XRAM)	Shared by CE and MPU	5K*
2000-27FF	Static RAM	Volatile	Configuration RAM (I/O RAM)	Hardware control	2K
2800-287F	Static RAM	Nonvolatile (battery)	Configuration RAM (I/O RAM)	Battery-buffered memory	128
0000-00FF	Static RAM	Volatile	Internal RAM	Part of 80515 Core	256

**Memory size depends on IC. See the On-Chip Resources section for details.*

Table 5. Internal Data Memory Map

ADDRESS RANGE		DIRECT ADDRESSING	INDIRECT ADDRESSING
0x80	0xFF	Special Function Registers (SFRs)	RAM
0x30	0x7F	Byte addressable area	
0x20	0x2F	Bit addressable area	
0x00	0x1F	Register banks R0…R7	

MOVX Addressing

There are two types of instructions differing in whether they provide an 8-bit or 16-bit indirect address to the external data RAM:

- MOVX A,@Ri: The contents of R0 or R1 in the current register bank provide the eight low-order address bits with the eight high-order bits specified by the PDATA SFR. This method allows the user paged access (256 pages of 256 bytes each) to all ranges of the external data RAM.
- MOVX A,@DPTR: The data pointer generates a 16-bit address. This form is faster and more efficient when accessing very large data arrays (up to 64KB) since no additional instructions are needed to set up the eight high ordered bits of the address.

It is possible to mix the two MOVX types. This provides the user with four separate data pointers, two with direct access and two with paged access, to the entire external memory range.

Dual Data Pointer

The Dual Data Pointer accelerates the block moves of data. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit, located in the LSB of the DPS register, chooses the active pointer. DPTR is selected when DPS[0] = 0 and DPTR1 is selected when DPS[0] = 1.

The user switches between pointers by toggling the LSB of the DPS register. The values in the data pointers are not affected by the LSB of the DPS register. All DPTR related instructions use the currently selected DPTR for any activity.

An alternative data pointer is available in the form of the PDATA register (SFR 0xBF), sometimes referred to as USR2). It defines the high byte of a 16-bit address when reading or writing XDATA with the instruction MOVX A,@ Ri or MOVX @Ri,A.

Internal Data Memory Map and Access

The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always 1 byte wide.

The Special Function Registers (SFR) occupy the upper 128 bytes. The SFR area of internal data memory is available **only by direct addressing**. Indirect addressing of this area accesses the upper 128 bytes of Internal RAM. The lower 128 bytes contain working registers and bit addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW, SFR 0xD0) select which bank is in use. The next 16 bytes form a block of bit addressable memory space at addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing.

Special Function Registers

Only a few addresses in the SFR memory space are occupied; other addresses are unimplemented. A read access to unimplemented addresses returns undefined data, while a write access has no effect. SFRs specific to the 71M654xT are shown in bold print on a shaded field. The registers at 0x80, 0x88, 0x90, etc., are bit addressable, all others are byte addressable.

Timers and Counters

The 71M6543FT/HT/GT/GHT contains two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle, i.e., it counts up once for every 12 periods of the MPU clock. In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from certain DIO pins, see 2.5.8 Digital I/O). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the clock frequency (CKMPU). There are no restrictions on the duty cycle, however to ensure proper recognition of the 0 or 1 state, an input should be stable for at least 1 machine cycle.

Table 6. Special Function Register Map

HEX/ BIN	BIT ADDRESSABLE	BYTE ADDRESSABLE							BIN/ HEX
	X000	X001	X010	X011	X100	X101	X110	X111	
F8	**INTBITS**	**VSTAT**			**RCMD**	**SPI_CMD**			FF
F0	B								F7
E8	**IFLAGS**								EF
E0	A								E7
D8	WDCON								DF
D0	PSW								D7
C8	T2CON								CF
C0	IRCON								C7
B8	IEN1	IP1	S0RELH	S1RELH				PDATA	BF
B0	**P3** (DIO12:15)		**FLSH_CTL**				**FLSH_ BANK**	**FLSH_ PGADR**	B7
A8	IEN0	IP0	S0RELL						AF
A0	**P2** (DIO8:11)								A7
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL	**EEDATA**	**EECTRL**	9F
90	**P1**(DIO4:7)		DPS		**FLSH_ ERASE**				97
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON		8F
80	**P0** (DIO0:3)	SP	DPL	DPH	DPL1	DPH1		PCON	87

Table 7. Generic 80515 SFRs: Location and Reset Values

NAME	ADDRESS	RESET VALUE	DESCRIPTION
P0	0x80	0xFF	Port 0
SP	0x81	0x07	Stack Pointer
DPL	0x82	0x00	Data Pointer Low 0
DPH	0x83	0x00	Data Pointer High 0
DPL1	0x84	0x00	Data Pointer Low 1
DPH1	0x85	0x00	Data Pointer High 1
PCON	0x87	0x00	UART Speed Control
TCON	0x88	0x00	Timer/Counter Control
TMOD	0x89	0x00	Timer Mode Control
TL0	0x8A	0x00	Timer 0, low byte
TL1	0x8B	0x00	Timer 1, high byte
TH0	0x8C	0x00	Timer 0, low byte
TH1	0x8D	0x00	Timer 1, high byte
CKCON	0x8E	0x01	Clock Control (Stretch = 1)
P1	0x90	0xFF	Port 1
DPS	0x92	0x00	Data Pointer select Register
S0CON	0x98	0x00	Serial Port 0, Control Register
S0BUF	0x99	0x00	Serial Port 0, Data Buffer
IEN2	0x9A	0x00	Interrupt Enable Register 2
S1CON	0x9B	0x00	Serial Port 1, Control Register
S1BUF	0x9C	0x00	Serial Port 1, Data Buffer

Table 7. Generic 80515 SFRs: Location and Reset Values (continued)

NAME	ADDRESS	RESET VALUE	DESCRIPTION
S1RELL	0x9D	0x00	Serial Port 1, Reload Register, low byte
P2	0xA0	0xFF	Port 2
IEN0	0xA8	0x00	Interrupt Enable Register 0
IP0	0xA9	0x00	Interrupt Priority Register 0
S0RELL	0xAA	0xD9	Serial Port 0, Reload Register, low byte
P3	0xB0	0xFF	Port 3
IEN1	0xB8	0x00	Interrupt Enable Register 1
IP1	0xB9	0x00	Interrupt Priority Register 1
S0RELH	0xBA	0x03	Serial Port 0, Reload Register, high byte
S1RELH	0xBB	0x03	Serial Port 1, Reload Register, high byte
PDATA	0xBF	0x00	High address byte for MOVX@Ri - also called *USR2*
IRCON	0xC0	0x00	Interrupt Request Control Register
T2CON	0xC8	0x00	Polarity for INT2 and INT3
PSW	0xD0	0x00	Program Status Word
WDCON	0xD8	0x00	Baud Rate Control Register (only WDCON[7] bit used)
A	0xE0	0x00	Accumulator
B	0xF0	0x00	B Register

Table 8. Timers/Counters Mode Description

M1	M0	MODE	FUNCTION
0	0	Mode 0	13-bit Counter/Timer mode with 5 lower bits in the TL0 or TL1 register and the remaining 8 bits in the TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are held at zero.
0	1	Mode 1	16-bit Counter/Timer mode.
1	0	Mode 2	8-bit auto-reload Counter/Timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	Mode 3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8-bit Timer/Counters.

Four operating modes can be selected for Timer 0 and Timer 1. The TMOD register is used to select the appropriate mode. The timer/counter operation is controlled by the TCON register. Bits TR1 and TR0 in the TCON register start their associated timers when set.

Interrupts

The 80515 provides 11 interrupt sources with four priority levels. Each source has its own interrupt request flag(s) located in a special function register (TCON, IRCON, and SCON). Each interrupt requested by the corresponding interrupt flag can be individually enabled or disabled by the interrupt enable bits in the IEN0, IEN1, and IEN2.

Referring to Figure 12, interrupt sources can originate from within the 80515 MPU core (referred to as Internal Sources) or can originate from other parts of the 71M654xT SoC (referred to as External Sources). There are seven external interrupt sources, (EX0-EX6).

Interrupt Overview

When an interrupt occurs, the MPU vectors to the predetermined address. Once the interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from interrupt instruction (RETI). When a RETI instruction is executed,

the processor returns to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor also indicates this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, and then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt is acknowledged by hardware forcing an LCALL to the appropriate vector address, if the following conditions are met:

- No interrupt of equal or higher priority is already in progress.
- An instruction is currently being executed and is not completed.
- The instruction in progress is not RETI or any write access to the registers IEN0, IEN1, IEN2, IP0 or IP1.

The following SFR registers control the interrupt functions:

- The interrupt enable registers: IEN0, IEN1 and IEN2.
- The Timer/Counter control registers, TCON and T2CON.
- The interrupt request register, IRCON.
- The interrupt priority registers: IP0 and IP1.

External MPU Interrupts

The seven external interrupts are the interrupts external to the 80515 core, i.e., signals that originate in other parts of the 71M654xT, for example the CE, DIO, RTC, or EEPROM interface.

The polarity of interrupts 2 and 3 is programmable in the MPU via the I3FR and I2FR bits in T2CON (SFR 0xC8). Interrupts 2 and 3 should be programmed for falling sensitivity (I3FR = I2FR = 0). The generic 8051 MPU literature states that interrupts 4 through 6 are defined as rising-edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 9.

External interrupt 0 and 1 can be mapped to pins on the device using DIO resource maps.

On-Chip Resources

Flash Memory

The device includes 128KB (71M6543GT/GHT) or 64KB (71M6543FT/HT) of on-chip flash memory. The flash memory primarily contains MPU and CE program code. It also contains images of the CE RAM and I/O RAM. On power-up, before enabling the CE, the MPU copies these images to their respective locations.

Flash space allocated for the CE program is limited to 4096 16-bit words (8KB). The CE program must begin on a 1KB boundary of the flash address space. The CE_LCTN[6:0] (71M6543GT/GHT) or CE_LCTN[5:0] (71M6543FT/HT) field defines where in flash the CE code resides. The address of the CE program is 0bXXXX XX00 0000 0000, where XXXX XX represents one of the 64 1KB pages at which the CE program begins.

Flash memory can be accessed by the MPU and the CE for reading, and by the SPI interface for reading or writing.

Table 9. External MPU Interrupts

EXTERNAL INTERRUPT	CONNECTION	POLARITY	FLAG RESET
0	Digital I/O (IE0)	Programmable	Automatic
1	Digital I/O (IE1)	Programmable	Automatic
2	CE_PULSE (IE_XPULSE, IE_YPULSE, IE_WPULSE, IE_VPULSE)	Rising	Manual
3	CE_BUSY (IE3)	Falling	Automatic
4	VSTAT (VSTAT[2:0] changed) (IE4)	Rising	Automatic
5	EEPROM busy (falling), SPI (rising) (IE_EEX, IE_SPI)	—	Manual
6	XFER_BUSY (falling), RTC_1SEC, RTC_1MIN, RTC_T, TC_TEMP (IE_XFER, IE_RTC1S, IE_RT1M, IE_RTCT)	Falling	Manual

The program memory of the 71M6543GT/71M6543GHT consists of a fixed lower bank area of 32 kB addressable at 0x0000 to 0x7FFF plus an upper bank area of 32 kB, addressable at 0x8000 to 0xFFFF. The upper bank area is banked using the I/O RAM FLSH_BANK register as follows. Note that when FLSH_BANK[1:0] = 00, the upper bank area is the same as the lower bank area (Table 10).

The flash memory page address register FLSH_PGADR[6:0] (SFR B7[7:1]) points to an address in the 71M6543GT/71M6543GHT program address space. This address in the 71M6543GT/71M6543GHT program address space can refer to different flash memory addresses, depending on the setting of the FLSH_BANK[1:0] bits. The CE location register (CE_LCTN[6:0]), on the other hand, points directly to an address in the flash memory and is not affected by the FLSH_BANK[1:0] bits.

When the SECURE bit (SFR B2[6]) is set to a 1, page erase of certain flash memory pages is blocked. These pages are page 0 (flash memory address range 0x00000 –0x003FF) and all pages between the start of the CE program (CE_LCTN[6:0]) and flash memory address 0x1FFFF.

While operating in SPI flash mode (SFM), SPI single-byte transactions are used to write to FLSH_BANK[1:0]. During a SPI single-byte transaction, SPI_CMD[1:0] overwrites the contents of FLSH_BANK[1:0]. This allows access to the entire 128KB flash memory while operating in SFM on the 71M6543GT/71M6543GHT.

MPU/CE RAM

The 71M6543FT/HT/GT/GHT includes 5KB of static RAM memory on-chip (XRAM) plus 256 bytes of internal RAM in the MPU core. The static RAM is used for data storage for both MPU and CE operations.

I/O RAM

The I/O RAM can be seen as a series of hardware registers that control basic hardware functions. I/O RAM address space starts at 0x2000.

The 71M6543FT/HT/GT/GHT includes 128 bytes NV RAM memory on-chip in the I/O RAM address space (addresses 0x2800 to 0x287F). This memory section is supported by the voltage applied at V_{BAT_RTC} and the data in it are preserved in BRN, LCD, and SLP modes as long as the voltage at V_{BAT_RTC} is within specification.

Crystal Oscillator

The oscillator drives a standard 32.768kHz tuning-fork crystal. This type of crystal is accurate and does not require a high-current oscillator circuit. The oscillator power dissipation is very low to maximize the lifetime of the V_{BAT_RTC} battery.

Oscillator calibration can improve the accuracy of both the RTC and metering.

PLL

Timing for the device is derived from the 32,768Hz crystal oscillator. The oscillator output is routed to a phase-locked loop (PLL). The PLL multiplies the crystal frequency by 600 to produce a stable 19.6608MHz clock frequency. This is the master clock (MCK), and all on-chip timing, except for the RTC clock, is derived from MCK.

The master clock can operate at either 19.66MHz or 6.29MHz depending on the PLL_FAST bit. The MPU clock frequency CKMPU is determined by another divider controlled by the I/O RAM control field MPU_DIV[2:0] and can be set to MCK x $2^{-(MPU\_DIV+2)}$, where MPU_DIV[2:0] may vary from 0 to 4. The 71M654xT $V_{V3P3SYS}$ supply current is reduced by reducing the MPU clock frequency. When the ICE_E pin is high, the circuit also generates the 9.83MHz clock for use by the emulator.

The two general-purpose counter/timers contained in the MPU are clocked by CKMPU.

The PLL is only turned off in SLP mode.

When the part is waking up from SLP or LCD modes, the PLL is turned on in 6.29MHz mode, and the PLL frequency is not be accurate until the PLL_OK flag becomes active. Due to potential overshoot, the MPU should not change the value of PLL_FAST until PLL_OK is true.

Table 10. External MPU Interrupts

FLSH_BANK[1:0]	ADDRESS RANGE FOR LOWER BANK (0x0000–0x7FFF)	ADDRESS RANGE FOR UPPER BANK (0x8000–0x7FFF)
00	0x0000–0x7FFF	0x0000–0x7FFF
01	0x0000–0x7FFF	0x8000–0x7FFF
10	0x0000–0x7FFF	0x10000–0x17FFFF
11	0x0000–0x7FFF	0x18000–0x1FFFF

Real-Time Clock (RTC)

The real-time clock is driven directly by the crystal oscillator and is powered by either the $V_{V3P3SYS}$ pin or the V_{BAT_RTC} pin, depending on the V3OK internal bit. The RTC consists of a counter chain and a set of output registers. The counter chain consists of registers for seconds, minutes, hours, day of week, day of month, month, and year. The chain registers are supported by a shadow register that facilitates read and write operations.

RTC Trimming

The RTC accuracy can be trimmed by means of a digital trimming mechanism that affects only the RTC. Either or both of these adjustment mechanisms can be used to trim the RTC.

The 71M6543FT/HT/GT/GHT can also be configured to regularly measure die temperature, including in SLP and LCD modes and while the MPU is halted. If enabled, the temperature information is automatically used to correct for the temperature variation of the crystal. A quadratic equation is used to compute the temperature correction factors.

The temperature is passed both to the quadratic calculation block and to a range check block. If the temperature exceeds the limits established in the SMIN, SMAX and SFILT registers when a range checking is enabled, a WAKE or an INTERRUPT event is posted.

The quadratic calculation block computes the position on the inverse parabolic curve that is characteristic for tuning fork crystals based on the known α and T_0 values for the crystal (these are published by the crystal manufacturer and are relatively consistent for a particular crystal type). Finally, the absolute frequency error is added or subtracted from the computed value, and the final result is used to compensate the frequency of the crystal.

RTC Interrupts

The RTC generates interrupts each second and each minute. These interrupts are called RTC_1SEC and RTC_1MIN. In addition, the RTC functions as an alarm clock by generating an interrupt when the minutes and hours registers both equal their respective target counts as defined in the alarm registers. The alarm clock interrupt is called RTC_T. All three interrupts appear in the MPU's external interrupt 6.

Temperature Sensor

The 71M654xT includes an on-chip temperature sensor for determining the temperature of its bandgap reference. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system for the compensation of current, voltage and energy measurement and the RTC. See the *Metrology Temperature Compensation*.

The 71M654xT uses a dual-slope temperature measurement technique that is operational in SLP and LCD mode, as well as BRN and MSN modes. This means that the temperature sensor can be used to compensate for the frequency variation of the crystal, even in SLP mode while the MPU is halted.

In MSN and BRN modes, the temperature sensor is awakened on command from the MPU by setting the TEMP_START control bit. The MPU must wait for the TEMP_START bit to clear before reading STEMP[15:0] and before setting the TEMP_START bit once again. In SLP and LCD modes, it is awakened at a regular rate set by TEMP_PER[2:0].

The result of the temperature measurement can be read from STEMP[15:0]. Typically, only eleven bits are significant, the remaining high-order bits reflecting the sign of the temperature relative to 0C.

Battery Monitor

The 71M654xT temperature measurement circuit can also monitor the batteries at the V_{BAT} and V_{BAT_RTC} pins. The battery to be tested (i.e., V_{BAT} or V_{BAT_RTC} pin) is selected by TEMP_BSEL.

When TEMP_BAT is set, a battery measurement is performed as part of each temperature measurement. The value of the battery reading is stored in register BSENSE[7:0]. The battery voltage can be calculated by using the formula in the BATTERY MONITOR section of the electrical characteristics table.

In MSN mode, a 100µA de-passivation load can be applied to the selected battery (i.e., selected by the TEMP_BSEL bit) by setting the BCURR bit. Battery impedance can be measured by taking a battery measurement with and without BCURR. Regardless of the BCURR bit setting, the battery load is never applied in BRN, LCD, and SLP modes.

Digital I/O and LCD Segment Drivers

The 71M6543FT/HT/GT/GHT combines most DIO pins with LCD segment drivers. Each SEG/DIO pin can be configured as a DIO pin or as a segment (SEG) driver pin.

On reset or power-up, all DIO pins are DIO inputs until they are configured as desired under MPU control. The pin function can be configured by the I/O RAM registers LCD_MAPn. Setting the bit corresponding to the pin in LCD_MAPn to 1 configures the pin for LCD, setting LCD_MAPn to 0 configures it for DIO.

Once a pin is configured as DIO, it can be configured independently as an input or output. The PB pin is a dedicated digital input and is not part of the SEGDIO system.

Some pins (SEGDIO2 through SEGDIO11 and PB) can be routed to internal logic such as the interrupt controller or a timer channel. This routing is independent of the direction of the pin, so that outputs can be configured to cause an interrupt or start a timer.

A total of 32 combined SEG/DIO pins plus 5 SEG outputs are available for the 71M6543FT/HT/GT/GHT. These pins can be categorized as follows:

17 combined SEG/DIO segment pins:

- SEGDIO4…SEGDIO5 (2 pins)
- SEGDIO9…SEGDIO14 (6 pins)
- SEGDIO19…SEGDIO25 (7 pins)
- SEGDIO44…SEGDIO45 (2 pins)

15 combined SEG/DIO segment pins shared with other functions:

- SEGDIO0/WPULSE, SEGDIO1/VPULSE (2 pins)
- SEGDIO2/SDCK, SEGDIO3/SDATA (2 pins)
- SEGDIO6/XPULSE, SEGDIO7/YPULSE (2 pins)
- SEGDIO8/DI (1 pin)
- SEGDIO26/COM5, SEGDIO27/COM4 (2 pins)
- SEGDIO36/SPI_CSZ…SEGDIO39/SPI_CKI (4 pins)
- SEGDIO51/OPT_TX, SEGDIO55/OPT_RX (2 pins)

5 dedicated SEG segment pins are available:

- ICE Inteface pins: SEG48/E_RXTX, SEG49/E_TCLK, SEG50/E_RST (3 pins)
- Test Port pins: SEG46/TMUX2OUT, SEG47/TMUXOUT (2 pins)

There are four dedicated common segment outputs (COM0…COM3) plus the two additional shared common segment outputs that are listed under combined SEG/DIO shared pins (SEGDIO26/COM5, SEGDIO27/COM4).

Thus, in a configuration where none of these pins are used as DIOs, there can be up to 37 LCD segment pins with 4 commons, or 35 LCD segment pins with 6 commons. And in a configuration where LCD segment pins are not used, there can be up to 32 DIO pins.

LCD Drivers

The LCD drivers are grouped into up to six commons (COM0 – COM5) and up to 56 segment drivers. The LCD interface is flexible and can drive 7-segment digits, 14-segments digits or annunciator symbols.

LCD voltage can be taken from the V_{LCD} pin or the $V_{V3P3SYS}$ pin. A contrast DAC regulates V_{LCD} from either V_{BAT} or $V_{V3P3SYS}$.

The LCD system has the ability to drive up to six segments per SEG driver. If the display is configured with six back planes, the 6-way multiplexing minimizes the number of SEG pins required to drive a display. This maximizes the number of DIO pins available to the application. If 5-state multiplexing is selected, SEGDIO27 is converted to COM4. If 6-state multiplexing is selected, SEGDIO26 is converted to COM5.

The LCD_ON and LCD_BLANK bits are an easy way to either blank the LCD display or to turn all segments on. Neither bit affects the contents of the LCD data stored in the LCDSEG_DIO[ ] registers. In comparison, LCD_RST (I/O RAM 0x240C[2]) clears all LCD data to zero. LCD_RST affects only pins that are configured as LCD.

The LCD can be driven in static, ½ bias, and ⅓ bias modes. Note that COM pins that are not required in a specific mode maintain a ‘segment off’ state rather than GND, VCC, or high impedance.

The segment drivers SEGDIO22 and SEGDIO23 can be configured to blink at either 0.5 Hz or 1 Hz. The blink rate is controlled by LCD_Y. There can be up to six segments connected to each of these driver pins. The I/O RAM fields LCD_BLKMAP22[5:0] and LCD_BLKMAP23[5:0] identify which pixels, if any, are to blink. LCD_BLKMAP22[5:0] and LCD_BLKMAP23[5:0] are nonvolatile.

The LCD bias may be compensated for temperature using the LCD_DAC[4:0] field. The bias may be adjusted from 1.4 V below the 3.3 V supply ($V_{V3P3SYS}$ in MSN mode and V_{BAT} in BRN and LCD modes). When the LCD_DAC[4:0] field is set to 000, the DAC is bypassed and powered down. This can be used to reduce current in LCD mode.

The 71M6543FT/HT/GT/GHT has 56 LCD driver pins available, and can drive up to 336 segments.

Square Wave Output

The 71M654xT includes a square wave generator that can be configured to present a square wave on the SEGDIO15 pin. This square wave can be used as a clock to drive other devices and peripherals.

The output is enabled by setting the OUT_SQE bit. The output frequency can then be selected by setting the OUT_SQ[1:0] bits.

EEPROM Interface

The 71M654xT provides hardware support for both two-pin (I^2C) and three-wire (MICROWIRE) EEPROMs.

Two-Pin EEPROM Interface

The two-pin serial interface is multiplexed onto the SEGDIO2 (SDCK) and SEGDIO3 (SDATA) pins. Configure the interface for two-pin mode by setting DIO_EEX[1:0] = 01. The MPU communicates with the interface through the SFR registers EEDATA and EECTRL. To write a byte of data to the EEPROM the MPU places the data in EEDATA and then writes the Transmit code to EECTRL. This initiates the transmit operation which is finished when the BUSY bit falls. INT5 is also asserted when BUSY falls. The MPU can then check the RX_ACK bit to see if the EEPROM acknowledged the transmission.

A byte is read by writing the Receive command to EECTRL and waiting for the BUSY bit to fall. Upon completion, the received data is in EEDATA. The serial transmit and receive clock is 78kHz during each transmission, and then holds in a high state until the next transmission.

The two-pin interface handles protocol details. The MPU can command the interface to issue a start, a repeated start and a stop condition, and it can manage the transmitted ACK status as well.

Three-Wire EEPROM Interface

The three-wire interface supports standard MICROWIRE (single data pin with clock and select pins) or a subset of SPI (separate DI and DO pins with clock and select pins). MICROWIRE is selected by setting DIO_EEX[1:0] = 10. In this mode, EECTRL selects whether the interface is sending or receiving, and eight bits of data are transferred in each transaction. In this configuration, SEGDIO2 is configured for clock, and SEGDIO3 is configured for data.

When separate DI/DO pins are selected (DIO_EEX[1:0] = 11) the interface operates as a subset of SPI. Only SPI modes 0 or 3 are supported. In this configuration, SEGDIO3 is DO and SEGDIO8 is DI.

UART

The 71M6543FT/HT/GT/GHT include a UART (UART0) that can be programmed to communicate with a variety of AMR modules and other external devices. A second UART (UART1) is connected to the optical port.

The 80515 only supports two UARTs, but meters occasionally need three. The 71M654xT tries to help in two ways.

First, as shown in Figure 7, the 71M654xT can be configured to switch the optical UART to DIOs 5 and 17 by setting UMUX_SEL (I/O RAM 0x2456[4]) to 1. This is useful when a conventional UART can appear by command at different pins. The DIOs must not be configured as LCD outputs.

Also, as shown in Figure 7, the 71M654xT can also be configured to drive the opti7al UART with DIO signal in a bit banged configuration. When control bit OPT_BB (I/O RAM 0x2022[0]) is set, the optical port is driven by DIO5 and the SEGDIO5 pin is driven by UART1_TX. This configuration is typically used when the two dedicated UARTs must be connected to high speed clients and a slower optical UART is permissible.

SPI Slave Port

The SPI slave port communicates directly with the MPU data bus and is able to read and write Data RAM and I/O RAM locations. It is also able to send commands to the MPU. The interface to the slave port consists of the SPI_CSZ, SPI_CKI, SPI_DI and SPI_DO pins. These pins are multiplexed with the combined DIO/LCD segment driver pins SEGDIO36 to SEGDIO39.

Additionally, the SPI interface allows flash memory to be read and to be programmed. To facilitate flash programming, cycling power or asserting RESET causes the SPI port pins to default to SPI mode. The SPI port is disabled by clearing the SPI_E bit.

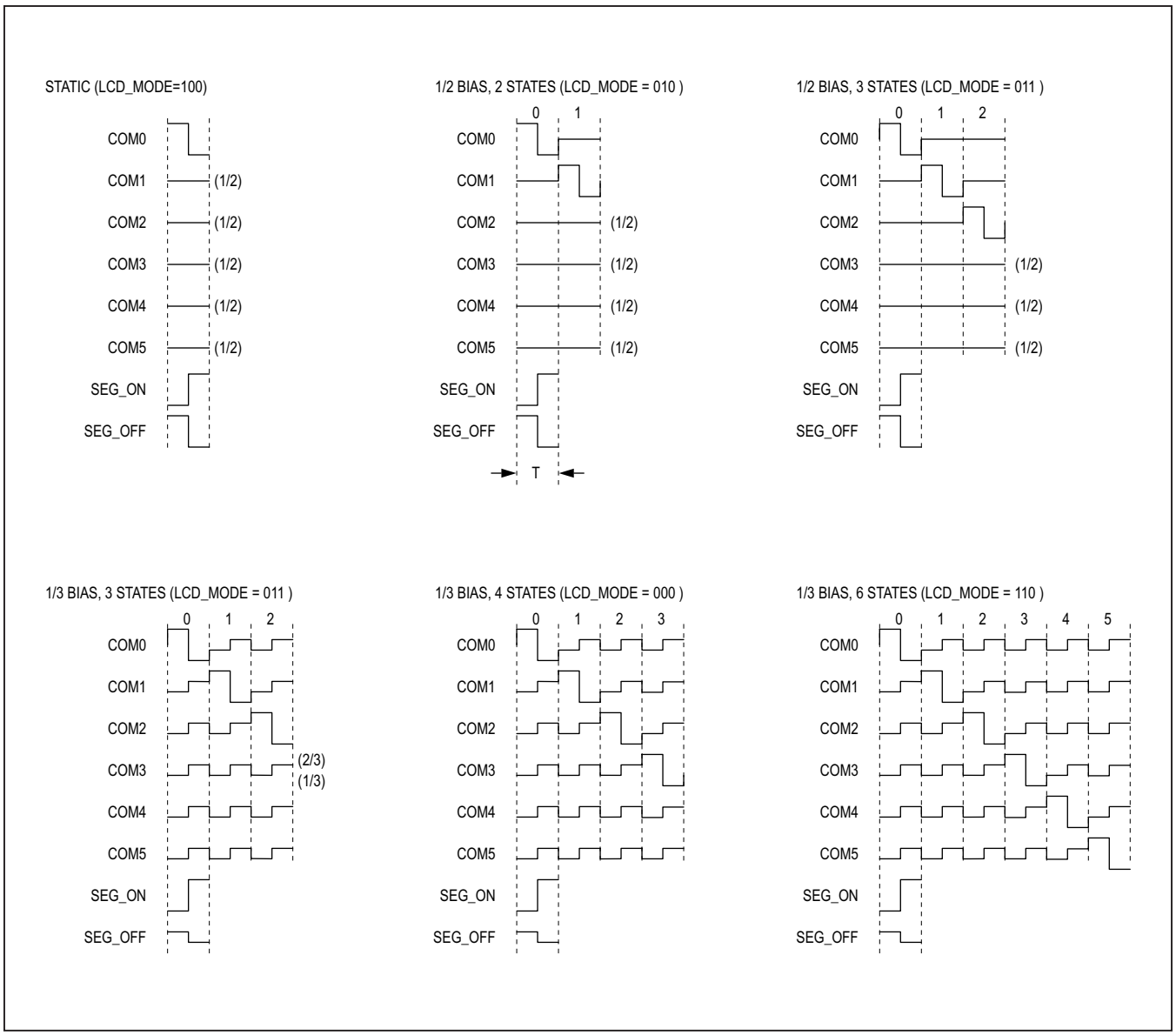


Figure 6. Typical LCD Waveforms

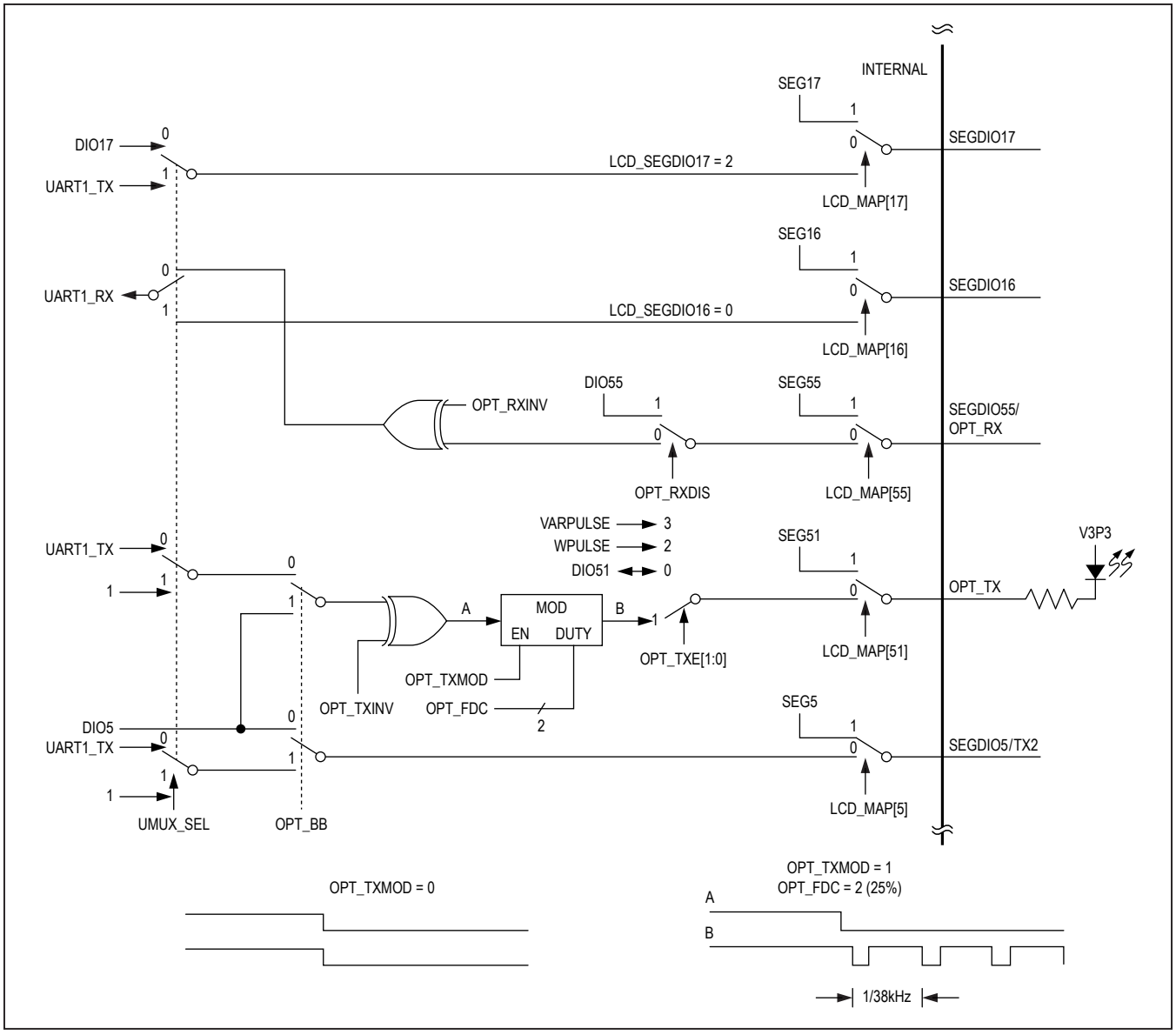


Figure 7. Optical Interface (UART1)

Possible applications for the SPI interface are:

- An external host reads data from CE locations to obtain metering information. This can be used in applications where the 71M654xT function as a smart front-end with preprocessing capability. Since the addresses are in 16-bit format, any type of XRAM data can be accessed: CE, MPU, I/O RAM, but not SFRs or the 80515-internal register bank.
- A communication link can be established via the SPI interface: By writing into MPU memory locations, the external host can initiate and control processes in the 71M654xT MPU. Writing to a CE or MPU location normally generates an interrupt, a function that can be used to signal to the MPU that the byte that had just been written by the external host must be read and processed. Data can also be inserted by the external host without generating an interrupt.
- An external DSP can access front-end data generated by the ADC. This mode of operation uses the 71M654xT as an analog front-end (AFE).
- Flash programming by the external host (SPI Flash Mode).

SPI Safe Mode

Sometimes it is desirable to prevent the SPI interface from writing to arbitrary RAM locations and thus disturbing MPU and CE operation. This is especially true in AFE applications. For this reason, the SPI SAFE mode was created. In SPI SAFE mode, SPI write operations are disabled except for a 16 byte transfer region at address 0x400 to 0x40F. If the SPI host needs to write to other addresses, it must use the SPI_CMD register to request the write operation from the MPU. SPI SAFE mode is enabled by the SPI_SAFE bit.

SPI Flash Mode (SFM)

In normal operation, the SPI slave interface cannot read or write the flash memory. However, the 71M6543FT/HT/GT/GHT supports a SPI flash mode (SFM) which facilitates initial programming of the flash memory. When in SFM mode, the SPI can erase, read, and write the flash memory. Other memory elements such as XRAM and I/O RAM are not accessible in this mode. In order to protect the flash contents, several operations are required before the SFM mode is successfully invoked.

In SFM mode, n byte reads and dual-byte writes to flash memory are supported. Since the flash write operation is always based on a two-byte word, the initial address must always be even. Data is written to the 16-bit flash memory bus after the odd word is written.

While operating in SPI flash mode (SFM), SPI single-byte transacations are used to wrtie FLSH_BANK[1:0]. During an SPI single-byte transaction, SPI_CMD[1:0] overwrites the contents of FLSH_BANK[1:0]. This allows access to the entire 128KB flash memory while operating in SFM on the 71M6543GT/GHT.

In SFM mode, the MPU is completely halted. The 71M6543FT/HT/GT/GHT must be reset by the WD timer or by the RESET pin in order to exit SFM mode.

If the SPI port is used for code updates (in lieu of a programmer that uses the ICE port), then a code that disables the flash access through SPI can potentially lock out flash program updates.

Hardware Watchdog Timer

An independent, robust, fixed-duration, watchdog timer (WDT) is included in the 71M6543FT/HT/GT/GHT. It uses the RTC crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time, the WDT overflows and the part is reset as if the RESET pin were pulled high, except that the I/O RAM bits are in the same state as after a wake-up from SLP or LCD modes. After 4100 CK32 cycles (or 125 ms) following the WDT overflow, the MPU is launched from program address 0x0000.

The watchdog timer is also reset when the internal signal WAKE = 0.

Test Ports

Two independent multiplexers allow the selection of internal analog and digital signals for the TMUXOUT and TMUX2OUT pins. These pins are multiplexed with the SEG47 and SEG46 function. In order to function as test pins, LCD_MAP[46] and LCD_MAP[47] must be 0.

The TMUXOUT and TMUX2OUT pins may be used for diagnostics purposes during the product development cycle or in the production test. The RTC 1-second output may be used to calibrate the crystal oscillator. The RTC 4-second output provides higher precision for RTC calibration. RTCLK may also be used to calibrate the RTC.

Functional Description

Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t)I(t)dt$$

Assuming phase angles are constant, the following formulae apply:

- P = Real Energy [Wh] = V x A x cos (φ) x t
- Q = Reactive Energy [VARh] = V x A x sin (φ) x t
- S = Apparent Energy [VAh] = $\sqrt{P^2 + Q^2}$

For a practical meter, not only voltage and current amplitudes, but also phase angles and harmonic content may change constantly. Thus, simple RMS measurements are inherently inaccurate. The 71M654xT, however, functions by emulating the integral operation above by processing current and voltage samples at a constant rate. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied by the sample period yield an accurate value for the instantaneous energy. Summing the instantaneous energy quantities over time provides accurate results for accumulated energy.

The application of 240V AC and 100A results in an accumulation of 480Ws (= 0.133 Wh) over the 20ms period, as indicated by the accumulated power curve. The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

Battery Modes

The 71M654xT can operate in one of four power modes: mission (MSN), brownout (BRN), sleep (SLP), or LCD-only (LCD) mode.

Shortly after system power ($V_{V3P3SYS}$) is applied, the part is in mission mode. MSN mode means that the part is operating with system power and that the internal PLL is stable. This mode is the normal operating mode where the part is capable of measuring energy.

When system power is not available, the 71M654xT is in one of three battery modes: BRN, SLP or LCD.

An internal comparator monitors the voltage at the V_{V3P3A} pin (note that $V_{V3P3SYS}$ and V_{V3P3A} are typically connected together at the PCB level). When the V_{V3P3A} dc voltage drops below 2.8 VDC, the comparator resets an internal power status bit called V3OK. As soon as system power is removed and V3OK = 0, the 71M654xT switches to battery power (V_{BAT} pin), notifies the MPU by issuing an interrupt and updates the VSTAT[2:0] register. The MPU continues to execute code when the system transitions from MSN to BRN mode. Depending on the MPU code, the MPU can choose to stay in BRN mode, or transition to LCD or to SLP mode. BRN mode is similar to MSN mode except that resources powered by

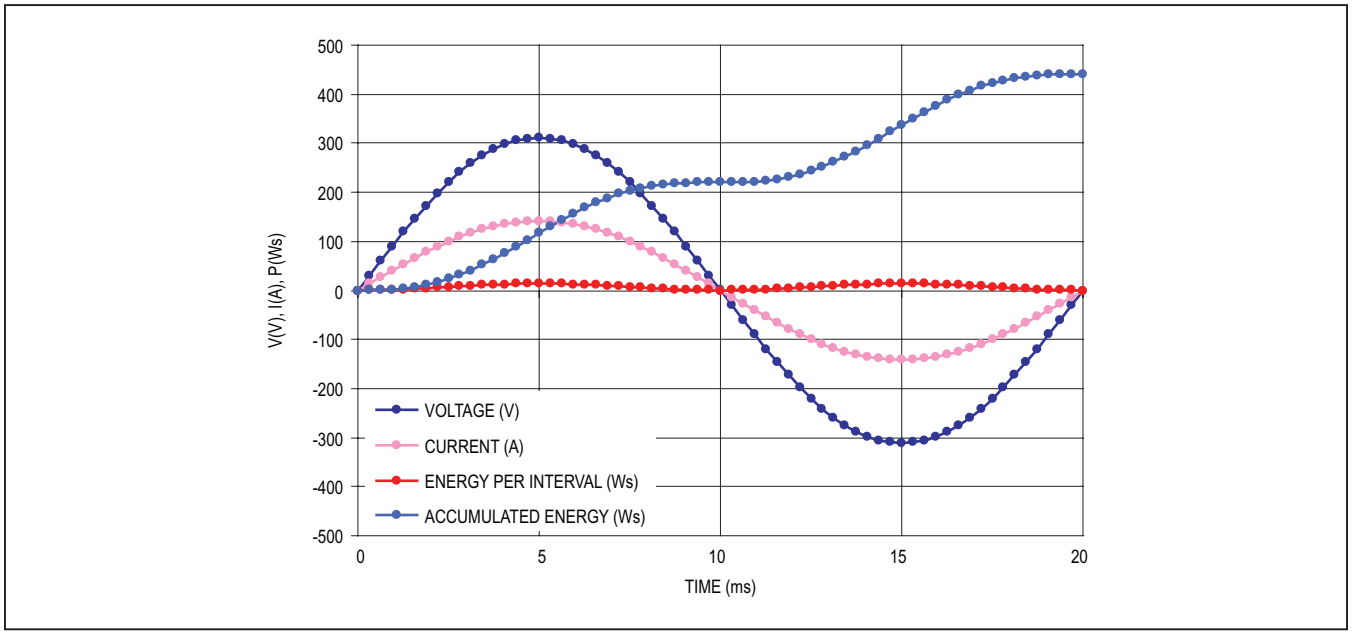


Figure 8. Waveforms Comparing Voltage, Current, Energy per Interval, and Accumulated Energy

V_{V3P3A} power, such as the ADC are inaccurate. In BRN mode the CE continues to run and should be turned off to conserve V_{BAT} power. Also, the PLL continues to function at the same frequency as in MSN mode and its frequency should be reduced to save power.

When system power is restored, the 71M654xT automatically transitions from any of the battery modes (BRN, LCD, SLP) back to MSN mode, switches back to using system power ($V_{V3P3SYS}$, V_{V3P3A}), issues an interrupt and updates VSTAT[1:0]. The MPU software should restore MSN mode operation by issuing a soft reset to restore system settings to values appropriate for MSN mode.

Transitions from both LCD and SLP mode to BRN mode can be initiated by the following events:

1) Wake-up timer timeout.
2) Pushbutton (PB) is activated.
3) A rising edge on SEGDIO4, SEGDIO52, or SEGDIO55.
4) Activity on the RX or OPT_RX pins.

Brownout Mode

In BRN mode, most nonmetering digital functions are active including ICE, UART, EEPROM, LCD and RTC. In BRN mode, the PLL continues to function at the same frequency as MSN mode. It is up to the MPU to reduce the PLL frequency or the MPU frequency in order to minimize power consumption.

From BRN mode, the MPU can choose to enter LCD or SLP modes. When system power is restored while the 71M654xT is in BRN mode, the part automatically transitions to MSN mode.

LCD Only Mode

LCD mode may be commanded by the MPU at any time by setting the LCD_ONLY control bit. However, it is recommended that the LCD_ONLY control bit be set by the MPU only after the 71M654xT has entered BRN mode. For example, if the 71M654xT is in MSN mode when LCD_ONLY is set, the duration of LCD mode is very brief and the 71M654xT immediately wakes.

In LCD mode, V_{V3P3D} is disabled, thus removing all current leakage from the V_{BAT} pin. Before asserting LCD_ONLY mode, it is recommended that the MPU minimize PLL current by reducing the output frequency of the PLL to 6.2MHz (i.e., write PLL_FAST = 0).

In LCD mode, the data contained in the LCD_SEG registers is displayed using the segment driver pins. Up to two LCD segments connected to the pins SEGDIO22 and SEGDIO23 can be made to blink without the involvement of the MPU, which is disabled in LCD mode. To minimize battery power consumption, only segments that are used should be enabled.

After the transition from LCD mode to MSN or BRN mode, the PC (Program Counter) is at 0x0000, the XRAM is in an undefined state, and configuration I/O RAM bits are reset (see Table 11 for I/O RAM state upon wake). The data stored in nonvolatile I/O RAM locations is preserved in LCD mode (the shaded locations in Table 10 are nonvolatile).

Sleep Mode

When the $V_{V3P3SYS}$ pin voltage drops below 2.8 VDC, the 71M654xT enters BRN mode and the V_{V3P3D} pin obtains power from the V_{BAT} pin instead of the $V_{V3P3SYS}$ pin. Once in BRN mode, the MPU may invoke SLP mode by setting the SLEEP bit. The purpose of SLP mode is to consume the least amount power while still maintaining the real time clock, temperature compensation of the RTC, and the nonvolatile portions of the I/O RAM.

In SLP mode, the V_{V3P3D} pin is disconnected, removing all sources of current leakage from the V_{BAT} pin. The nonvolatile I/O RAM locations and the SLP mode functions, such as the temperature sensor, oscillator, RTC, and the RTC temperature compensation are powered by the V_{BAT_RTC} pin. SLP mode can be exited only by a system power-up event or one of the wake methods.

If the SLEEP bit is asserted when $V_{V3P3SYS}$ pin power is present (i.e., while in MSN mode), the 71M654xT enters SLP mode, resetting the internal WAKE signal, at which point the 71M654xT begins the standard wake from sleep procedures.

When power is restored to the $V_{V3P3SYS}$ pin, the 71M654xT transitions from SLP mode to MSN mode and the MPU PC (Program Counter) is initialized to 0x0000. At this point, the XRAM is in an undefined state, but nonvolatile I/O RAM locations are preserved.

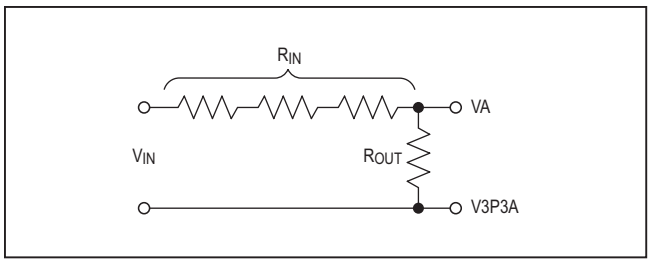


Figure 9. Typical Voltage Sense Circuit Using Resistive Divider

Applications Information

Connecting 5V Devices

All digital input pins of the 71M654xT are compatible with external 5V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5V devices.

Direct Connection of Sensors

The 71M654xT supports direct connection of current transformer and shunt-fed sensors.

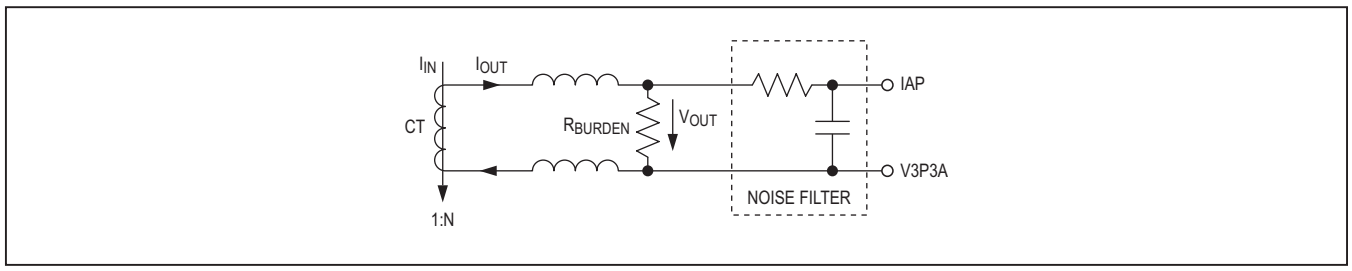


Figure 10. Typical Current-Sense Circuit Using Current Transformer in a Single-Ended Configuration

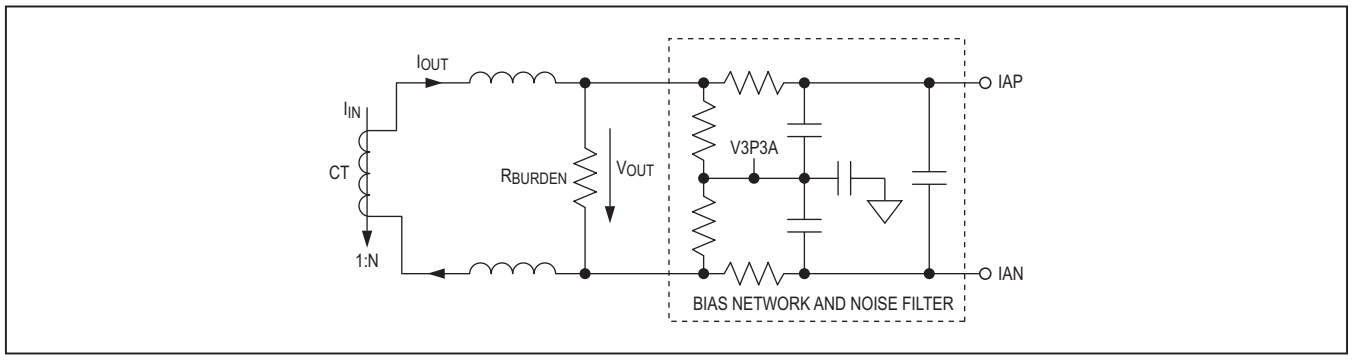


Figure 11. Typical Current-Sense Circuit Using Current Transformer in a Differential Configuration

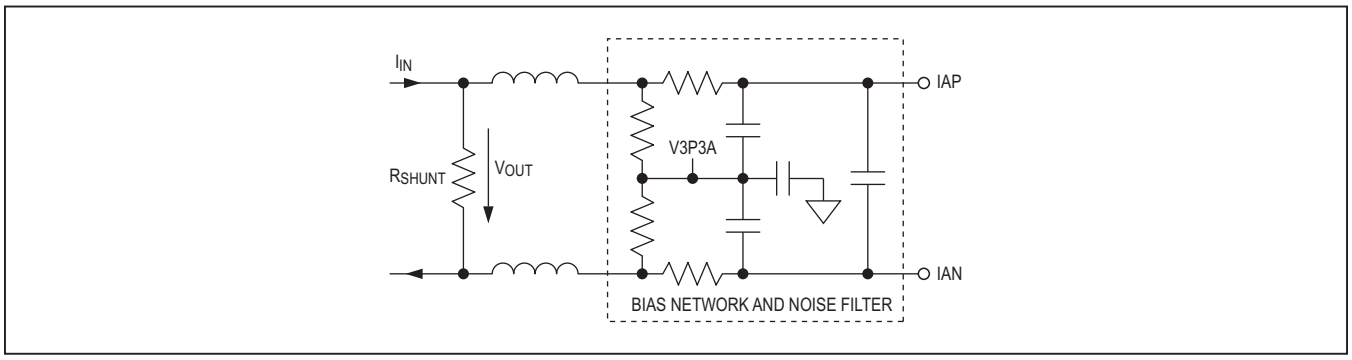


Figure 12. Typical Current-Sense Circuit Using Shunt in a Differential Configuration

Using the 71M6543FT/HT/GT/GHT with Local Sensors

The 71M6543FT/HT/GT/GHT can be configured to operate with locally connected current sensors. All current inputs are connected to a current transformer (CT) and are therefore isolated. This configuration implements a polyphase measurement with tamper-detection using one current sensor to measure the neutral current. For best performance, all current sensor inputs are configured for differential mode.

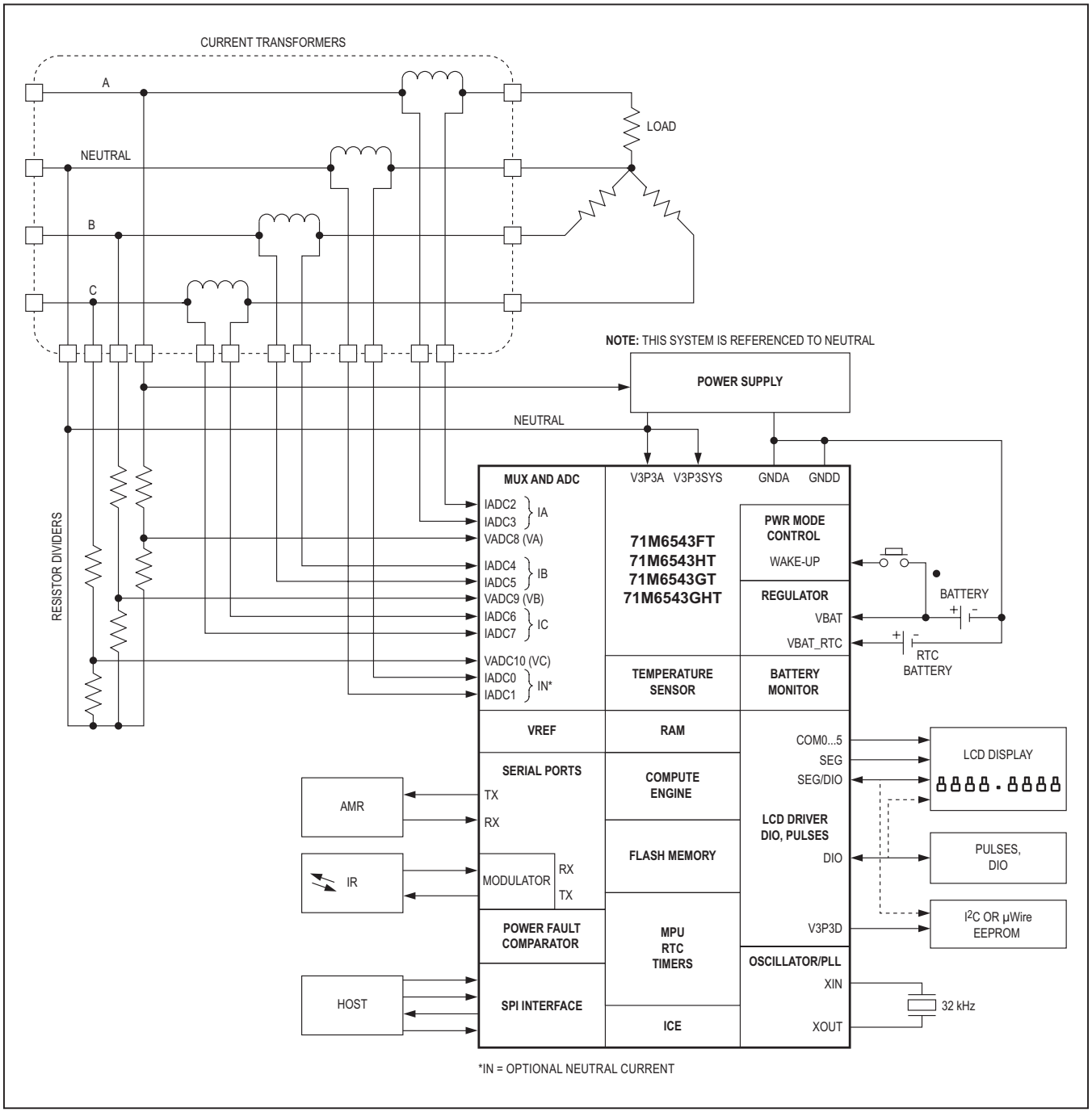


Figure 13. 71M6543FT/HT/GT/GHT Typical Operating Circuit Using Locally Connected Sensors

Using the 71M6543FT/HT/GT/GHT with Remote Sensors

The 71M6543FT/HT/GT/GHT can be configured to operate with 71M6x03 remote sensor interfaces and current shunts. This configuration implements a polyphase measurement with tamper-detection. For best performance, the IADC0-IADC1 current sensor input is configured for differential mode (DIFFA_E = 1). The outputs of the 71M6x03 isolated sensor interface are routed through a pulse transformer, which is connected to the current input pins (IADC2-IADC7). The current input pins (IADC2-IADC7) must be configured for remote sensor communication (i.e., RMT_E =1).

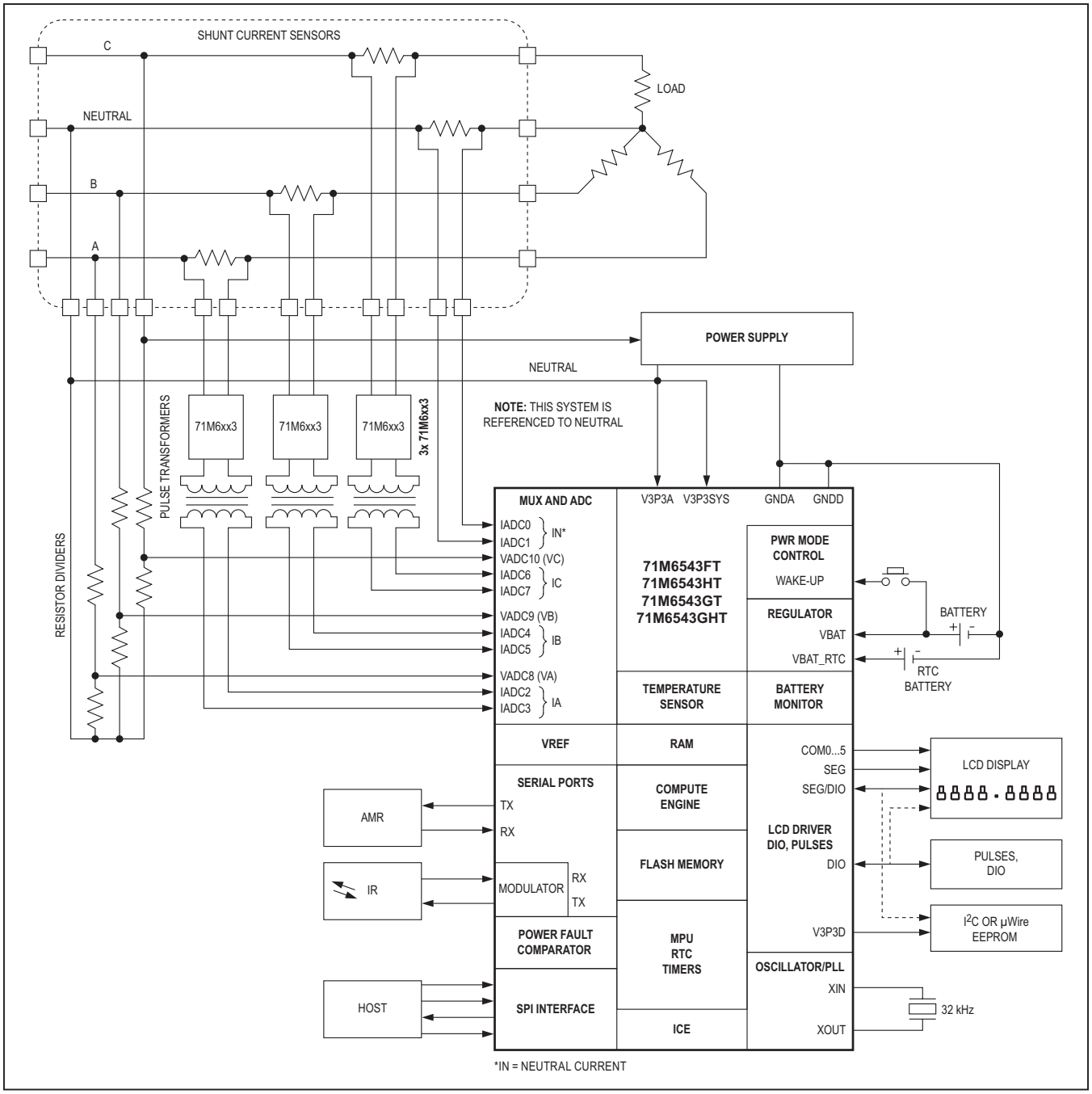


Figure 14. 71M6543FT/HT/GT/GHT Typical Operating Circuit Using Remote Neutral Current Sensor

Metrology Temperature Compensation

Since the V_{REF} bandgap amplifier is chopper-stabilized the DC offset voltage (the most significant long-term drift mechanism in bandgap voltage references) is automatically removed by the chopper circuit. Both the 71M654xT and the 71M6x03 feature chopper circuits for their respective V_{REF} voltage reference. V_{REF} is trimmed to a target value of 1.195V during the device manufacturing process and the result of the trim stored in nonvolatile fuses.

For the 71M654xT device (Q0.5% energy accuracy), the TRIMT[7:0] value can be read by the MPU during initialization in order to calculate parabolic temperature compensation coefficients suitable for each individual 71M654xT device. The resulting temperature coefficient for V_{REF} in the 71M654xT is ±40 ppm/°C.

By using the trim information in the TRIMT register and the sensed temperature, a gain adjustment for the sensor can be computed. See the *71M6543FT/HT/GT/GHT User's Guide* for more information about compensating sensors for temperature variations.

Connecting I²C EEPROMs

I²C EEPROMs or other I²C compatible devices should be connected to the DIO pins SEGDIO2 and SEGDIO3.

Pullup resistors of roughly 10kΩ to V_{V3P3D} (to ensure operation in BRN mode) should be used for both SDCK and SDATA signals. The DIO_EEX[1:0] field in I/O RAM must be set to 01 in order to convert the DIO pins SEGDIO2 and SEGDIO3 to I²C pins SDCK and SDATA.

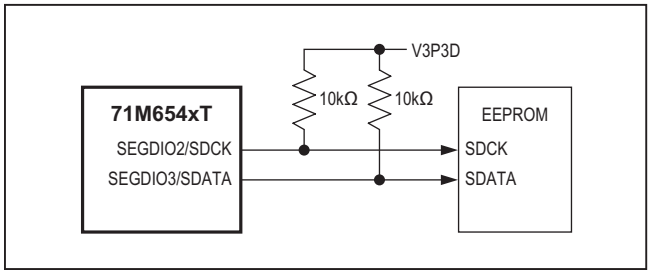


Figure 15. Typical I²C Operating Circuit

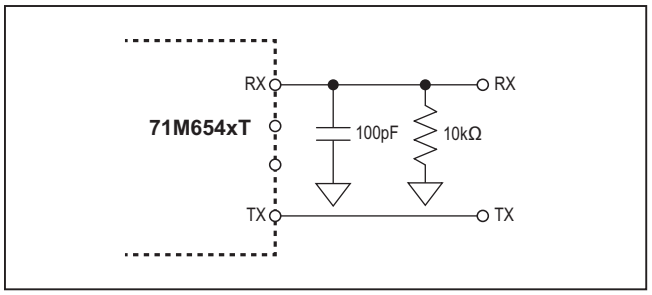


Figure 16. Typical UART Operating Circuit

Connecting Three-Wire EEPROMs

MICROWIRE EEPROMs and other compatible devices should be connected to the DIO pins SEGDIO2/SDCK and SEGDIO3/SDATA.

UART0

The UART0 RX pin should be pulled down by a 10kΩ resistor and additionally protected by a 100pF ceramic capacitor.

Optical Interface

The OPT_TX and OPT_RX pins can be used for a regular serial interface (by connecting a RS_232 transceiver for example), or they can be used to directly operate optical components (for example, an infrared diode and phototransistor implementing a FLAG interface). Figure 16 shows the basic connections for UART1. The OPT_TX pin becomes active when the I/O RAM control field OPT_TXE (I/O RAM 0x2456[3:2]) is set to 00.

The polarity of the OPT_TX and OPT_RX pins can be inverted with the configuration bits, OPT_TXINV and OPT_RXINV, respectively.

The OPT_TX output may be modulated at 38kHz when system power is present. Modulation is not available in BRN mode. The OPT_TXMOD bit enables modulation. The duty cycle is controlled by OPT_FDC[1:0], which can select 50%, 25%, 12.5%, and 6.25% duty cycle. A 6.25% duty cycle means OPT_TX is low for 6.25% of the period. The OPT_RX pin uses digital signal thresholds. It may need an analog filter when receiving modulated optical signals.

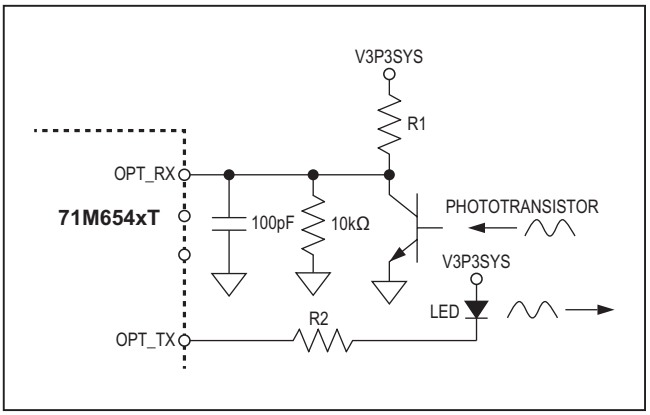


Figure 17. Optical Interface Typical Operating Circuit

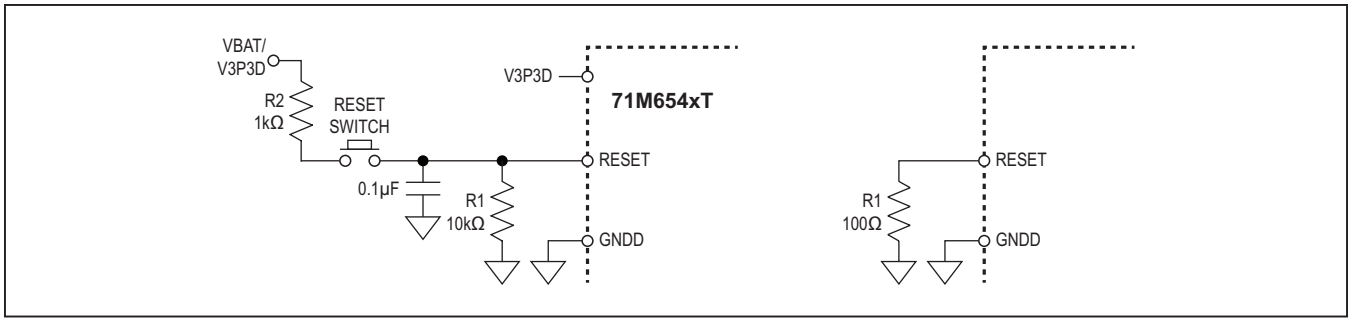


Figure 18. Typical Reset Circuits

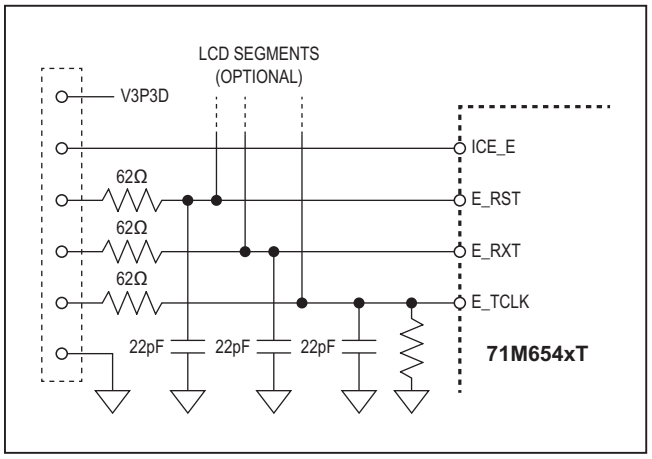


Figure 19. Typical Emulator Connections

With modulation, an optical emitter can be operated at higher current than nominal, enabling it to increase the distance along the optical path.

If operation in BRN mode is desired, the external components should be connected to V_{V3P3D}. However, it is recommended to limit the current to a few mA.

Reset

Even though a functional meter does not necessarily need a reset switch, it is useful to have a reset push-button for prototyping. The RESET signal may be sourced from $V_{V3P3SYS}$ (functional in MSN mode only), V_{V3P3D} (MSN and BRN modes), or V_{BAT} (all modes, if a battery is present), or from a combination of these sources, depending on the application. RESET causes the CPU to restart and returns all IO RAM values to their default values.

For a production meter, the RESET pin should be protected by the external components. R1 should be in the range of 100Ω and mounted as closely as possible to the IC.

Emulator Port Pins

Even when the emulator is not used, small shunt capacitors to ground (22pF) should be used for protection from EMI. Production boards should have the ICE_E pin connected to ground.

MPU Firmware Library

All application-specific MPU functions are featured in the demonstration C source code supplied by Maxim Integrated. The code is available as part of the Demonstration Kit for the 71M6543FT/GT/GHT. The Demonstration Kits come with preprogrammed with demo firmware and mounted on a functional sample meter Demo Board. The Demo Boards allow for quick and efficient evaluation of the IC without having to write firmware or having to supply an in-circuit emulator (ICE). Contact Maxim Integrated for information on price and availability of demonstration boards.

Meter Calibration

Once the 71M654xT energy meter device has been installed in a meter system, it must be calibrated. A complete calibration includes:

- Establishment of the reference temperature (typically 22°C).
- Calibration of the metrology section: calibration for tolerances of the current sensors, voltage dividers and signal conditioning components as well as of the internal reference voltage (V_{REF}) at the reference temperature.

The metrology section can be calibrated using the gain and phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by the current sensors or by the effects of reactive power supplies.

Due to the flexibility of the MPU firmware, any calibration method, such as calibration based on energy, or current and voltage can be implemented. It is also possible to implement segment-wise calibration (depending on current range).

The 71M6543FT/HT/GT/GHT support common industry standard calibration techniques, such as single-point (energy-only), multipoint (energy, V_{RMS}, I_{RMS}), and auto-calibration.

Contact Maxim Integrated to obtain a copy of the latest calibration spreadsheet file for the 71M654xT.

Firmware Interface

Overview: Functional Order

The I/O RAM locations at addresses 0x2000 to 0x20FF have sequential addresses to facilitate reading by the MPU. These I/O RAM locations are usually modified only at power-up. These addresses are an alternative sequential address to subsequent addresses (above 0x2100). For instance, EQU[2:0] can be accessed at I/O RAM 0x2000[7:5] or at I/O RAM 0x2106[7:5].

Unimplemented (U) and reserved (R) bits are shaded in light gray. Unimplemented bits are identified with a 'U'. Unimplemented bits have no memory storage, writing them has no effect, and reading them always returns zero.

Reserved bits are identified with an 'R', and must always be written with a zero. Writing values other than zero to reserved bits may have undesirable side effects and must be avoided.

Nonvolatile bits are shaded in dark gray. Nonvolatile bits are backed up during power failures if the system includes a battery connected to the V_{BAT} pin.

Table 11. I/O RAM Locations in Numerical Order

NAME	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CE6	2000	EQU[2:0]			U	CHOP_E[1:0]		RTM_E	CE_E
CE5	2001	U	U	U	SUM_SAMPS[12:8]				
CE4	2002	SUM_SAMPS[7:0]							
CE3	2003	U	CE_LCTN[6:0] for 71M6543GT/GHT, CE_LCTN[5:0] for 71M6543FT/HT						
CE2	2004	PLS_MAXWIDTH[7:0]							
CE1	2005	PLS_INTERVAL[7:0]							
CE0	2006	DIFF6_E	DIFF4_E	DIFF2_E	DIFF0_E	RFLY_DIS	FIR_LEN[1:0]		PLS_INV
RCE0	2007	CHOPR[1:0]		RMT6_E	RMT4_E	RMT2_E	R	R	R
RTMUX	2008	U	TMUXRB[2:0]			U	TMUXRA[2:0]		
Reserved	2009	U	U	R	U	U	U	U	U
MUX5	200A	MUX_DIV[3:0]				MUX10_SEL			
MUX4	200B	MUX9_SEL				MUX8_SEL			
MUX3	200C	MUX7_SEL				MUX6_SEL			
MUX2	200D	MUX5_SEL				MUX4_SEL			
MUX1	200E	MUX3_SEL				MUX2_SEL			
MUX0	200F	MUX1_SEL				MUX0_SEL			
TEMP	2010	TEMP_BSEL	TEMP_PWR	OSC_COMP	TEMP_BAT	U	TEMP_PER[2:0]		
LCD0	2011	LCD_E	LCD_MODE[2:0]			LCD_ALLCOM	LCD_Y	LCD_CLK[1:0]	
LCD1	2012	LCD_VMODE[1:0]	LCD_BLNKMAP23[5:0]						
LCD2	2013	LCD_BAT	R	LCD_BLNKMAP22[5:0]					
LCD_MAP6	2014	LCD_MAP[55:48]							
LCD_MAP5	2015	LCD_MAP[47:40]							
LCD_MAP4	2016	LCD_MAP[39:32]							
LCD_MAP3	2017	LCD_MAP[31:24]							
LCD_MAP2	2018	LCD_MAP[23:16]							
LCD_MAP1	2019	LCD_MAP[15:8]							
LCD_MAP0	201A	LCD_MAP[7:0]							
DIO_R5	201B	U	U	U	U	U	DIO_RPB[2:0]		
DIO_R4	201C	U	DIO_R11[2:0]			U	DIO_R10[2:0]		
DIO_R3	201D	U	DIO_R9[2:0]			U	DIO_R8[2:0]		
DIO_R2	201E	U	DIO_R7[2:0]			U	DIO_R6[2:0]		
DIO_R1	201F	U	DIO_R5[2:0]			U	DIO_R4[2:0]		

Table 11. I/O RAM Locations in Numerical Order (continued)

NAME	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIO_R0	2020	U	DIO_R3[2:0]			U	DIO_R2[2:0]		
DIO0	2021	DIO_EEX[1:0]		U	U	OPT_TXE[1:0]		OPT_TXMOD	OPT_TXINV
DIO1	2022	DIO_PW	DIO_PV	OPT_FDC[1:0]		U	OPT_RXDIS	OPT_RXINV	OPT_BB
DIO2	2023	DIO_PX	DIO_PY	U	U	U	U	U	U
INT1_E	2024	EX_EEX	EX_XPULSE	EX_YPULSE	EX_RTCT	EX_TCTEMP	EX_RTC1M	EX_RTC1S	EX_XFER
INT2_E	2025	EX_SPI	EX_WPULSE	EX_VPULSE					
WAKE_E	2026	U	EW_TEMP	U	EW_RX	EW_PB	EW_DIO4	EW_DIO52†	EW_DIO55
SFMM	2080	SFMM[7:0] (via SPI slave port only)							
SFMS	2081	SFMS[7:0] (via SPI slave port only)							
CE AND ADC									
MUX5	2100	MUX_DIV[3:0]				MUX10_SEL[3:0]			
MUX4	2101	MUX9_SEL[3:0]				MUX8_SEL[3:0]			
MUX3	2102	MUX7_SEL[3:0]				MUX6_SEL[3:0]			
MUX2	2103	MUX5_SEL[3:0]				MUX4_SEL[3:0]			
MUX1	2104	MUX3_SEL[3:0]				MUX2_SEL[3:0]			
MUX0	2105	MUX1_SEL[3:0]				MUX0_SEL[3:0]			
CE6	2106	EQU[2:0]			U	CHOP_E[1:0]		RTM_E	CE_E
CE5	2107	U	U	U	SUM_SAMPS[12:8]				
CE4	2108	SUM_SAMPS[7:0]							
CE3	2109	U	CE_LCTN[6:0] for 71M6543GT/GHT, CE_LCTN[5:0] for 71M6543FT/HT						
CE2	210A	PLS_MAXWIDTH[7:0]							
CE1	210B	PLS_INTERVAL[7:0]							
CE0	210C	R	R	DIFFB_E	DIFFA_E	RFLY_DIS	FIR_LEN[1:0]	PLS_INV	CE0
RTM0	210D	U	U	U	U	U	U	RTM0[9:8]	
RTM0	210E	RTM0[7:0]							
RTM1	210F	RTM1[7:0]							
RTM2	2110	RTM2[7:0]							
RTM3	2111	RTM3[7:0]							
FIR_EXT	2112	U	U	U	U	SLOT_EXT[3:0]			
CLOCK GENERATION									
CKGN	2200	OUT_SQ[1:0]		ADC_DIV	PLL_FAST	RESET	MPU_DIV[2:0]		
V_{REF} TRIM FUSES									
TRIMT	2309	TRIMT[7:0]							
LCD/DIO									
LCD0	2400	LCD_E	LCD_MODE[2:0]			LCD_ALLCOM	LCD_Y	LCD_CLK[1:0]	
LCD1	2401	LCD_VMODE[1:0]		LCD_BLNKMAP23[5:0]					
LCD2	2402	LCD_BAT	R	LCD_BLNKMAP22[5:0]					
LCD_MAP6	2405	LCD_MAP[55:48]							
LCD_MAP5	2406	LCD_MAP[47:40]							
LCD_MAP4	2407	LCD_MAP[39:32]							
LCD_MAP3	2408	LCD_MAP[31:24]							
LCD_MAP2	2409	LCD_MAP[23:16]							
LCD_MAP1	240A	LCD_MAP[15:8]							
LCD_MAP0	240B	LCD_MAP[7:0]							
LCD4	240C	U	U	U	U	U	LCD_RST	LCD_BLANK	LCD_ON
LCD_DAC	240D	U	U	U	LCD_DAC[4:0]				
SEGDIO0	2410	U	U	LCD_SEG0[5:0]					
SEGDIO1	2411	U	U	LCD_SEG1[5:0]					
SEGDIO2	2412	U	U	LCD_SEG2[5:0]					
SEGDIO3	2413	U	U	LCD_SEG3[5:0]					
SEGDIO4	2414	U	U	LCD_SEG4[5:0]					
SEGDIO5	2415	U	U	LCD_SEG5[5:0]					

Table 11. I/O RAM Locations in Numerical Order (continued)

NAME	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SEGDIO6	2416	U	U	LCD_SEG6[5:0]					
SEGDIO7	2417	U	U	LCD_SEG7[5:0]					
SEGDIO8	2418	U	U	LCD_SEG8[5:0]					
SEGDIO9	2419	U	U	LCD_SEG9[5:0]					
SEGDIO10	241A	U	U	LCD_SEG10[5:0]					
SEGDIO11	241B	U	U	LCD_SEG11[5:0]					
SEGDIO12	241C	U	U	LCD_SEG12[5:0]					
SEGDIO13	241D	U	U	LCD_SEG13[5:0]					
SEGDIO14	241E	U	U	LCD_SEG14[5:0]					
SEGDIO15	241F	U	U	LCD_SEG15[5:0]					
SEGDIO16	2420	U	U	LCD_SEG16[5:0]					
SEGDIO17	2421	U	U	LCD_SEG17[5:0]					
SEGDIO18	2422	U	U	LCD_SEG18[5:0]					
SEGDIO19	2423	U	U	LCD_SEG19[5:0]					
SEGDIO20	2424	U	U	LCD_SEG20[5:0]					
SEGDIO21	2425	U	U	LCD_SEG21[5:0]					
SEGDIO22	2426	U	U	LCD_SEG22[5:0]					
SEGDIO23	2427	U	U	LCD_SEG23[5:0]					
SEGDIO24	2428	U	U	LCD_SEG24[5:0]					
SEGDIO25	2429	U	U	LCD_SEG25[5:0]					
SEGDIO26	242A	U	U	LCD_SEG26[5:0]					
SEGDIO27	242B	U	U	LCD_SEG27[5:0]					
SEGDIO28	242C	U	U	LCD_SEG28[5:0]					
SEGDIO29	242D	U	U	LCD_SEG29[5:0]					
SEGDIO30	242E	U	U	LCD_SEG30[5:0]					
SEGDIO31	242F	U	U	LCD_SEG31[5:0]					
SEGDIO32	2430	U	U	LCD_SEG32[5:0]					
SEGDIO33	2431	U	U	LCD_SEG33[5:0]					
SEGDIO34	2432	U	U	LCD_SEG34[5:0]					
SEGDIO35	2433	U	U	LCD_SEG35[5:0]					
SEGDIO36	2434	U	U	LCD_SEG36[5:0]					
SEGDIO37	2435	U	U	LCD_SEG37[5:0]					
SEGDIO38	2436	U	U	LCD_SEG38[5:0]					
SEGDIO39	2437	U	U	LCD_SEG39[5:0]					
SEGDIO40	2438	U	U	LCD_SEG40[5:0]					
SEGDIO41	2439	U	U	LCD_SEG41[5:0]					
SEGDIO42	243A	U	U	LCD_SEG42[5:0]					
SEGDIO43	243B	U	U	LCD_SEG43[5:0]					
SEGDIO44	243C	U	U	LCD_SEG44[5:0]					
SEGDIO45	243D	U	U	LCD_SEG45[5:0]					
SEGDIO46	243E	U	U	LCD_SEG46[5:0]					
SEGDIO47	243F	U	U	LCD_SEG47[5:0]					
SEGDIO48	2440	U	U	LCD_SEG48[5:0]					
SEGDIO49	2441	U	U	LCD_SEG49[5:0]					
SEGDIO50	2442	U	U	LCD_SEG50[5:0]					
SEGDIO51	2443	U	U	LCD_SEG51[5:0]					
SEGDIO52	2444	U	U	LCD_SEG52[5:0]					
SEGDIO53	2445	U	U	LCD_SEG53[5:0]					
SEGDIO54	2446	U	U	LCD_SEG54[5:0]					
SEGDIO55	2447	U	U	LCD_SEG55[5:0]					
DIO_R5	2450	U	U	U	U	U	DIO_RPB[2:0]		
DIO_R4	2451	U	DIO_R11[2:0]			U	DIO_R10[2:0]		

Table 11. I/O RAM Locations in Numerical Order (continued)

NAME	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIO_R3	2452	U	DIO_R9[2:0]			U	DIO_R8[2:0]		
DIO_R2	2453	U	DIO_R7[2:0]			U	DIO_R6[2:0]		
DIO_R1	2454	U	DIO_R5[2:0]			U	DIO_R4[2:0]		
DIO_R0	2455	U	DIO_R3[2:0]			U	DIO_R2[2:0]		
DIO0	2456	DIO_EEX[1:0]		U	UMUX_SEL	OPT_TXE[1:0]		OPT_TXMOD	OPT_TXINV
DIO1	2457	DIO_PW	DIO_PV	OPT_FDC[1:0]		U	OPT_RXDIS	OPT_RXINV	OPT_TXINV
DIO2	2458	DIO_PX	DIO_PY	U	OUT_SQE	U	U	U	U
NONVOLATILE BITS									
TMUX	2502	U	U	TMUX[5:0]					
TMUX2	2503	U	U	U	TMUX2[4:0]				
TC_A1	2508	U	U	U	U	U	U	TC_A[9:8]	
TC_A2	2509	TC_A[7:0]							
TC_B1	250A	U	U	U	U	TC_B[11:8]			
TC_B2	250B	TC_B[7:0]							
PQMASK	2511	U	U	U	U	U	PQMASK[2:0]		
TSEL	2518	U	U	U	TEMP_SELE	TEMP_SEL[3:0]			
TSBASE1	2519	U	U	U	U	U	SBASE[10:8]		
TSBASE2	251A	SBASE[7:0]							
TSMAX	251B	U	SMAX[6:0]						
TSMIN	251C	U	SMIN[6:0]						
TSFILT	251D	U	U	U	U	SFILT[3:0]			
71M6x03 REMOTE INTERFACE									
REMOTE2	2602	RMT_RD[15:8]							
REMOTE1	2603	RMT_RD[7:0]							
RBITS									
INT1_E	2700	EX_EEX	EX_XPULSE	EX_YPULSE	EX_RTCT	EX_TCTEMP	EX_RTC1M	EX_RTC1S	EX_XFER
INT2_E	2701	EX_SPI	EX_WPULSE	EX_VPULSE	U	U	U	U	U
SECURE	2702	FLSH_UNLOCK[3:0]				R	FLSH_RDE	FLSH_WRE	R
Analog0	2704	VREF_CAL	VREF_DIS	PRE_E	ADC_E	BCURR	SPARE[2:0]		
INTBITS	2707	U	INT6	INT5	INT4	INT3	INT2	INT1	INT0
FLAG0	SFR E8	IE_EEX	IE_XPULSE	IE_YPULSE	IE_RTCT	IE_TCTEMP	IE_RTC1M	IE_RTC1S	IE_XFER
FLAG1	SFR F8	IE_SPI	IE_WPULSE	IE_VPULSE	U	U	U	U	PB_STATE
STAT	SFR F9	U	U	U	PLL_OK	U	VSTAT[2:0]		
REMOTE0	SFR FC	U	PERR_RD	PERR_WR	RCMD[4:0]				
SPI1	SFR FD	SPI_CMD[7:0]							
SPI0	2708	SPI_STAT[7:0]							
RCE0	2709	CHOPR[1:0]		R	R	RMT_E	R	R	R
RTMUX	270A	U	R	R	R	U	TMUXRA[2:0]		
INFO_PG	270B	U	U	U	U	U	U	U	INFO_PG
DIO3	270C	U	U	PORT_E	SPI_E	SPI_SAFE	U	U	U
TNM1	2710	U	TEMP_NMAX[14:8]						
TNM2	2711	TEMP_NMAX[7:0]							
TM1	2712	U	U	U	U	TEMP_M[11:8]			
TM2	2713	TEMP_M[7:0]							
TNB1	2714	TEMP_NBAT[15:8]							
TNB2	2715	TEMP_NBAT[7:0]							
NV RAM AND RTC									
NVRAMxx	2800	NVRAM[0] to NVRAM[7F] - 128 bytes, direct access, 0x2800 to 0x287F							
WAKE	2880	WAKE_TMR[7:0]							
STEMP1	2881	STEMP[15:8]							

Table 11. I/O RAM Locations in Numerical Order (continued)

NAME	ADDR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STEMP0	2882	STEMP[7:0]							
BSENSE	2885	BSENSE[7:0]							
PQ2	2886	U	U	U	PQ[20:16]				
PQ1	2887	PQ[15:8]							
PQ0	2888	PQ[7:0]							
RTC0	2890	RTC_WR	RTC_RD	U	RTC_FAIL	U	U	U	U
RTC2	2892	RTC_SBSC[7:0]							
RTC3	2893	U	U	RTC_SEC[5:0]					
RTC4	2894	U	U	RTC_MIN[5:0]					
RTC5	2895	U	U	U	RTC_HR[4:0]				
RTC6	2896	U	U	U	U	U	RTC_DAY[2:0]		
RTC7	2897	U	U	U	RTC_DATE[4:0]				
RTC8	2898	U	U	U	U	RTC_MO[3:0]			
RTC9	2899	RTC_YR[7:0]							
RTC11	289C	U	U	U	U	TC_C[11:8]			
RTC12	289D	TC_C[7:0]							
RTC13	289E	U	U	RTC_TMIN[5:0]					
RTC14	289F	U	U	U	RTC_THR[4:0]				
TEMP	28A0	TEMP_BSEL	TEMP_PWR	OSC_COMP	TEMP_BAT	TBYTE_BUSY	TEMP_PER[2:0]		
WF1	28B0	WF_CSTART	WF_RST	WF_RSTBIT	WF_OVF	WF_ERST	WF_BADVDD	U	U
WF2	28B1	U	WF_TEMP	WF_TMR	WF_RX	WF_PB	WF_DIO4	WF_DIO52	WF_DIO55
MISC	28B2	SLEEP	LCD_ONLY	WAKE_ARM	U	U	U	U	U
WAKE_E	28B3	U	EW_TEMP	U	EW_RX	EW_PB	EW_DIO4	EW_DIO52 †	EW_DIO55
WDRST	28B4	WD_RST	TEMP_START	U	U	U	U	U	U
MPU PORTS									
P3	SFR B0	DIO_DIR[15:12]				DIO[15:12]			
P2	SFR A0	DIO_DIR[11:8]				DIO[11:8]			
P1	SFR 90	DIO_DIR[7:4]				DIO[7:4]			
P0	SFR 80	DIO_DIR[3:0]				DIO[3:0]			
FLASH									
FLASH_ ERASE	SFR 94	FLSH_ERASE[7:0]							
FLSH_CTL	SFR B2	PREBOOT	SECURE	U	U	FLSH_PEND	FLSH_PSTWR	FLSH_MEEN	FLSH_PWE
FLSH_BANK	SFR B6	U	U	U	U	U	U	FLSH_BANK[1:0]	
FLSH_ PGADR	SFR B7	FLSH_PGADR[6:0]							U
I²C									
EEDATA	SFR 9E	EEDATA[7:0]							
EECTRL	SFR 9F	EECTRL[7:0]							

I/O RAM Map: Details

Writable bits are written by the MPU into configuration RAM. Typically, they are initially stored in flash memory and copied to the configuration RAM by the MPU. Some of the more frequently programmed bits are mapped to the MPU SFR memory space. The remaining bits are mapped to the address space 0x2XXX. The RST and WK columns describe the bit values upon reset and wake, respectively. No entry in one of these columns means the bit is either read-only or is powered by the NV supply and is not initialized. Write-only bits return zero when they are read.

Locations that are shaded in grey are nonvolatile (i.e., battery-backed).

Table 12. I/O RAM Locations in Alphabetical Order

NAME	LOCATION	RST	WK	DIR	DESCRIPTION
ADC_E	2704[4]	0	0	R/W	Enables ADC and V_{REF}. When disabled, reduces bias current.
ADC_DIV	2200[5]	0	0	R/W	ADC_DIV controls the rate of the ADC and FIR clocks. The ADC_DIV setting determines whether MCK is divided by 4 or 8: 0 = MCK/4 1 = MCK/8 The resulting ADC and FIR clock is as shown below.
					PLL_FAST = 0 / **PLL_FAST = 1** MCK: 6.291456MHz / 19.660800MHz ADC_DIV = 0: 1.572864MHz / 4.9152MHz ADC_DIV = 1: 0.786432MHz / 2.4576MHz
BCURR	2704[3]	0	0	R/W	Connects a 100µA load to the battery selected by TEMP_BSEL.
BSENSE[7:0]	2885[7:0]	–	–	R	The result of the battery measurement.
CE_E	2106[0]	0	0	R/W	CE enable.
CE_LCTN[6:0] CE_LCTN[5:0]	2109[6:0] 2109[5:0]	31	31	R/W	CE program location. The starting address for the CE program is 1024 x CE_LCTN. CE_LCTN[6:0], 2109[6:0] for 71M6543GT/GHT; CE_LCTN[5:0], 2109[5:0] for 71M6543HT/GHT.
CHIP_ID[15:0]	2300[7:0] 2301[7:0]	0 0	0 0	R R	These bytes contain the chip identification. CHIP_ID[15:0]: 71M6543FT (0810h) 71M6543HT (11ACh) 71M6543GT (2019h) 71M6543GHT (2021h)
CHOP_E[1:0]	2106[3:2]	0	0	R/W	Chop enable for the reference bandgap circuit. The value of CHOP changes on the rising edge of MUXSYNC according to the value in CHOP_E: 00 = toggle[1] 01 = positive 10 = reversed 11 = toggle [1]except at the mux sync edge at the end of an accumulation interval.
CHOPR[1:0]	2709[7:6]	00	00	R/W	The CHOP settings for the remote sensor. 00 = Auto chop. Change every MUX frame. 01 = Positive 10 = Negative 11 = Auto chop. Same as 00.
DIFF0_E	210C[4]	0	0	R/W	Enables IADC0-IADC1 differential configuration.
DIFF2_E	210C[5]	0	0	R/W	Enables IADC2-IADC3 differential configuration.
DIFF4_E	210C[6]	0	0	R/W	Enables IADC4-IADC5 differential configuration.
DIFF6_E	210C[7]	0	0	R/W	Enables IADC6-IADC7 differential configuration.
DIO_R2[2:0] DIO_R3[2:0] DIO_R4[2:0] DIO_R5[2:0] DIO_R6[2:0] DIO_R7[2:0] DIO_R8[2:0] DIO_R9[2:0] DIO_R10[2:0] DIO_R11[2:0] DIO_RPB[2:0]	2455[2:0] 2455[6:4] 2454[2:0] 2454[6:4] 2453[2:0] 2453[6:4] 2452[2:0] 2452[6:4] 2451[2:0] 2451[6:4] 2450[2:0]	0 0 0 0 0 0 0 0 0 0 0	-	R/W	Connects PB and dedicated I/O pins DIO2 through DIO11 to internal resources. If more than one input is connected to the same resource, the MULTIPLE column below specifies how they are combined. **DIO_Rx** / **RESOURCE** / **MULTIPLE** 0: NONE / – 1: Reserved / OR 2: T0 (Timer0 clock or gate) / OR 3: T1 (Timer1 clock or gate) / OR 4: IO interrupt (int0) / OR 5: IO interrupt (int1) / OR
DIO_DIR[15:12] DIO_DIR[11:8] DIO_DIR[7:4] DIO_DIR[3:0]	SFR B0[7:4] SFR A0[7:4] SFR 90[7:4] SFR 80[7:4]	F	F	R/W	Programs the direction of the first 16 DIO pins. 1 indicates output. Ignored if the pin is not configured as I/O. See DIO_PV and DIO_PW for special option for the SEGDIO0 and SEGDIO1 outputs. See DIO_EEX for special option for SEGDIO2 and SEGDIO3. Note that the direction of DIO pins above 15 is set by SEGDIOx[1]. See PORT_E to avoid power-up spikes.
DIO[15:12] DIO[11:8] DIO[7:4] DIO[3:0]	SFR B0[3:0] SFR A0[3:0] SFR 90[3:0] SFR 80[3:0]	F	F	R/W	The value on the first 16 DIO pins. Pins configured as LCD reads zero. When written, changes data on pins configured as outputs. Pins configured as LCD or input ignore writes. Note that the data for DIO pins above 15 is set by SEGDIOx[0].

Table 12. I/O RAM Locations in Alphabetical Order (continued)

<table>
<tr><th>NAME</th><th>LOCATION</th><th>RST</th><th>WK</th><th>DIR</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="5">DIO_EEX[1:0]</td><td rowspan="5">2456[7:6]</td><td rowspan="5">0</td><td rowspan="5">-</td><td rowspan="5">R/W</td><td>When set, converts pins SEGDIO3/SEGDIO2 to interface with external EEPROM. SEGDIO2 becomes SDCK and SEGDIO3 becomes bidirectional SDATA, but only if LCD_MAP[2] and LCD_MAP[3] are cleared.</td></tr>
<tr><td>DIO_EEX[1:0] | FUNCTION</td></tr>
<tr><td>00 | Disable EEPROM interface</td></tr>
<tr><td>01 | 2-Wire EEPROM interface
10 | 3-Wire EEPROM interface</td></tr>
<tr><td>11 | 3-Wire EEPROM interface with separate DO (DIO3) and DI (DIO8) pins.</td></tr>
<tr><td>DIO_PV</td><td>2457[6]</td><td>0</td><td>–</td><td>R/W</td><td>Causes VARPULSE to be output on pin SEGDIO1, if LCD_MAP[1] = 0.</td></tr>
<tr><td>DIO_PW</td><td>2457[7]</td><td>0</td><td>–</td><td>R/W</td><td>Causes WPULSE to be output on pin SEGDIO0, if LCD_MAP[0] = 0.</td></tr>
<tr><td>DIO_PX</td><td>2458[7]</td><td>0</td><td>–</td><td>R/W</td><td>Causes XPULSE to be output on pin SEGDIO6, if LCD_MAP[6] = 0.</td></tr>
<tr><td>DIO_PY</td><td>2458[6]</td><td>0</td><td>–</td><td>R/W</td><td>Causes YPULSE to be output on pin SEGDIO7, if LCD_MAP[7] = 0.</td></tr>
<tr><td>EEDATA[7:0]</td><td>SFR 9E</td><td>0</td><td>0</td><td>R/W</td><td>Serial EEPROM interface data.</td></tr>
<tr><td>EECTRL[7:0]</td><td>SFR 9F</td><td>0</td><td>0</td><td>R/W</td><td>Serial EEPROM interface control.
<table>
<tr><th>STATUS BIT</th><th>NAME</th><th>READ/ WRITE</th><th>RESET STATE</th><th>POLARITY</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>ERROR</td><td>R</td><td>0</td><td>Positive</td><td>1 when an illegal command is received.</td></tr>
<tr><td>6</td><td>BUSY</td><td>R</td><td>0</td><td>Positive</td><td>1 when serial data bus is busy.</td></tr>
<tr><td>5</td><td>RX_ACK</td><td>R</td><td>1</td><td>Positive</td><td>1 indicates that the EEPROM sent an ACK bit.</td></tr>
</table></td></tr>
<tr><td>EQU[2:0]</td><td>2106[7:5]</td><td>0</td><td>0</td><td>R/W</td><td>Specifies the power equation.
<table>
<tr><th>EQU[2:0]</th><th>DESCRIPTION</th><th>ELEMENT 0</th><th>ELEMENT 1</th><th>ELEMENT 2</th><th>RECOMMENDED MUX SEQUENCE</th></tr>
<tr><td>3</td><td>2 element 4W 3ϕ Delta</td><td>VA(IA-IB)/2</td><td>0</td><td>VC x IC</td><td>IA VA IB VB IC VC</td></tr>
<tr><td>4</td><td>2 element 4W 3ϕ Wye</td><td>VA(IA-IB)/2</td><td>VB(IC-IB)/2</td><td>0</td><td>IA VA IB VB IC VC</td></tr>
<tr><td>5</td><td>2 element 4W 3ϕ Wye</td><td>VA x IA</td><td>VB x IB</td><td>VC x IC</td><td>IA VA IB VB IC VC</td></tr>
</table>
Note: The available CE codes implement only equation 5. Contact your Maxim representative to obtain CE codes for equation 3 or 4.</td></tr>
<tr><td>EX_XFER
EX_RTC1S
EX_RTC1M
EX_TCTEMP
EX_RTCT
EX_SPI
EX_EEX
EX_XPULSE
EX_YPULSE
EX_WPULSE
EX_VPULSE</td><td>2700[0]
2700[1]
2700[2]
2700[3]
2700[4]
2701[7]
2700[7]
2700[6]
2700[5]
2701[6]
2701[5]</td><td>0</td><td>0</td><td>R/W</td><td>Interrupt enable bits. These bits enable the XFER_BUSY, the RTC_1SEC, etc. The bits are set by hardware and cannot be set by writing a 1. The bits are reset by writing 0. Note that if one of these interrupts is to enabled, its corresponding 8051 EX enable bit must also be set.</td></tr>
<tr><td>EW_DIO4</td><td>28B3[2]</td><td>0</td><td>–</td><td>R/W</td><td>Connects SEGDIO4 to the WAKE logic and permits SEGDIO4 rising to wake the part. This bit has no effect unless DIO4 is configured as a digital input.</td></tr>
<tr><td>EW_DIO52</td><td>28B3[1]</td><td>0</td><td>–</td><td>R/W</td><td>Connects SEGDIO52 to the WAKE logic and permits SEGDIO52 rising to wake the part. This bit has no effect unless SEGDIO52 is configured as a digital input.</td></tr>
<tr><td>EW_DIO55</td><td>28B3[0]</td><td>0</td><td>–</td><td>R/W</td><td>Connects SEGDIO55 to the WAKE logic and permits SEGDIO55 rising to wake the part. This bit has no effect unless SEGDIO55 is configured as a digital input.</td></tr>
<tr><td>EW_PB</td><td>28B3[3]</td><td>0</td><td>–</td><td>R/W</td><td>Connects PB to the WAKE logic and permits PB rising to wake the part. PB is always configured as an input.</td></tr>
<tr><td>EW_RX</td><td>28B3[4]</td><td>0</td><td>–</td><td>R/W</td><td>Connects RX to the WAKE logic and permits RX rising to wake the part. See the WAKE description on page 84 for de-bounce issues.</td></tr>
</table>

Table 12. I/O RAM Locations in Alphabetical Order (continued)

<table>
<tr><th>NAME</th><th>LOCATION</th><th>RST</th><th>WK</th><th>DIR</th><th>DESCRIPTION</th></tr>
<tr><td>EW_TEMP</td><td>28B3[5]</td><td>0</td><td>–</td><td>R/W</td><td>Connects the temperature range check hardware to the WAKE logic and permits the range check hardware to wake the part.</td></tr>
<tr><td>FIR_LEN[1:0]</td><td>210C[2:1]</td><td>0</td><td>0</td><td>R/W</td><td>Determines the number of ADC cycles in the ADC decimation FIR filter.
PLL_FAST = 1:
<table>
<tr><th>FIR_LEN[1:0]</th><th>ADC CYCLES</th></tr>
<tr><td>00</td><td>141</td></tr>
<tr><td>01</td><td>288</td></tr>
<tr><td>10</td><td>384</td></tr>
</table>
PLL_FAST = 0:
<table>
<tr><th>FIR_LEN[1:0]</th><th>ADC CYCLES</th></tr>
<tr><td>00</td><td>135</td></tr>
<tr><td>01</td><td>276</td></tr>
<tr><td>10</td><td>Not allowed</td></tr>
</table>
The ADC LSB size and full-scale values depend on the FIR_LEN[1:0] setting.</td></tr>
<tr><td>FLSH_BANK</td><td>SFR B6[1:0]</td><td>01</td><td>01</td><td>R/W</td><td>Flash Bank Selection
<table>
<tr><th>FLSH_BANK[1:0]</th><th>ADDRESS RANGE FOR LOWER BANK (0x0000–0x7FFF)</th><th>ADDRESS RANGE FOR UPPER BANK (0x8000–0x7FFF)</th></tr>
<tr><td>00</td><td>0x0000–0x7FFF</td><td>0x0000–0x7FFF</td></tr>
<tr><td>01</td><td>0x0000–0x7FFF</td><td>0x8000–0x7FFF</td></tr>
<tr><td>10</td><td>0x0000–0x7FFF</td><td>0x10000–0x17FFFF</td></tr>
<tr><td>11</td><td>0x0000–0x7FFF</td><td>0x18000–0x1FFFF</td></tr>
</table></td></tr>
<tr><td>FLSH_ERASE[7:0]</td><td>SFR 94[7:0]</td><td>0</td><td>0</td><td>W</td><td>Flash Erase Initiate
FLSH_ERASE is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for FLSH_ERASE in order to initiate the appropriate Erase cycle.
(default = 0x00).
0x55 = Initiate Flash Page Erase cycle. Must be proceeded by a write to FLSH_PGADR[6:0] (SFR 0xB7[7:1]).
0xAA = Initiate Flash Mass Erase cycle. Must be proceeded by a write to FLSH_MEEN and the ICE port must be enabled.
Any other pattern written to FLSH_ERASE has no effect.</td></tr>
<tr><td>FLSH_MEEN</td><td>SFR B2[1]</td><td>0</td><td>0</td><td>W</td><td>Mass Erase Enable
0 = Mass Erase disabled (default).
1 = Mass Erase enabled.
Must be re-written for each new Mass Erase cycle.</td></tr>
<tr><td>FLSH_PEND</td><td>SFR B2[3]</td><td>0</td><td>0</td><td>R</td><td>Indicates that a timed flash write is pending. If another flash write is attempted, it is ignored.</td></tr>
<tr><td>FLSH_PGADR[6:0]</td><td>SFR B7[7:1]</td><td>0</td><td>0</td><td>W</td><td>Flash Page Erase Address
Flash Page Address (page 0 thru 63) that is erased during the Page Erase cycle. (default = 0x00).
Must be re-written for each new Page Erase cycle.</td></tr>
<tr><td>FLSH_PSTWR</td><td>SFR B2[2]</td><td>0</td><td>0</td><td>R/W</td><td>Enables timed flash writes. When 1, and if CE_E = 1, flash write requests are stored in a one-element deep FIFO and are executed when CE_BUSY falls. FLSH_PEND can be read to determine the status of the FIFO. If FLSH_PSTWR = 0 or if CE_E = 0, flash writes are immediate.</td></tr>
<tr><td>FLSH_PWE</td><td>SFR B2[0]</td><td>0</td><td>0</td><td>R/W</td><td>Program Write Enable
0 = MOVX commands refer to External RAM Space, normal operation (default).
1 = MOVX @DPTR,A moves A to External Program Space (Flash) @ DPTR.
This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.</td></tr>
<tr><td>FLSH_RDE</td><td>2702[2]</td><td>–</td><td>–</td><td>R</td><td>Indicates that the flash may be read by ICE or SPI slave. FLSH_RDE = (!SECURE)</td></tr>
<tr><td>FLSH_UNLOCK [3:0]</td><td>2702[7:4]</td><td>0</td><td>0</td><td>R/W</td><td>Must be a ‘2’ to enable any flash modification. See the description of Flash security for more details.</td></tr>
<tr><td>FLSH_WRE</td><td>2702[1]</td><td>–</td><td>–</td><td>R</td><td>Indicates that the flash may be written through ICE or SPI slave ports.</td></tr>
</table>

Table 12. I/O RAM Locations in Alphabetical Order (continued)

NAME	LOCATION	RST	WK	DIR	DESCRIPTION
IE_XFER IE_RTC1S IE_RTC1M IE_TCTEMP IE_RTCT IE_SPI IE_EEX IE_XPULSE IE_YPULSE IE_WPULSE IE_VPULSE	SFR E8[0] SFR E8[1] SFR E8[2] SFR E8[3] SFR E8[4] SFR F8[7] SFR E8[7] SFR E8[6] SFR E8[5] SFR F8[4] SFR F8[3]	0	0	R/W	Interrupt flags for external interrupts 2, 5, and 6. These flags monitor the source of the int2, int5, and int6 interrupts (external interrupts to the MPU core). These flags are set by hardware and must be cleared by the software interrupt handler. The IEX2 (SFR 0xC0[1]) and IEX6 (SFR 0xC0[5]) interrupt flags are automatically cleared by the MPU core when it vectors to the interrupt handler. IEX2 and IEX6 must be cleared by writing zero to their corresponding bit positions in SFR 0xC0, while writing ones to the other bit positions that are not being cleared.
INTBITS	2707[6:0]	–	–	R	Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use.
LCD_ALLCOM	2400[3]	0	–	R/W	Configures SEG/COM bits as COM. Has no effect on pins whose LCD_MAP bit is zero.
LCD_BAT	2402[7]	0	–	R/W	Connects the LCD power supply to V_{BAT} in all modes.
LCD_BLNKMAP23[5:0] LCD_BLNKMAP22[5:0]	2401[5:0] 2402[5:0]	0	–	R/W	Identifies which segments connected to SEG23 and SEG22 should blink. 1 means ‘blink.’ The most significant bit corresponds to COM5, the least significant, to COM0.
LCD_CLK[1:0]	2400[1:0]	0	–	R/W	Sets the LCD clock frequency. Note: fw = 32,768Hz **LCD_CLK** → **LCD CLOCK FREQUENCY (Hz)** 00 → 64 01 → 128 10 → 256 11 → 512
LCD_DAC[4:0]	240D[4:0]	0	–	R/W	The LCD contrast DAC. This DAC controls the V_{LCD} voltage and has an output range of 2.5V to 5V. The VLCD voltage is V_{LCD} = 2.5 + 2.5 x LCD_DAC[4:0]/31 Thus, the LSB of the DAC is 80.6mV. The maximum DAC output voltage is limited by $V_{V3P3SYS}$, V_{BAT}, and whether LCD_BSTE = 1.
LCD_E	2400[7]	0	–	R/W	Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs if their LCD_MAP bit is 1.
LCD_MAP[55:48] LCD_MAP[47:40] LCD_MAP[39:32] LCD_MAP[31:24] LCD_MAP[23:16] LCD_MAP[15:8] LCD_MAP[7:0]	2405[7:0] 2406[7:0] 2407[7:0] 2408[7:0] 2409[7:0] 240A[7:0] 240B[7:0]	0 0 0 0 0 0 0	– – – – – – –	R/W R/W R/W R/W R/W R/W R/W	Enables LCD segment driver mode of combined SEGDIO pins. Pins that cannot be configured as outputs (SEG48 through SEG50) become inputs with internal pull ups when their LCD_MAP bit is zero. Also, note that SEG48 through SEG50 are multiplexed with the in-circuit emulator signals. When the ICE_E pin is high, the ICE interface is enabled, and SEG48 through SEG50 become E_RXTX, E_TCLK and E_RST, respectively.
LCD_MODE[2:0]	2400[6:4]	0	–	R/W	Selects the LCD bias and multiplex mode. **LCD_MODE** → **OUTPUT** 000 → 4 states, ⅓ bias 001 → 3 states, ⅓ bias 010 → 2 states, ½ bias 011 → 3 states, ½ bias 100 → Static display 101 → 5 states, ⅓ bias 110 → 6 states, ⅓ bias

Table 12. I/O RAM Locations in Alphabetical Order (continued)

NAME	LOCATION	RST	WK	DIR	DESCRIPTION
LCD_ON LCD_BLANK	240C[0] 240C[1]	0 0	– –	R/W R/W	Turns on or off all LCD segments without changing LCD data. If both bits are set, the LCD display is turned on.
LCD_ONLY	28B2[6]	0	0	W	Puts the IC to sleep, but with LCD display still active. Ignored if system power is present. It awakens when Wake Timer times out, when certain DIO pins are raised, or when system power returns.
LCD_RST	240C[2]	0	–	R/W	Clear all bits of LCD data. These bits affect SEGDIO pins that are configured as LCD drivers. This bit does not auto clear.
LCD_SEG0[5:0]	2410[5:0]	0	–	R/W	SEG Data for SEG0
LCD_SEG1[5:0]	2411[5:0]	0	–	R/W	SEG Data for SEG1
LCD_SEG2[5:0]	2412[5:0]	0	–	R/W	SEG Data for SEG2
LCD_SEG3[5:0]	2413[5:0]	0	–	R/W	SEG Data for SEG3
LCD_SEG4[5:0]	2414[5:0]	0	–	R/W	SEG Data for SEG4
LCD_SEG5[5:0]	2415[5:0]	0	–	R/W	SEG Data for SEG5
LCD_SEG6[5:0]	2416[5:0]	0	–	R/W	SEG Data for SEG6
LCD_SEG7[5:0]	2417[5:0]	0	–	R/W	SEG Data for SEG7
LCD_SEG8[5:0]	2418[5:0]	0	–	R/W	SEG Data for SEG8
LCD_SEG9[5:0]	2419[5:0]	0	–	R/W	SEG Data for SEG9
LCD_SEG10[5:0]	241A[5:0]	0	–	R/W	SEG Data for SEG10
LCD_SEG11[5:0]	241B[5:0]	0	–	R/W	SEG Data for SEG11
LCD_SEG12[5:0]	241C[5:0]	0	–	R/W	SEG Data for SEG12
LCD_SEG13[5:0]	241D[5:0]	0	–	R/W	SEG Data for SEG13
LCD_SEG14[5:0]	241E[5:0]	0	–	R/W	SEG Data for SEG14
LCD_SEG15[5:0]	241F[5:0]	0	–	R/W	SEG Data for SEG15
LCD_SEG16[5:0]	2420[5:0]	0	–	R/W	SEG Data for SEG16
LCD_SEG17[5:0]	2421[5:0]	0	–	R/W	SEG Data for SEG17
LCD_SEG18[5:0]	2422[5:0]	0	–	R/W	SEG Data for SEG18
LCD_SEG19[5:0]	2423[5:0]	0	–	R/W	SEG Data for SEG19
LCD_SEG20[5:0]	2424[5:0]	0	–	R/W	SEG Data for SEG20
LCD_SEG21[5:0]	2425[5:0]	0	–	R/W	SEG Data for SEG21
LCD_SEG22[5:0]	2426[5:0]	0	–	R/W	SEG Data for SEG22
LCD_SEG23[5:0]	2427[5:0]	0	–	R/W	SEG Data for SEG23
LCD_SEG24[5:0]	2428[5:0]	0	–	R/W	SEG Data for SEG24
LCD_SEG25[5:0]	2429[5:0]	0	–	R/W	SEG Data for SEG25
LCD_SEG26[5:0]	242A[5:0]	0	–	R/W	SEG Data for SEG26
LCD_SEG27[5:0]	242B[5:0]	0	–	R/W	SEG Data for SEG27
LCD_SEG28[5:0]	242C[5:0]	0	–	R/W	SEG Data for SEG28
LCD_SEG29[5:0]	242D[5:0]	0	–	R/W	SEG Data for SEG29
LCD_SEG30[5:0]	242E[5:0]	0	–	R/W	SEG Data for SEG30
LCD_SEG31[5:0]	242F[5:0]	0	–	R/W	SEG Data for SEG31
LCD_SEG32[5:0]	2430[5:0]	0	–	R/W	SEG Data for SEG32
LCD_SEG33[5:0]	2431[5:0]	0	–	R/W	SEG Data for SEG33
LCD_SEG34[5:0]	2432[5:0]	0	–	R/W	SEG Data for SEG34
LCD_SEG35[5:0]	2433[5:0]	0	–	R/W	SEG Data for SEG35
LCD_SEG36[5:0]	2434[5:0]	0	–	R/W	SEG Data for SEG36
LCD_SEG37[5:0]	2435[5:0]	0	–	R/W	SEG Data for SEG37
LCD_SEG38[5:0]	2436[5:0]	0	–	R/W	SEG Data for SEG38
LCD_SEG39[5:0]	2437[5:0]	0	–	R/W	SEG Data for SEG39
LCD_SEG40[5:0]	2438[5:0]	0	–	R/W	SEG Data for SEG40
LCD_SEG41[5:0]	2439[5:0]	0	–	R/W	SEG Data for SEG41
LCD_SEG42[5:0]	243A[5:0]	0	–	R/W	SEG Data for SEG42
LCD_SEG43[5:0]	243B[5:0]	0	–	R/W	SEG Data for SEG43
LCD_SEG44[5:0]	243C[5:0]	0	–	R/W	SEG Data for SEG44
LCD_SEG45[5:0]	243D[5:0]	0	–	R/W	SEG Data for SEG45

Table 12. I/O RAM Locations in Alphabetical Order (continued)

NAME	LOCATION	RST	WK	DIR	DESCRIPTION
LCD_SEG46[5:0]	243E[5:0]	0	–	R/W	SEG Data for SEG46
LCD_SEG47[5:0]	243F[5:0]	0	–	R/W	SEG Data for SEG47
LCD_SEG48[5:0]	2440[5:0]	0	–	R/W	SEG Data for SEG48
LCD_SEG49[5:0]	2441[5:0]	0	–	R/W	SEG Data for SEG49
LCD_SEG50[5:0]	2442[5:0]	0	–	R/W	SEG Data for SEG50
LCD_SEG51[5:0]	2443[5:0]	0	–	R/W	SEG Data for SEG51
LCD_SEG52[5:0]	2444[5:0]	0	–	R/W	SEG Data for SEG52
LCD_SEG53[5:0]	2445[5:0]	0	–	R/W	SEG Data for SEG53
LCD_SEG54[5:0]	2446[5:0]	0	–	R/W	SEG Data for SEG54
LCD_SEG55[5:0]	2447[5:0]	0	–	R/W	SEG Data for SEG55
LCD_VMODE[1:0]	2401[7:6]	00	00	R/W	Specifies how V_{LCD} is generated. **LCD_VMODE** / **DESCRIPTION** 11 – External V_{LCD} 10 – LCD DAC enabled 01 – LCD DAC enabled 00 – No DAC. V_{LCD} = V3P3L.
LCD_Y	2400[2]	0	–	R/W	LCD Blink Frequency (ignored if blink is disabled). 1 = 1 Hz, 0 = 0.5 Hz
MPU_DIV[2:0]	2200[2:0]	0	0	R/W	MPU clock rate is: MPU Rate = MCK Rate x $2^{-(2+MPU\_DIV[2:0])}$. The maximum value for MPU_DIV[2:0] is 4. Based on the default values of the PLL_FAST bit and MPU_DIV[2:0], the power up MPU rate is 6.29MHz/4 = 1.5725MHz. The minimum MPU clock rate is 38.4kHz when PLL_FAS T = 1.
MUX2_SEL[3:0]	2104[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 2.
MUX3_SEL[3:0]	2104[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 3.
MUX4_SEL[3:0]	2103[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 4.
MUX5_SEL[3:0]	2103[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 5.
MUX6_SEL[3:0]	2102[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 6.
MUX7_SEL[3:0]	2102[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 7.
MUX8_SEL[3:0]	2101[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 8.
MUX9_SEL[3:0]	2101[7:4]	0	0	R/W	Selects which ADC input is to be converted during time slot 9.
MUX10_SEL[3:0]	2100[3:0]	0	0	R/W	Selects which ADC input is to be converted during time slot 10.
MUX_DIV[3:0]	2100[7:4]	0	0	R/W	MUX_DIV[3:0] is the number of ADC time slots in each MUX frame. The maximum number of time slots is 11.
OPT_BB	2457[0]	0	–	R/W	Configures the input of the optical port to be a DIO pin to allow it to be bit-banged. In this case, DIO5 becomes a third high speed UART.
OPT_FDC[1:0]	2457[5:4]	0	–	R/W	Selects OPT_TX modulation duty cycle. **OPT_FDC** / **FUNCTION** 00 – 50% low 01 – 25% low 10 – 12.5% low 11 – 6.25% low
OPT_RXDIS	2457[2]	0	–	R/W	OPT_RX can be configured as an input to the optical UART or as SEGDIO55. OPT_RXDIS = 0 and LCD_MAP[55] = 0: OPT_RX OPT_RXDIS = 1 and LCD_MAP[55] = 0: DIO55 OPT_RXDIS = 0 and LCD_MAP[55] = 1: SEG55 OPT_RXDIS = 1 and LCD_MAP[55] = 1: SEG55
OPT_RXINV	2457[1]	0	–	R/W	Inverts result from OPT_RX comparator when 1. Affects only the UART input. Has no effect when OPT_RX is used as a DIO input.
OPT_TXE [1:0]	2456[3:2]	00	–	R/W	Configures the OPT_TX output pin. If LCD_MAP[51] = 0: 00 = DIO51, 01 = OPT_TX, 10 = WPULSE, 11 = VARPULSE If LCD_MAP[51] = 1: xx = SEG51
OPT_TXINV	2456[0]	0	–	R/W	Invert OPT_TX when 1. This inversion occurs before modulation.

Table 12. I/O RAM Locations in Alphabetical Order (continued)

NAME	LOCATION	RST	WK	DIR	DESCRIPTION
OPT_TXMOD	2456[1]	0	–	R/W	Enables modulation of OPT_TX. When OPT_TXMOD is set, OPT_TX is modulated when it would otherwise have been zero. The modulation is applied after any inversion caused by OPT_TXINV.
OSC_COMP	28A0[5]	0	–	R/W	Enables the automatic update of the PQ RTC compensation value every time the temperature is measured.
OUT_SQ[1:0]	2200[7:6]	0	0	R/W	Defines the square wave output on SEGDIO15 (if OUT_SQE=1) 00 – Off 01 – 3.2768MHz 10 – 4.9152MHz 11 – 9.83MHz
OUT_SQE	2458[4]	0	0	R/W	Enables the square wave output on SEGDIO15.
PB_STATE	SFR F8[0]	0	0	R	The de-bounced state of the PB pin.
PERR_RD PERR_WR	SFR FC[6] SFR FC[5]	0	0	R/W	The IC sets these bits to indicate that a parity error on the remote sensor has been detected. Once set, the bits are remembered until they are cleared by the MPU.
PLL_OK	SFR F9[4]	0	0	R	Indicates that the clock generation PLL is settled.
PLL_FAST	2200[4]	0	0	R/W	Controls the speed of the PLL and MCK. 1 = 19.66 MHz (XTAL x 600) 0 = 6.29MHz (XTAL x 192)
PLS_ MAXWIDTH[7:0]	210A[7:0]	FF	FF	R/W	PLS_MAXWIDTH[7:0] determines the maximum width of the pulse (low-going pulse if PLS_INV = 0 or high-going pulse if PLS_INV = 1). The maximum pulse width is (2 x PLS_MAXWIDTH[7:0] + 1) x TI. Where TI is PLS_INTERVAL[7:0] in units of CK_FIR clock cycles. If PLS_INTERVAL[7:0] = 0 or PLS_MAXWIDTH[7:0] = 255, no pulse width checking is performed and the output pulses have 50% duty cycle.
PLS_ INTERVAL[7:0]	210B[7:0]	0	0	R/W	PLS_INTERVAL[7:0] determines the interval time between pulses. The time between output pulses is PLS_INTERVAL[7:0] x 4 in units of CK_FIR clock cycles. If PLS_INTERVAL[7:0] = 0, the FIFO is not used and pulses are output as soon as the CE issues them. PLS_INTERVAL[7:0] is calculated as follows: PLS_INTERVAL[7:0] = Floor (Mux frame duration in CK_FIR cycles/ CE pulse updates per Mux frame/4) For example, since the 71M654xT CE code is written to generate 6 pulses in one integration interval, when the FIFO is enabled (i.e., PLS_INTERVAL[7:0] ≠ 0) and that the frame duration is 1950 CK_FIR clock cycles, PLS_INTERVAL[7:0] should be written with Floor(1950/6/4) = 81 so that the five pulses are evenly spaced in time over the integration interval and the last pulse is issued just prior to the end of the interval.
PLS_INV	210C[0]	0	0	R/W	Inverts the polarity of WPULSE, VARPULSE, XPULSE and YPULSE. Normally, these pulses are active low. When inverted, they become active high.
PORT_E	270C[5]	0	0	R/W	Enables outputs from the pins SEGDIO0-SEGDIO15. PORT_E = 0 after reset and power-up blocks the momentary output pulse that would occur on SEGDIO0 to SEGDIO15.
PQ[20:0]	2886[4:0] 2887[7:0] 2888[7:0]	0	0	R	Temperature compensation value computed by the quadratic compensation formula.
PQMASK	2511[2:0]	0	0	R/W	Sets the length of the PQ mask. The mask is ANDed with the last four bits of PQ according to the table below. PQMASK also determines the length of PULSE_AUTO in TMUX.

PQMASK	MASK	PULSE_AUTO WIDTH
000	0000	1s
001	1000	2s
010	1100	4s
011	1110	8s
100	1111	16s

PRE_E	2704[5]	0	0	R/W	Enables the 8x preamplifier.
PREBOOT	SFRB2[7]	–	–	R	Indicates that preboot sequence is active.
RCMD[4:0]	SFR FC[4:0]	0	0	R/W	When the MPU writes a non-zero value to RCMD[4:0], the IC issues a command to the appropriate remote sensor. When the command is complete, the IC clears RCMD[4:0].
RESET	2200[3]	0	0	W	When set, writes a one to WF_RSTBIT and then causes a reset.
RFLY_DIS	210C[3]	0	0	R/W	Controls how the IC drives the power pulse for the 71M6x03. When set, the power pulse is driven high and low. When cleared, it is driven high followed by an open circuit fly-back interval.

Table 12. I/O RAM Locations in Alphabetical Order (continued)

NAME	LOCATION	RST	WK	DIR	DESCRIPTION
RMT2_E	2709[3]	0	0	R/W	Enables the remote interface.
RMT4_E	2709[4]	0	0	R/W	Enables the remote interface.
RMT6_E	2709[5]	0	0	R/W	Enables the remote interface.
RMT_RD[15:8] RMT_RD[7:0]	2602[7:0] 2603[7:0]	0	0	R	Response from remote read request.
RTC_FAIL	2890[4]	0	0	R/W	Indicates that a count error has occurred in the RTC and that the time is not trustworthy. This bit can be cleared by writing a 0.
RTC_RD	2890[6]	0	0	R/W	Freezes the RTC shadow register so it is suitable for MPU reads. When RTC_RD is read, it returns the status of the shadow register: 0 = up to date, 1 = frozen.
RTC_SBSC[7:0]	2892[7:0]	–	–	R	Time remaining until the next 1 second boundary. LSB = 1/256 second.
RTC_TMIN[5:0]	289E[5:0]	0	–	R/W	The target minutes register. See RTC_THR below.
RTC_THR[4:0]	289F[4:0]	0	–	R/W	The target hours register. The RTC_T interrupt occurs when RTC_MIN becomes equal to RTC_TMIN and RTC_HR becomes equal to RTC_THR.
RTC_WR	2890[7]	0	0	R/W	Freezes the RTC shadow register so it is suitable for MPU writes. When RTC_WR is cleared, the contents of the shadow register are written to the RTC counter on the next RTC clock (~500 Hz). When RTC_WR is read, it returns 1 as long as RTC_WR is set. It continues to return one until the RTC counter actually updates.
RTC_SEC[5:0] RTC_MIN[5:0] RTC_HR[4:0] RTC_DAY[2:0] RTC_DATE[4:0] RTC_MO[3:0] RTC_YR[7:0]	2893[5:0] 2894[5:0] 2895[4:0] 2896[2:0] 2897[4:0] 2898[3:0] 2899[7:0]	– – – – – – –	– – – – – – –	R/W	The RTC interface registers. These are the year, month, day, hour, minute and second parameters for the RTC. The RTC is set by writing to these registers. Year 00 and all others divisible by 4 are defined as a leap year. SEC 00 to 59 MIN 00 to 59 HR 00 to 23 (00 = Midnight) DAY 01 to 07 (01 = Sunday) DATE 01 to 31 MO 01 to 12 YR 00 to 99 Each write operation to one of these registers must be preceded by a write to 0x20A0.
RTM_E	2106[1]	0	0	R/W	Real Time Monitor enable. When 0, the RTM output is low.
RTM0[9:8] RTM0[7:0] RTM1[7:0] RTM2[7:0] RTM3[7:0]	210D[1:0] 210E[7:0] 210F[7:0] 2110[7:0] 2111[7:0]	0 0 0 0 0	0 0 0 0 0	R/W	Four RTM probes. Before each CE code pass, the values of these registers are serially output on the RTM pin. The RTM registers are ignored when RTM_E = 0. Note that RTM0 is 10 bits wide. The others assume the upper two bits are 00.
SBASE:[10:0]	2519[2:0] 251A[7:0]	0	0	R/W	Base temperature for limit checking
SECURE	SFR B2[6]	0	0	R/W	Inhibits erasure of page 0 and flash addresses above the beginning of CE code as defined by CE_LCTN[6:0] for 71M6543GT/GHT and CE_LCTN[5:0] for 71M6543FT/HT. Also inhibits the read of flash via the SPI and ICE port.
SFILT	251D[3:0]	0	0	R/W	Filter variable for wake on temperature extremes.
SLEEP	28B2[7]	0	0	W	Puts the part to SLP mode. Ignored if system power is present. The part wakes when the Wake timer expires, when push button is pushed, or when system power returns.
SLOT_EXT[3:0]	2112[3:0]	0	0	R/S	If non-zero, will extend the duration of time slot zero by up to 15 extra crystal cycles. The ADC result for time slot zero will be left-shifted nine bits if SLOT_EXT=0 and four bits if SLOT_EXT≠0.
SMAX[6:0]	251B[6:0]	0	0	R/W	Maximum temperature for limit checking
SMIN[6:0]	251C[6:0]	0	0	R/W	Minimum temperature for limit checking
SPI_CMD[7:0]	SFR FD[7:0]	–	–	R	SPI command register for the 8-bit command from the bus master.
SPI_E	270C[4]	1	1	R/W	SPI port enable. Enables SPI interface on pins SEGDIO36 – SEGDIO39. Requires that LCD_MAP[36-39] = 0.
SPI_SAFE	270C[3]	0	0	R/W	Limits SPI writes to SPI_CMD and a 16-byte region in DRAM. No other writes are permitted.
SPI_STAT[7:0]	2708[7:0]	0	0	R	SPI_STAT contains the status results from the previous SPI transaction. Bit 7: Ready error: The 71M654xT was not ready to read or write as directed by the previous command. Bit 6: Read data parity: This bit is the parity of all bytes read from the 71M654xT in the previous command. Does not include the SPI_STAT byte. Bit 5: Write data parity: This bit is the overall parity of the bytes written to the 71M654xT in the previous command. It includes CMD and ADDR bytes. Bit 4-2: Bottom 3 bits of the byte count. Does not include ADDR and CMD bytes. One, two, and three byte instructions return 111. Bit 1: SPI FLASH mode: This bit is zero when the TEST pin is zero. Bit 0: SPI FLASH mode ready: Used in SPI FLASH mode. Indicates that the flash is ready to receive another write instruction.

Table 12. I/O RAM Locations in Alphabetical Order (continued)

NAME	LOCATION	RST	WK	DIR	DESCRIPTION
STEMP[15:0]	2881[7:0] 2882[7:0]	–	–	R	The result of the temperature measurement.
STEMP_T22_P	SFR A8, SFR A9				STEMP measurement at T22 probe.
STEMP_T85_P	SFR AA, SFR AB				STEMP measurement at T85 probe.
SUM_SAMPS[12:8] SUM_SAMPS[7:0]	2107[4:0] 2108[7:0]	0	0	R/W	The number of multiplexer cycles per XFER_BUSY interrupt. Maximum value is 8191 cycles.
T22_P	SFR 9A				Probe temperature, LSB = 0.1°C. 2's complement = 10(T -22).
T85_P	SFR A6, SFR A7				Probe temperature at +85°C, LSB = 0.1°C. 2's complement = 10(T - 22).
TC_A[9:0]	2508[1:0] 2509[7:0]	0	0	R/W	Temperature compensation factor for quadratic compensation.
TC_B[11:0]	250A[3:0] 205B[7:0]	0	0	R/W	Temperature compensation factor for quadratic compensation.
TC_C[11:0]	289C[3:0] 289D[7:0]	0	0	R/W	Temperature compensation factor for quadratic compensation.
TEMP_22[12:8] TEMP_22[7:0]	230A[4:0] 230B[7:0]	0	–	R	Storage location for STEMP at 22NC. STEMP is an 11-bit word.
TEMP_BAT	28A0[4]	0	–	R/W	Causes V_{BAT} to be measured whenever a temperature measurement is performed.
TEMP_BSEL	28A0[7]	0	–	R/W	Selects which battery is monitored by the temperature sensor: 1 = V_{BAT}, 0 = V_{BAT_RTC}
TBYTE_BUSY	28A0[3]	0	0	R	Indicates that hardware is still writing the 0x28A0 byte. Additional writes to this byte will be locked out while it is one. Write duration could be as long as 6ms.
TEMP_PER[2:0]	28A0[2:0]	0	–	R/W	Sets the period between temperature measurements. Automatic measurements can be enabled in any mode (MSN, BRN, LCD, or SLP). TEMP_PER = 0 disables automatic temperature updates, in which case TEMP_START may be used by the MPU to initiate a one-shot temperature measurement. **TEMP_PER** / **TIME (s)** 0 / No temperature updates 1-6 / $2^{(3+TEMP\_PER)}$ 7 / Continuous updates In automatic mode, TEMP_START is the indicator for the temperature sensor status: TEMP_START = 1 (temperature sensor is busy, cannot measure temperature) TEMP_START = 0 (temperature sensor is idle, can measure temperature)
TEMP_PWR	28A0[6]	0	–	R/W	Selects the power source for the temp sensor: 1 = V_{V3P3D}, 0 = V_{BAT_RTC}. This bit is ignored in SLP and LCD modes, where the temp sensor is always powered by V_{BAT_RTC}.
TEMP_START	28B4[6]	0	0	R/W	When TEMP_PER = 0 automatic temperature measurements are disabled, and TEMP_START may be set by the MPU to initiate a one-shot temperature measurement. In automatic mode, TEMP_START is the indicator for the temperature sensor status: TEMP_START = 1 (temperature sensor is busy, cannot measure temperature) TEMP_START = 0 (temperature sensor is idle, can measure temperature) TEMP_START is ignored in SLP and LCD modes. Hardware clears TEMP_START when the temperature measurement is complete.
TMUX[5:0]	2502[5:0]	–	–	R/W	Selects one of 32 signals for TMUXOUT.
TMUX2[4:0]	2503[4:0]	–	–	R/W	Selects one of 32 signals for TMUX2OUT.
TMUXRA[2:0]	270A[2:0]	000	000	R/W	The TMUX setting for the remote isolated sensor (71M6x03).
UMUX_SEL	2456[4]	0	0	R/W	Selects UART1 IO pins. Selects OPT_TX and OPT_RX when 0. Selects SEGDIO17 and SEGDIO16 when 1. If UMUX_SEL = 0, SEGDIO17, and SEGDIO16 are standard DIO pins, reflecting the value of LCD_SEGDIO16[5:0] and LCD_SEGDIO17[5:0].
VREF_CAL	2704[7]	0	0	R/W	Brings the ADC reference voltage out to the V_{REF} pin. This feature is disabled when VREF_DIS=1.
VREF_DIS	2704[6]	0	1	R/W	Disables the internal ADC voltage reference.

Table 12. I/O RAM Locations in Alphabetical Order (continued)

VSTAT[2:0]	SFR F9[2:0]	–	–	R	This word describes the source of power and the status of V_{DD}.
					000: System Power OK. V_{V3P3A}>3.0v. Analog modules are functional and accurate. [V3AOK,V3OK] = 11
					001: System Power Low. 2.8v<V_{V3P3A}<3.0v. Analog modules not accurate. Switchover to battery power is imminent. [V3AOK,V3OK] = 01
					010: Battery power and V_{DD} OK. V_{DD}>2.25v. Full digital functionality. [V3AOK,V3OK] = 00, [VDDOK,VDDgt2] = 11
					011: Battery power and V_{DD}>2.0. Flash writes are inhibited. If the TRIMVDD[5] fuse is blown, PLL_FAST (I/O RAM 0x2200[4]) is cleared. [V3AOK,V3OK] = 00, [VDDOK,VDDgt2] = 01
					101: Battery power and V_{DD}<2.0. When VSTAT=101, processor is nearly out of voltage. Processor failure is imminent. [V3AOK,V3OK] = 00, [VDDOK,VDDgt2] = 00
WAKE_ARM	28B2[5]	0	–	R/W	Arms the WAKE timer and loads it with WAKE_TMR[7:0]. When SLEEP or LCD_ONLY is asserted by the MPU, the WAKE timer becomes active.
NAME	**LOCATION**	**RST**	**WK**	**DIR**	**DESCRIPTION**
WAKE_TMR[7:0]	2880[7:0]	0	–	R/W	Timer duration is WAKE_TMR+1 seconds.
WD_RST	28B4[7]	0	0	W	Reset the WD timer. The WD is reset when a 1 is written to this bit. Writing a one clears and restarts the watch dog timer.
WF_DIO4	28B1[2]	0	–	R	DIO4 wake flag bit. If DIO4 is configured to wake the part, this bit is set whenever the de-bounced version of DIO4 rises. It is held in reset if DI04 is not configured for wakeup.
WF_DIO52	28B1[1]	0	–	R	DIO52 wake flag bit. If DIO52 is configured to wake the part, this bit is set whenever the de-bounced version of DIO52 rises. It is held in reset if DI052 is not configured for wakeup.
WF_DIO55	28B1[0]	0	–	R	DIO55 wake flag bit. If DIO55 is configured to wake the part, this bit is set whenever the de-bounced version of DIO55 rises. It is held in reset if DI055 is not configured for wakeup.
WF_TEMP	28B1[6]	0	–	R	Indicates that the temperature range check hardware caused the part to wake up.
WAKE_ARM	28B2[5]	0	–	R/W	Arms the WAKE timer and loads it with WAKE_TMR[7:0]. When SLEEP or LCD_ONLY is asserted by the MPU, the WAKE timer becomes active.
WF_PB	28B1[3]	0	–	R	Indicates that the PB caused the part to wake.
WF_RX	28B1[4]	0	–	R	Indicates that RX caused the part to wake.
WF_CSTART WF_RST WF_RSTBIT WF_OVF WF_ERST WF_BADVDD	28B0[7] 28B0[6] 28B0[5] 28B0[4] 28B0[3] 28B0[2]	0 1 0 0 0 0	–	R	Indicates that the Reset pin, Reset bit, ERST pin, Watchdog timer, the cold start detector, or bad V_{BAT} caused the part to reset.

Reading the Info Page (71M6543HT/GHT Only)

High-precision trim fuse values provided in the 71M6543HT and 71M6543GHT devices cannot be directly accessed through the I/O RAM space. These trim fuses reside in a special area termed the Info Page. The MPU gains access to the Info Page by setting the INFO_PG (I/O RAM 0x270B[0]) control bit. Once the INFO_PG bit is set, Info Page contents are accessible in program memory space based at the address specified by the contents of CE_LCTN[6:0] (71M6543GHT) or CE_LCTN[5:0] (71M6543HT) (I/O RAM 0x2109[6:0] for 71M6543GHT or 0x2109[5:0] for 71M6543HT). CE_LCTN[6:0] (71M6543GHT) or CE_LCTN[5:0] (71M6543HT) specifies a base address at a 1KB address boundary. Thus, the base address for the Info Page is at 1024 x CE_LCTN[6:0] (71M6543GHT) or CE_LCTN[5:0] (71M6543HT). Table 12 provides a list of the available 71M6543HT and 71M6543GHT trim fuses and their corresponding offsets relative to the Info Page base address. After reading the desired Info Page information, the MPU must reset the INFO_PG bit.

The code below provides an example for reading Info Page fuse trims. In this code example, the address, px is a pointer to the MPU's code space. In assembly language, the Info Page data objects, which are read-only, must be accessed with the MOVC 8051 instruction.

In C, Info Page trim fuses must be fetched with a pointer of the correct width, depending whether an 8-bit or a 16-bit data object is to be fetched. The case statements in the code example below perform casts to obtain a pointer of the correct size for each object, as needed.

In assembly language, the MPU has to form 11-bit or 16-bit values from two separate 8-bit fetches, depending on the object being fetched.

The byte values containing less than 8 valid bits are LSB justified. For example Info Page offset 0x90 is an 8-bit object, whose three LSBs are bits [10:8] of the complete TEMP_85[10:0] 11-bit object. The Info Page data objects are 2's complement format and should be sign extended when read into a 16-bit data type (see case _TEMP85 in the code example).

```
#if HIGH_PRECISION_METER
int16_t read_trim (enum eTRIMSEL select) {
        uint8r_t *px;
        int16_t x;
        px = ((uint16_t)select) + ((uint8r_t *)(CE3 << 10));
        switch (select)
        {
        default:
        case _TRIMBGD:
                INFO_PG = 1;
                x = *px;
                INFO_PG = 0;
                break;
        case _TRIMBGB:
                INFO_PG = 1;
                x = *(uint16r_t*)px;
                INFO_PG = 0;
                break;
        case _TEMP85:
                INFO_PG = 1;
                x = *(uint16r_t*)px;
                INFO_PG = 0;
                if (x & 0x800)
                        x |= 0xF800;
                break;
        }
        return (x);
}
#endif //#if HIGH_PRECISION_METER
```

Table 13: Info Page Trim Fuses

TRIM FUSE	OBJECT SIZE	ADDRESS OFFSET	COMMENTS
TEMP_85[10:8] TEMP_85[7:0] (11 bits)	8 bits 8 bits	0x90 0x91	TEMP_85[10:0] holds the STEMP[10:0] reading at +85NC. 2's complement format
TRIMBGB[15:8] TRIMBGB[7:0] (16 bits)	8 bits 8 bits	0x92 0x93	TRIMBGB[15:0] holds the deviation of VREF from its ideal value (1.195V) at +85NC. LSB = 0.1 mV 2's complement format
TRIMBGD[7:0] (8 bits)	8 bits	0x94	TRIMBGD[7:0] holds the deviation of VREF from its ideal value (1.195V) at +22NC. LSB = 0.1 mV 2's complement format
LCDADJ12[7:0] (8 bits)	8 bits	0x95	LCDADJ12 = [VLCD-3.676v] at 22C when LCD_DAC = 0C. LSB = 5mV. Two's complement.
LCDADJ0[7:0] (8 bits)	8 bits	0x96	LCDADJ0 = [VLCD-2.65v] at 22C when LCD_DAC = 0. LSB = 5mV. Two's complement.

Table 14. Trim Fuse Bit Mapping

OFFSET	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x90	TEMP_85[10:0]						TEMP_85[10:8]		
0x91		TEMP_85[7:0]							
0x92	TRIMBGB[15:0]	TRIMBGB[15:8]							
0x93		TRIMBGB[7:0]							
0x94	TRIMBGD[7:0]	TRIMBGD[7:0]							

CE Interface Description

CE Program

The CE performs the precision computations necessary to accurately measure energy. These computations include offset cancellation, phase compensation, product smoothing, product summation, frequency detection, VAR calculation, sag detection and voltage phase measurement.

The CE program is supplied by Maxim Integrated as a data image that can be merged with the MPU operational code for meter applications. Typically, the CE program provided with the demonstration code covers most applications and does not need to be modified. Other variations of CE code are available. Contact your local Maxim Integrated representative to obtain the appropriate CE code required for a specific application.

CE Data Format

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement format

(-1 = 0xFFFFFFFF). Calibration parameters are defined in flash memory (or external EEPROM) and must be copied to CE data memory by the MPU before enabling the CE. Internal variables are used in internal CE calculations. Input variables allow the MPU to control the behavior of the CE code. Output variables are outputs of the CE calculations. The corresponding MPU address for the most significant byte is given by 0x0000 + 4 x CE_address and by 0x0003 + 4 x CE_address for the least significant byte.

Constants

- Sampling Frequency: 2520.62Hz.
- F_0: Frequency of the mains phases (typically 50Hz or 60Hz).
- IMAX: RMS current corresponding to 250mV peak (176.8 mVRMS) at the inputs IA and IB. IMAX needs to be adjusted if the preamplifier is activated for the IAP-IAN inputs. For a 250µΩ shunt resistor, IMAX becomes 707A (176.8 mVRMS/250FI = 707.2ARMS).
- VMAX: RMS voltage corresponding to 250mV peak at the VA and VB inputs.
- N_{ACC}: Accumulation count for energy measurements is SUM_SAMPS[12:0]. The duration of the accumulation interval for energy measurements is SUM_SAMPS[12:0]/F_S.
- X: Gain constant of the pulse generators. Its value is determined by PULSE_FAST and PULSE_SLOW.
- Voltage LSB (for sag threshold) = VMAX x 7.8798 x10^{-9} V.

The system constants IMAX and VMAX are used by the MPU to convert internal digital quantities (as used by the CE) to external, i.e., metering quantities. Their values are determined by the scaling of the voltage and current sensors used in an actual meter.

Environment

Before starting the CE using the CE_E bit (I/O RAM 0x2106[0]), the MPU has to establish the proper environment for the CE by implementing the following steps:

- Locate the CE code in flash memory using CE_LCTN[6:0] (71M6543GT/GHT or CE_LCTN[5:0] (71M6543FT/HT).
- Load the CE data into RAM.
- Establish the equation to be applied in EQU[2:0].
- Establish the number of samples per accumulation period in SUM_SAMPS[12:0].
- Establish the number of cycles per ADC multiplexer frame (MUX_DIV[3:0]).
- Apply proper values to MUXn_SEL, as well as proper selections for DIFFn_E and RMT_E in order to configure the analog inputs.
- Initialize any MPU interrupts, such as CE_BUSY, XFER_BUSY, or the power failure detection interrupt.
- VMAX = 600V, IMAX = 707A, and kH = 1Wh/pulse are assumed as default settings

When different CE codes are used, a different set of environment parameters need to be established. The exact values for these parameters are listed in the Application Notes and other documentation which accompanies the CE code.

The CE details described in this data sheet should be considered typical and may not, in aggregate, be indicative of any particular CE code. Contact your Maxim Integrated representative for details about available standard CE codes.

CE Calculations

The MPU selects the basic configuration for the CE by setting the EQU variable.

CE Input Data

Data from the AFE is placed into CE memory by hardware at ADC0-ADC10. Table 15 describes the process.

Table 15. Power Equations

EQU[2:0]	WATT AND VAR FORMULA (*WSUM/VARSUM*)	W0SUM/ VAR0SUM	W1SUM/ VAR1SUM	W2SUM/ VAR2SUM	I0SQ SUM	I1SQ SUM	I2SQ SUM
3	VA x (IA-IB/2) + VC x IC (2 element 4W 3ϕ Delta)	VA x (IA-IB)/2	—	VC x IC	IA-IB	IB	IC
4	VA x (IA-IB)/2 + VB(IC-IB)/2 (2 element 4W 3ϕ Wye)	VA x (IA-IB)/2	VB x (IC-IB)	—	IA-IB	IC-IB	IC
5	VA x IA+VB x IB + VC x IC (3 element 4W 3ϕ Wye)	VA x IA	VB x IB	VC x IC	IA	IB	IC

Table 16. CE Raw Data Access Locations

PIN	MUXn_SEL HANDLE				CE RAM LOCATION			
	DIFF0_E				DIFF0_E			
	0	1			0	1		
IADC0	0	0			0	0		
IADC1	1				1			
	RMT2_E, DIFF2_E				RMT2_E, DIFF2_E			
	0,0	0,1	1,0	1,1	0,0	0,1	1,0	1,1
IADC2	2	2	-	-	2	2	2*	2*
IADC3	3				3			
	RMT4_E, DIFF4_E				RMT4_E, DIFF4_E			
	0,0	0,1	1,0	1,1	0,0	0,1	1,0	1,1
IADC4	4	4	-	-	4	4	4*	4*
IADC5	5				5			
	RMT6_E, DIFF6_E				RMT6_E, DIFF6_E			
	0,0	0,1	1,0	1,1	0,0	0,1	1,0	1,1
IADC6	6	6	-	-	6	6	6*	6*
IADC7	7				7			
	There are no configuration bits for VADC8, 9, 10							
VADC8 (VA)	8				8			
VADC9 (VB)	9				9			
VADC10 (VC)	10				10			

**Remote interface data.*

Table 17. CE Status Register

CESTATUS BIT	NAME	DESCRIPTION
31:4	Not used	These unused bits are always zero.
3	F0	F0 is a square wave at the exact fundamental input frequency.
2	SAG_C	Normally zero. Becomes one when VB remains below SAG_THR for SAG_CNT samples. Does not return to zero until VB rises above SAG_THR.
1	SAG_B	Normally zero. Becomes one when VB remains below SAG_THR for SAG_CNT samples. Does not return to zero until VB rises above SAG_THR.
0	SAG_A	Normally zero. Becomes one when VA remains below SAG_THR for SAG_CNT samples. Does not return to zero until VA rises above SAG_THR.

CE Status and Control

The CESTATUS register (0x80) contains bits that reflect the status of the signals that are applied to the CE. CECONFIG (0x20) contains bits that control basic operation of the compute engine.

The CE code supports registers to establish the sag threshold and gain for each of the input channels. When the input RMS voltage level falls below an established level, a warning is posted to the MPU. This level is called the sag threshold, and it is set in the SAG_THR register.

Gain for each channel is adjusted in the GAIN_ADJ0 (voltage), GAIN_ADJ1 (current channel A) and GAIN_ADJ2 (current channel B).

Transfer Variables

After each pass through CE program code, the CE asserts a XFER_BUSY interrupt. This informs the MPU that new data is available. It is the responsibility of MPU code to retrieve the data from the CE in a timely manner.

Table 18. CE Configuration Register

CECONFIG BIT	NAME	DEFAULT	DESCRIPTION		
22	EXT_TEMP	0	When 1, the MPU controls temperature compensation via the GAIN_ADJn registers (CE RAM 0x40-0x42), when 0, the CE is in control.		
21	EDGE_INT	1	When 1, XPULSE produces a pulse for each zero-crossing of the mains phase selected by FREQSEL[1:0] , which can be used to interrupt the MPU.		
20	SAG_INT	1	When 1, activates YPULSE output when a sag condition is detected.		
19:8	SAG_CNT	252 (0xFC)	The number of consecutive voltage samples below SAG_THR (CE RAM 0x24) before a sag alarm is declared. The default value is equivalent to 100 ms.		
7:6	FREQSEL[1:0]	0	FREQSEL[1:0] selects the phase to be used for the frequency monitor, sag detection, and for the zero crossing counter (MAINEDGE_X).		
			FREQ SEL[1:0]		**PHASE SELECTED**
			0	0	A
			0	1	B*
			1	X	Not allowed
5	EXT_PULSE	1	When zero, causes the pulse generators to respond to internal data (WPULSE = WSUM_X, VPULSE = VARSUM_X). Otherwise, the generators respond to values the MPU places in APULSEW and APULSER.		
4:2	Reserved	0	Reserved.		
1	PULSE_FAST	0	When PULSE_FAST = 1, the pulse generator input is increased 16x. When PULSE_SLOW = 1, the pulse generator input is reduced by a factor of 64. These two parameters control the pulse gain factor X (see table below). Allowed values are either 1 or 0. Default is 0 for both (X = 6).		
0	PULSE_SLOW	0	**PULSE_FAST**	**PULSE_SLOW**	**X**
			0	0	$1.5 \times 2^2 = 6$
			1	0	$1.5 \times 2^6 = 96$
			0	1	$1.5 \times 2^{-4} = 0.09375$
			1	1	Do not use

Table 19. Sag Threshold and Gain Adjustment Registers

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x24	SAG_THR	2.39 x 10^7	The voltage threshold for sag warnings. The default value is equivalent to 113V peak or 80 VRMS if VMAX = 600VRMS. $SAG\_THR = \frac{V_{RMS} \cdot \sqrt{2}}{VMAX \cdot 7.8798 \cdot 10^{-9}}$
0x40	GAIN_ADJ0	16384	This register scales the voltage measurement channels VADC8 (VA), VADC9 (VB) AND VADC10 (VC). The default value of 16384 is equivalent to unity gain (1.000).
0x41	GAIN_ADJ1	16384	This register scales the IADC0-IADC1 current channel for neutral current. The default value of 16384 is equivalent to unity gain (1.000).
0x42	GAIN_ADJ2	16384	This register scales the IA current channel for Phase A. The default value of 16384 is equivalent to unity gain (1.000).
0x43	GAIN_ADJ3	16384	This register scales the IB current channel for Phase B. The default value of 16384 is equivalent to unity gain (1.000).
0x44	GAIN_ADJ4	16384	This register scales the IC current channel for Phase C. The default value of 16384 is equivalent to unity gain (1.000).

Table 20. CE Transfer Registers

CE ADDRESS	NAME	DESCRIPTION
0x84†	WSUM_X	The signed sum: W0SUM_X+W1SUM_X. Not used for EQU[2:0] = 0 and EQU[2:0] = 1.
0x85	W0SUM_X	The sum of Wh samples from each wattmeter element. LSB = 9.4045 x 10^{-13} x VMAX x IMAX Wh (local) LSB = 1.55124 x 10^{-12} x VMAX x IMAX Wh (remote)
0x86	W1SUM_X	
0x87	W2SUM_X	
0x88†	VARSUM_X	The signed sum: VAR0SUM_X+VAR1SUM_X. Not used for EQU[2:0] = 0 and EQU[2:0] = 1.
0x89	VAR0SUM_X	The sum of VARh samples from each wattmeter element. LSB = 9.4045 x 10^{-13} x VMAX x IMAX VARh (local) LSB = 1.55124 x 10^{-12} x VMAX x IMAX VARh (remote)
0x8A	VAR1SUM_X	
0x8B	VAR2SUM_X	
0x8C	I0SQSUM_X	The sum of squared current samples from each element. LSB = 9.9045 x 10^{-13} IMAX2 A^2h (local) LSB = 2.55872 x 10^{-12} x IMAX2 A^2h (remote)
0x8D	I1SQSUM_X	
0x8E	I2SQSUM_X	
0x8F	I3SQSUM_X	
0x90	V0SQSUM_X	The sum of squared voltage samples from each element. LSB= 9.4045 x 10^{-13} VMAX2 V^2h (local) LSB= 9.40448 x 10^{-13} x VMAX2 V^2h (remote)
0x91	V1SQSUM_X	
0x92	V2SQSUM_X	
0x82	FREQ_X	Fundamental frequency: $LSB \equiv \frac{2520.6Hz}{2^{32}} \approx 0.509 \cdot 10^{-6}$ Hz (for Local) $LSB \equiv \frac{2520.6Hz}{2^{32}} \approx 0.587 \cdot 10^{-6}$ Hz (for Remote)
0x83	MAINEDGE_X	The number of edge crossings of the selected voltage in the previous accumulation interval. Edge crossings are either direction and are debounced.

Pulse Generation

WRATE (CE RAM 0x21) along with the PULSE_SLOW and PULSE_FAST bits control the number of pulses that are generated per measured Wh and VARh quantities. The pulse rate is proportional to the WRATE value for a given energy. The meter constant Kh is derived from WRATE as the amount of energy measured for each pulse. That is, if Kh = 1Wh/pulse, a power applied to the meter of 120 V and 30 A results in one pulse per second; if the load is 240 V at 150 A, ten pulses per second are generated.

Normally, the CE takes the values from W0SUM_X and VAR0SUM_X and moves them to APULSEW and APULSER, respectively. Then, pulse generation logic in the CE creates the actual pulses. However, the MPU can take direct control of the pulse generation process by setting EXT_PULSE = 1. In this case, the MPU sets the pulse rate by directly loading APULSEW and APULSER.

Note that since creep management is an MPU function, when the CE manages pulse output (EXT_PULSE = 0) creep management is disabled.

The maximum pulse rate is 3 x F_S = 7.56kHz.

The maximum time jitter is 1/6 of the multiplexer cycle period (nominally 67µs) and is independent of the number of pulses measured. Thus, if the pulse generator is monitored for one second, the peak jitter is 67ppm. After 10 seconds, the peak jitter is 6.7ppm. The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it simply outputs at its maximum rate without exhibiting any rollover characteristics. The actual pulse rate, using WSUM as an example, is:

$$RATE = \frac{WRATE \cdot WSUM \cdot F_S \cdot X}{2^{46}} Hz$$

where F_S = sampling frequency (2520.6 Hz), X = Pulse speed factor derived from the CE variables PULSE_SLOW and PULSE_FAST.

Table 21. CE Pulse Generation Parameters

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x21	WRATE	547	$Kh = \frac{VMAX \cdot IMAX \cdot K}{WRATE \cdot N_{ACC} \cdot X} \cdot Wh/pulse$ where: K = 66.1782 (Local Sensors) K = 109.1587 (Remote Sensor) N_{ACC} = *SUM_SAMPS[12:0]* (*CE RAM 0x23*) X is a factor determined by PULSE_FAST and PULSE_SLOW. See CECONFIG definition for more information The default value yields 1.0 Wh/pulse for VMAX = 600 V and IMAX = 208 A. The maximum value for WRATE is 32,768 (2^{15}).
0x22	KVAR	6444	Scale factor for VAR measurement.
0x23	SUM_SAMPS	2520	*SUM_SAMPS* (N_{ACC}).
0x45	APULSEW	0	Wh pulse (WPULSE) generator input to be updated by the MPU when using external pulse generation. The output pulse rate is: *APULSEW* * F_S * 2^{-32} * WRATE * X * 2^{-14}. This input is buffered and can be updated by the MPU during a conversion interval. The change takes effect at the beginning of the next interval.
0x46	WPULSE_CTR	0	WPULSE counter.
0x47	WPULSE_FRAC	0	Unsigned numerator, containing a fraction of a pulse. The value in this register always counts up towards the next pulse.
0x48	WSUM_ACCUM	0	Roll-over accumulator for WPULSE.
0x49	APULSER	0	VARh (VPULSE) pulse generator input.
0x4A	VPULSE_CTR	0	VPULSE counter.
0x4B	VPULSE_FRAC	0	Unsigned numerator, containing a fraction of a pulse. The value in this register always counts up towards the next pulse.
0x4C	VSUM_ACCUM	0	Roll-over accumulator for VPULSE.

Table 22. Other CE Parameters

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x25	QUANT_VA	0	Compensation factors for truncation and noise in voltage, current, real energy and reactive energy for phase A.
0x26	QUANT_IA	0	
0x27	QUANT_A	0	
0x28	QUANT_VARA	0	
0x29 †	QUANT_VB	0	Compensation factors for truncation and noise in voltage, current, real energy and reactive energy for phase B.
0x2A	QUANT_IB	0	
0x2B	QUANT_B	0	
0x2C	QUANT_VARB	0	
0x2D	QUANT_VC	0	Compensation factors for truncation and noise in voltage, current, real energy and reactive energy for phase C.
0x2E	QUANT_IC	0	
0x2F	QUANT_C	0	
0x30	QUANT_VARC	0	
0x38	0x43453431		CE file name identifier in ASCII format (CE41a01f). These values are overwritten as soon as the CE starts
0x39	0x6130316B		
0x3A	0x00000000		

LSB weights for use with Local Sensors:

$QUANT\_Ix\_LSB = 5.08656 \cdot 10^{-13} \cdot IMAX^2$ (Amps^2)

$QUANT\_Wx\_LSB = 1.04173 \cdot 10^{-9} \cdot VMAX \cdot IMAX$ (Watts)

$QUANT\_VARx\_LSB = 1.04173 \cdot 10^{-9} \cdot VMAX \cdot IMAX$ (Vars)

LSB weights for use with the 71M6x03 isolated sensors:

$QUANT\_Ix\_LSB = 1.38392 \cdot 10^{-12} \cdot IMAX^2$ (Amps^2)

$QUANT\_Wx\_LSB = 1.71829 \cdot 10^{-9} \cdot VMAX \cdot IMAX$ (Watts)

$QUANT\_VARx\_LSB = 1.71829 \cdot 10^{-9} \cdot VMAX \cdot IMAX$ (Vars)

Table 23. CE Calibration Parameters

CE ADDRESS	NAME	DEFAULT	DESCRIPTION
0x10	CAL_IA	16384	These constants control the gain of their respective channels. The nominal value for each parameter is 2^{14} = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be increased by 1%. Refer to the 71M6x03 Demo Board User's Manual for the equations to calculate these calibration parameters.
0x11	CAL_VA	16384	
0x13	CAL_IB	16384	
0x14	CAL_VB	16384	
0x12	PHADJ_A	0	These constants control the CT phase compensation. Compensation does not occur when PHADJ_X = 0. As PHADJ_X is increased, more compensation (lag) is introduced. The range is P 215–1. If it is desired to delay the current by the angle Φ, the equations are: $PHADJ\_X = 2^{20}\frac{0.02229 \cdot \tan(\Phi)}{0.1487 - 0.0131 \cdot \tan(\Phi)}$ at 60Hz $PHADJ\_X = 2^{20}\frac{0.0155 \cdot \tan(\Phi)}{0.1241 - 0.009695 \cdot \tan(\Phi)}$ at 50Hz
0x15	PHADJ_B	0	
0x18	PHADJ_C	0	
0x12	L_COMP2_A	16384	The shunt delay compensation is obtained using the equation provided below: where: $L\_COMP2\_X = 16384 \times \frac{\sin(2\pi f/f_S) + \tan(\theta) \times [1 - \cos(2\pi f/f_S)]}{\sin(2\pi f/f_S) + \tan(\theta) \times \cos(2\pi f/f_S)}$ f_S = sampling frequency f = main frequency
0x15	L_COMP2_B	16384	
0x18	L_COMP2_C	16384	

CE Flow Diagrams

Figure 20, Figure 21, and Figure 22 show the data flow through the CE in simplified form. Functions not shown include delay compensation, sag detection, scaling, and the processing of meter equations.

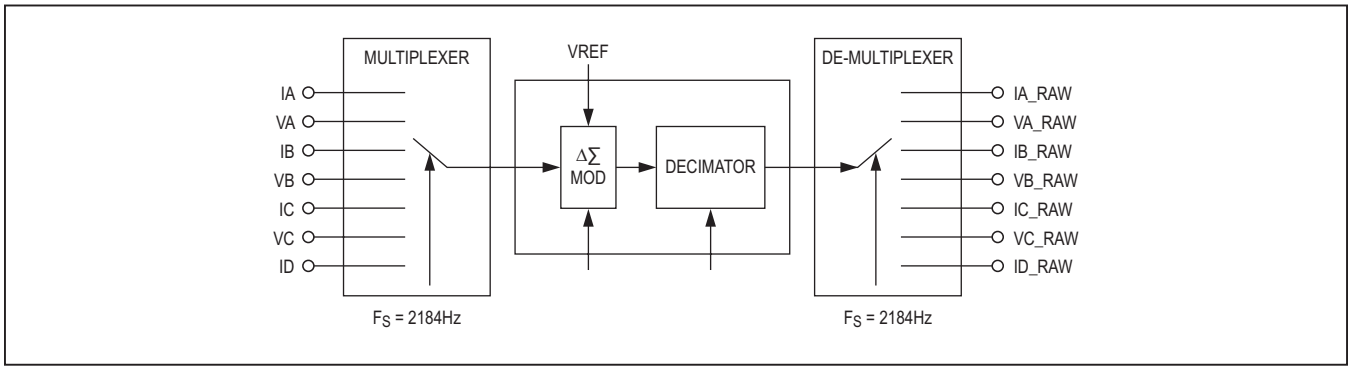


Figure 20. CE Data Flow—Multiplexer and ADC

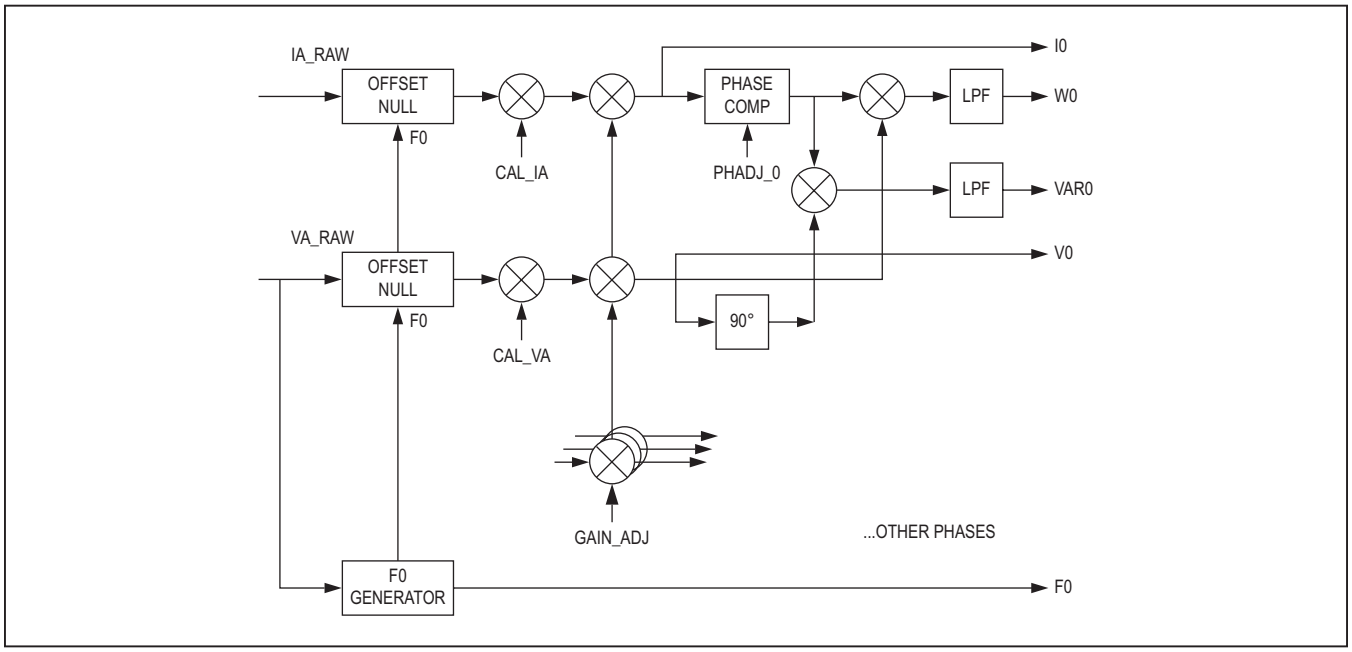


Figure 21. CE Data Flow—Offset, Gain, and Phase Compensation

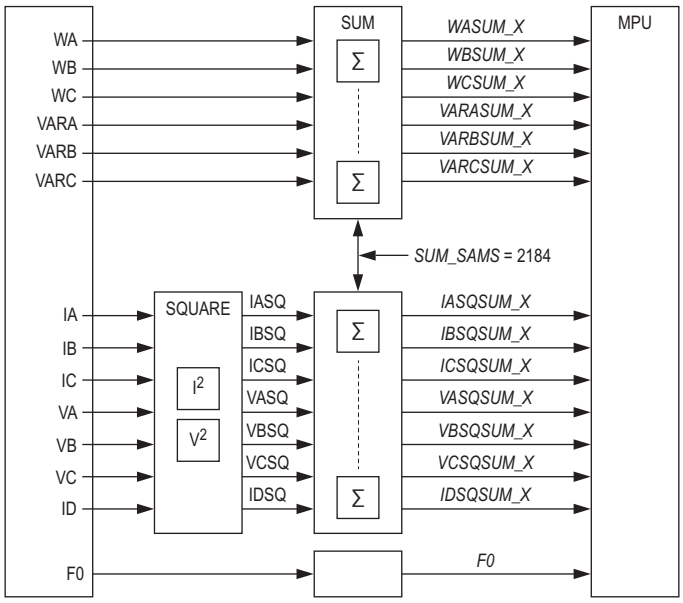


Figure 22. CE Data Flow—Squaring and Summation

Ordering Information

PART	TEMP RANGE	ACCURACY (TYP, %)	FLASH (KB)	PIN-PACKAGE
71M6543FT-IGT/F	-40°C to +85°C	0.1	64	100 LQFP
71M6543FT-IGTR/F	-40°C to +85°C	0.1	64	100 LQFP
71M6543HT-IGT/F	-40°C to +85°C	0.1	64	100 LQFP
71M6543HT-IGTR/F	-40°C to +85°C	0.1	64	100 LQFP
71M6543GT-IGT/F	-40°C to +85°C	0.1	128	100 LQFP
71M6543GT-IGTR/F	-40°C to +85°C	0.1	128	100 LQFP
71M6543GHT-IGT/F	-40°C to +85°C	0.1	128	100 LQFP
71M6543GHT-IGTR/F	-40°C to +85°C	0.1	128	100 LQFP

F = Lead(Pb)-free/RoHS-compliant package.

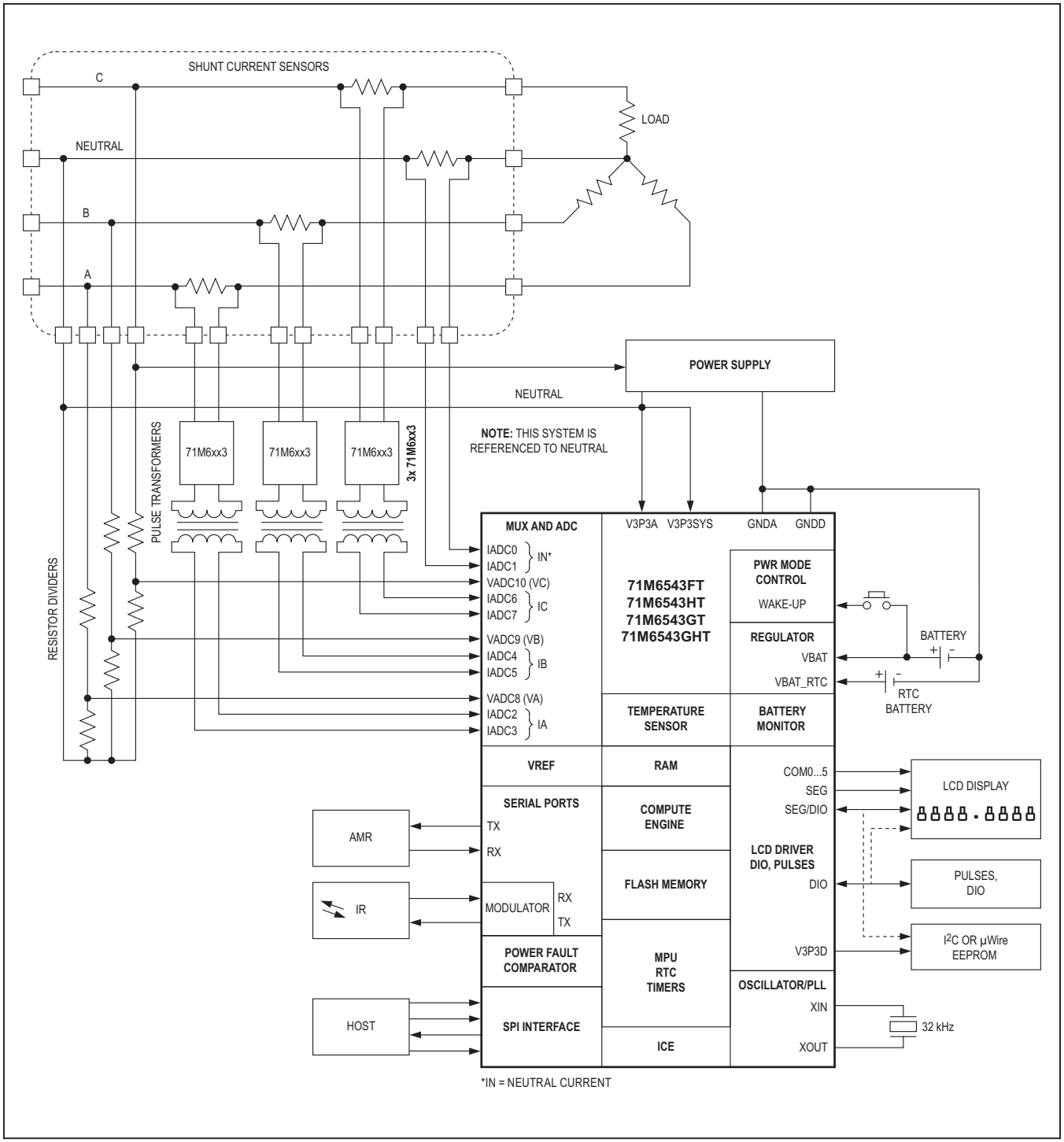
R = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
100 LQFP	C100L+8	**21-0684**	**90-0295**

Typical Operating Circuit



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/13	Initial release	—
1	8/13	Added description and specifications for 71M6543GT and 71M6543GHT devices, added note in *SPI Flash Mode* section about code updates, corrected part numbers listed in the *Reading the Info Page* section and in the figures, updated Table 12 for the external interrupts, changed the single-ended inputs from four to two, updated the description of TEMP_START and TEMP_PER in Table 12, updated Table 12 with definitions for STEMP_T22_P, STEMP_T85_P, T22_P, T85_P and UMUX_SEL, updated CHIP_ID description in Table 12, added description for the *UART* section	1–69
2	10/13	Removed pins 63–66 as N.C. (no connection) in the *Pin Descriptions* table	16
3	10/13	Removed “future product” status on 71M6543HT in the *Ordering Information* table, updated the V_{REF} Error specification in the *Electrical Characteristics*	10, 70
4	12/13	Updated the CXL and CXS capacitor values from 10pF and 15pF to 22pF	12, 14
5	2/14	Updated the V_{REF} coefficients in the *Electrical Characteristics* table; removed Note 2 from the EC notes; changed CXS and CXL notes in the *Recommended External Components* table; removed future status from 71M6543GHT in the *Ordering Information* table	8, 10, 12, 70
6	1/15	Updated the *Benefits and Features* section	1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim’s website at www.maximintegrated.com.

