FLASH MEMORY MT28F002C5

FEATURES

- Five erase blocks:
  - 16KB boot block (protected)
  - Two 8KB parameter blocks
  - Two main memory blocks (96KB and 128KB)
- Top boot block organization
- Address access time: 80ns
- Industry-standard pinouts
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- TSOP packaging

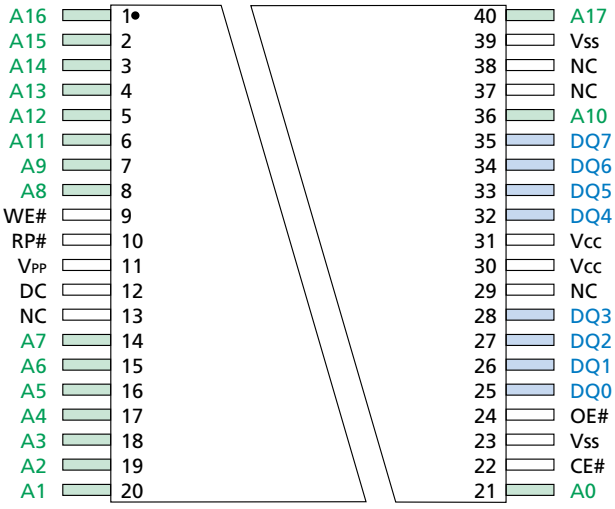
OPTIONS — MARKING

- Timing
  80ns access — -8
- Boot Block Starting Address
  Top — T
- Package
  Plastic 40-pin TSOP Type 1 (10mm x 20mm) VG

Part Number Example:
MT28F002C5VG-8 T

PIN ASSIGNMENT (Top View)

40-Pin TSOP Type I



GENERAL DESCRIPTION

The MT28F002C5 (x8) is a nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 2,097,152 bits. It is fabricated with Micron's advanced CMOS floating-gate process. Device operation and features of the MT28F002C5 are identical to the Smart 5 MT28F002B5, except the BIOS-optimized device is specified to operate at 5V V_{CC} and 12V V_{PP}, and it is available in a top boot configuration only. Due to process technology advances, 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 100 cumulative hours. For any operation, V_{CC} may be at 5V. In addition, the WP# pin is a "Don't Care." For further information on device operation or features, refer to the MT28F002B5 data sheet.

System designers can easily accommodate multiple types of boot block flash by connecting the DC pin ("Don't Care") to V_{SS}. By doing this, a Micron Smart 5 device or the BIOS-optimized device can be used in the same socket without any further hardware or software changes.

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest data sheet.

PIN DESCRIPTIONS

TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
9	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
12	DC	Input	Don't Care: This pin can be left floating, can be tied to a control pin or can be tied to V_{SS} or V_{CC} ($\pm$10µA input leakage). It should be tied to V_{SS} to allow for compatibility with 2Mb Smart 5 boot block flash.
22	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
10	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are "Don't Care," and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V); RP# must be held at V_{IH} during all other modes of operation.
24	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
21, 20, 19, 18, 17, 16, 15, 14, 8, 7, 36, 6, 5, 4, 3, 2, 1, 40	A0-A17	Input	Address Inputs: Select a unique location within the array.
25-28, 32-35	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
11	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH} (12V)[1]. V_{PP} is "Don't Care" during all other operations.
30, 31	V_{CC}	Supply	Power Supply: +5V $\pm$10%.
23, 39	V_{SS}	Supply	Ground.
13, 29, 37, 38	NC	–	No Connect: These pins may be driven or left unconnected.

NOTE: 1. For SmartVoltage-compatible production programming, 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 100 cumulative hours.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply
Relative to V_{SS} ..... -0.5V to +6V**
Input Voltage
Relative to V_{SS} ..... -0.5V to +6V**
V_{PP} Voltage Relative to V_{SS} ..... -0.5V to +12.6V†
RP# or A9 Pin Voltage
Relative to V_{SS} ..... -0.5V to +12.6V†
Temperature Under Bias ..... -10°C to +80°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**V_{CC} input and I/O pins may transition to -2V for <20ns and V_{CC} + 2V for <20ns.
†Voltage may pulse to -2V for <20ns and 14V for <20ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC READ OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2	V_{CC} + 0.5	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	1
Device Identification Voltage, A9	V_{ID}	11.4	12.6	V	1
V_{PP} Supply Voltage	V_{PP}	-0.5	12.6	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS (TTL) Output High Voltage (I_{OH} = -2.5mA)	V_{OH1}	2.4	–	V	1
Output Low Voltage (I_{OL} = 5.8mA)	V_{OL}	–	0.45	V	
OUTPUT VOLTAGE LEVELS (CMOS) Output High Voltage (I_{OH} = -100µA)	V_{OH2}	V_{CC} - 0.4	–	V	1
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); All other pins not under test = 0V	I_L	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 12.6 = V_{ID})	I_{ID}	–	500	µA	
INPUT LEAKAGE CURRENT: RP# INPUT (11.4V ≤ RP# ≤ 12.6 = V_{HH})	I_{HH}	–	500	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	

NOTE: 1. All voltages referenced to V_{SS}.

CAPACITANCE

(T_A = 25°C; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_I	8	pF	
Output Capacitance	C_O	12	pF	

READ AND STANDBY CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}; $\overline{RP}$ = V_{IH})	I_{CC1}	55	mA	1, 2
READ CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; $\overline{OE}$ ≥ V_{CC} - 0.2V; f = 10 MHz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; $\overline{RP}$ ≥ V_{CC} - 0.2V)	I_{CC2}	50	mA	1, 2
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RP}$ = V_{IH}; Other inputs = V_{IL} or V_{IH})	I_{CC3}	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RP}$ = V_{CC} - 0.2V)	I_{CC4}	130	µA	
DEEP POWER-DOWN CURRENT: V_{CC} SUPPLY ($\overline{RP}$ = V_{SS} ±0.2V)	I_{CC5}	20	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} > 5.5V)	I_{PP1}	50	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} ≤ 5.5V)	I_{PP2}	±10	µA	
DEEP POWER-DOWN CURRENT: V_{PP} SUPPLY ($\overline{RP}$ = V_{SS} ±0.2V)	I_{PP3}	5	µA	

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

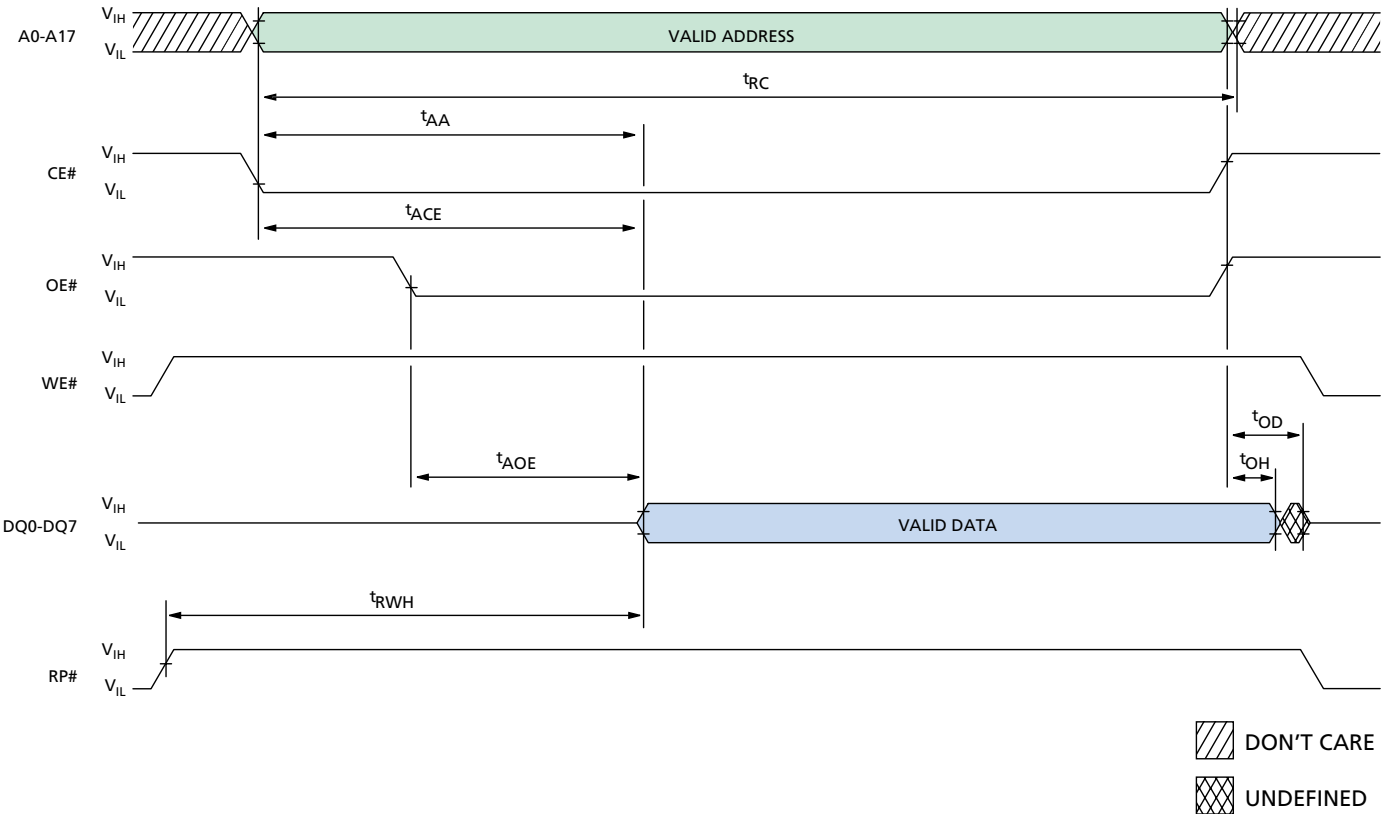
AC CHARACTERISTICS		-8			
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
READ cycle time	^tRC	80		ns	
Access time from $\overline{CE}$	^tACE		80	ns	3
Access time from $\overline{OE}$	^tAOE		40	ns	3
Access time from address	^tAA		80	ns	
$\overline{RP}$ HIGH to output valid delay	^tRWH		500	ns	
$\overline{OE}$ or $\overline{CE}$ HIGH to output in High-Z	^tOD		20	ns	
Output hold time from $\overline{OE}$, $\overline{CE}$ or address change	^tOH	0		ns	
$\overline{RP}$ LOW pulse width	^tRP	60		ns	

NOTE: 1. I_{CC} is dependent on cycle rates.
2. I_{CC} is dependent on output loading. Specified values are obtained with the outputs open.
3. $\overline{OE}$ may be delayed by ^tACE minus ^tAOE after $\overline{CE}$ falls before ^tACE is affected.

AC TEST CONDITIONS

Input pulse levels	0.4V to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8V and 2V
Output timing reference level	0.8V and 2V
Output load	1 TTL gate and C_L = 100pF

READ CYCLE



READ TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
t_{RC}	80		ns
t_{ACE}		80	ns
t_{AOE}		40	ns
t_{AA}		80	ns

SYMBOL	-8 MIN	-8 MAX	UNITS
t_{RWH}		500	ns
t_{OD}		20	ns
t_{OH}	0		ns

RECOMMENDED DC WRITE/ERASE CONDITIONS

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
V_{PP} WRITE/ERASE lockout voltage	V_{PPLK}	–	6.5	V	1
V_{PP} voltage during WRITE/ERASE operation	V_{PPH}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.4	12.6	V	
V_{CC} WRITE/ERASE lockout voltage	V_{LKO}	2	–	V	

WRITE/ERASE CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
BYTE WRITE CURRENT: V_{CC} SUPPLY	I_{CC8}	40	mA	
BYTE WRITE CURRENT: V_{PP} SUPPLY	I_{PP4}	25	mA	
ERASE CURRENT: V_{CC} SUPPLY	I_{CC9}	30	mA	
ERASE CURRENT: V_{PP} SUPPLY	I_{PP6}	40	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (ERASE suspended)	I_{CC10}	10	mA	2
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (ERASE suspended)	I_{PP7}	200	µA	

NOTE: 1. Absolute WRITE/ERASE protection when $V_{PP} \leq V_{PPLK}$.
2. Parameter is specified when device is not accessed. Actual current draw will be I_{CC10} plus read current if a READ is executed while the device is in erase suspend mode.

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: WE#-CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE cycle time	^tWC	80		ns	
WE# HIGH pulse width	^tWPH	30		ns	
CE# HIGH pulse width	^tCPH	30		ns	
CE# pulse width	^tCP	50		ns	
WE# pulse width	^tWP	50		ns	
Address setup time to WE# HIGH	^tAS	50		ns	
Address hold time from WE# HIGH	^tAH	0		ns	
Data setup time to WE# HIGH	^tDS	50		ns	
Data hold time from WE# HIGH	^tDH	0		ns	
CE# setup time to WE# LOW	^tCS	0		ns	
CE# hold time from WE# HIGH	^tCH	0		ns	
V_{PP} setup time to WE# HIGH	^tVPS	200		ns	
RP# HIGH to WE# LOW delay	^tRS	2		µs	
RP# at V_{HH} setup time to WE# HIGH	^tRHS	200		ns	1
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	2
Boot BLOCK ERASE duration	$^tWED2$	300		ms	1, 2
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	2
Main BLOCK ERASE duration	$^tWED4$	600		ms	2
WE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	3
V_{PP} hold time from status data valid	^tVPH	0		ns	2
RP# at V_{HH} hold time from status data valid	^tRHH	0		ns	1
Boot block relock delay time	^tREL		100	ns	4

NOTE: 1. RP# should be held at V_{HH} until boot block WRITE or ERASE is complete.
2. WRITE/ERASE times are measured to valid status register data (SR7 = 1).
3. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
4. ^tREL is required to relock boot block after WRITE or ERASE to boot block.

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: CE#-CONTROLLED WRITES

($0°C \le T_A \le +70°C$; $V_{CC} = +5V \pm 10\%$)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE cycle time	^tWC	80		ns	
WE# HIGH pulse width	^tWPH	30		ns	
CE# HIGH pulse width	^tCPH	30		ns	
CE# pulse width	^tCP	50		ns	
WE# pulse width	^tWP	50		ns	
Address setup time to CE# HIGH	^tAS	50		ns	
Address hold time from CE# HIGH	^tAH	0		ns	
Data setup time to CE# HIGH	^tDS	50		ns	
Data hold time from CE# HIGH	^tDH	0		ns	
WE# setup time to CE# LOW	^tWS	0		ns	
WE# hold time from CE# HIGH	^tWH	0		ns	
V_{PP} setup time to CE# HIGH	^tVPS	200		ns	
RP# HIGH to CE# LOW delay	^tRS	500		ns	
RP# at V_{HH} setup time to CE# HIGH	^tRHS	200		ns	1
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	2
Boot BLOCK ERASE duration	$^tWED2$	300		ms	1, 2
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	2
Main BLOCK ERASE duration	$^tWED4$	600		ms	2
CE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	3
V_{PP} hold time from status data valid	^tVPH	0		ns	2
RP# at V_{HH} hold time from status data valid	^tRHH	0		ns	1
Boot block relock delay time	^tREL		100	ns	4

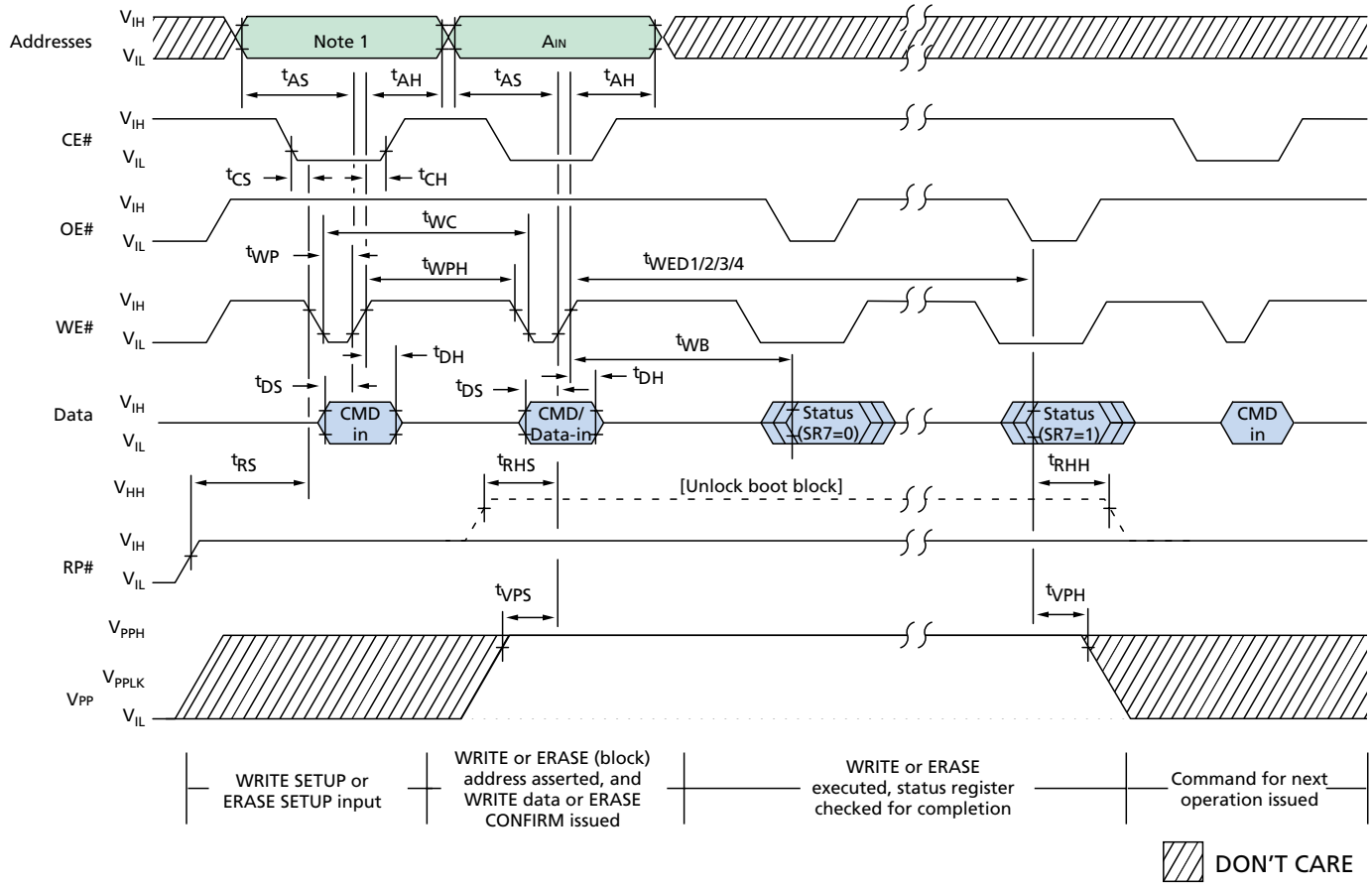
NOTE: 1. RP# should be held at V_{HH} until boot block WRITE or ERASE is complete.
2. WRITE/ERASE times are measured to valid status register data (SR7 = 1).
3. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
4. ^tREL is required to relock boot block after WRITE or ERASE to boot block.

WRITE AND ERASE DURATION CHARACTERISTICS

PARAMETER	TYP	MAX	UNITS	NOTES
Boot/parameter BLOCK ERASE time	0.5	7	s	1
Main BLOCK ERASE time	1.5	14	s	1
Main BLOCK WRITE time (byte mode)	1	–	s	1, 2, 3

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.
3. Typical WRITE times use checkerboard data pattern.

WRITE/ERASE CYCLE
WE#-CONTROLLED WRITE/ERASE



WRITE/ERASE TIMING PARAMETERS

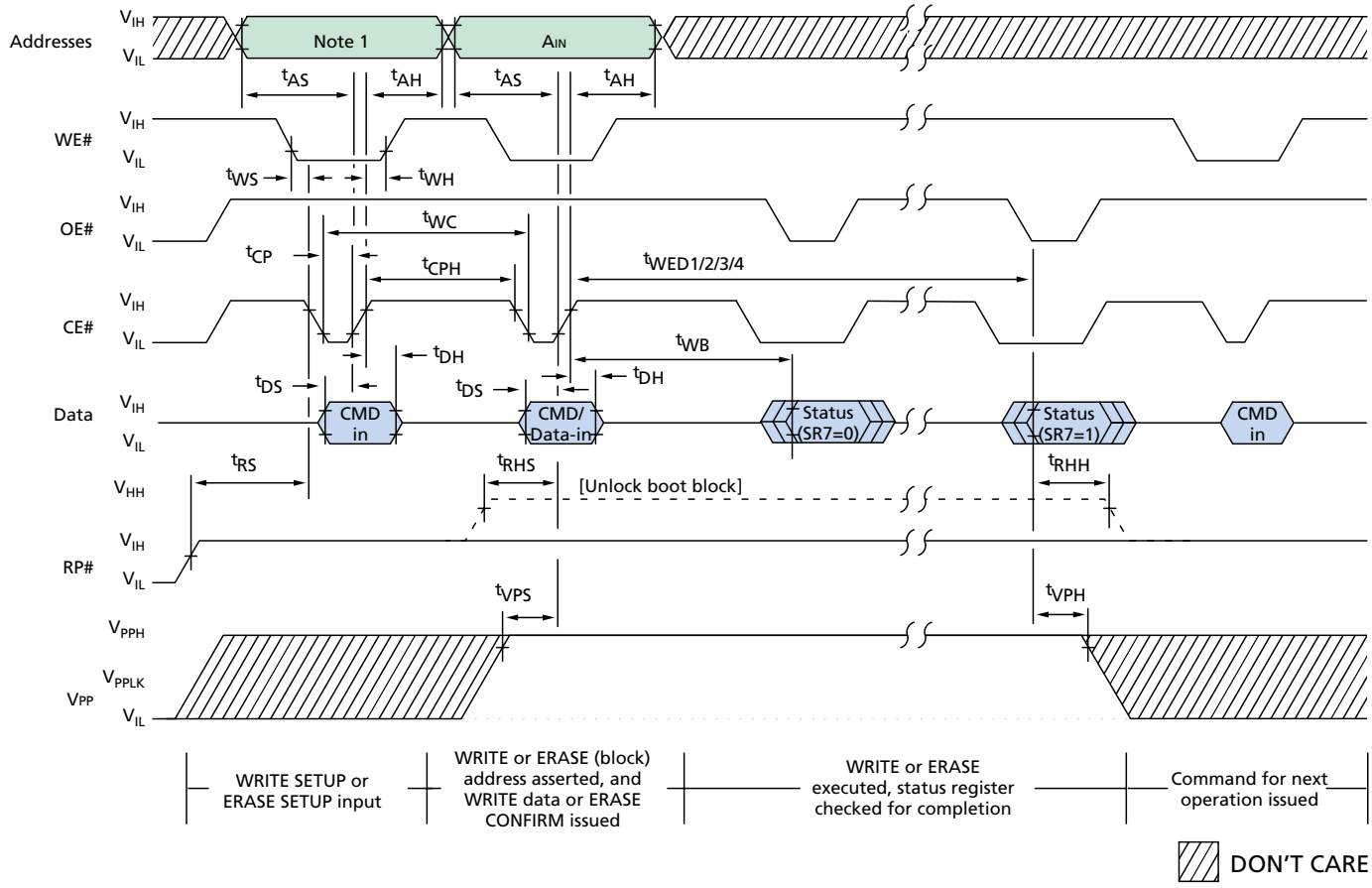
SYMBOL	-8 MIN	-8 MAX	UNITS
tWC	80		ns
tWPH	30		ns
tWP	50		ns
tAS	50		ns
tAH	0		ns
tDS	50		ns
tDH	0		ns
tCS	0		ns
tCH	0		ns
tVPS	200		ns

SYMBOL	-8 MIN	-8 MAX	UNITS
tRS	500		ns
tRHS	200		ns
tWED1	6		µs
tWED2	300		ms
tWED3	300		ms
tWED4	600		ms
tWB	200		ns
tVPH	0		ns
tRHH	0		ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.

WRITE/ERASE CYCLE

CE#-CONTROLLED WRITE/ERASE



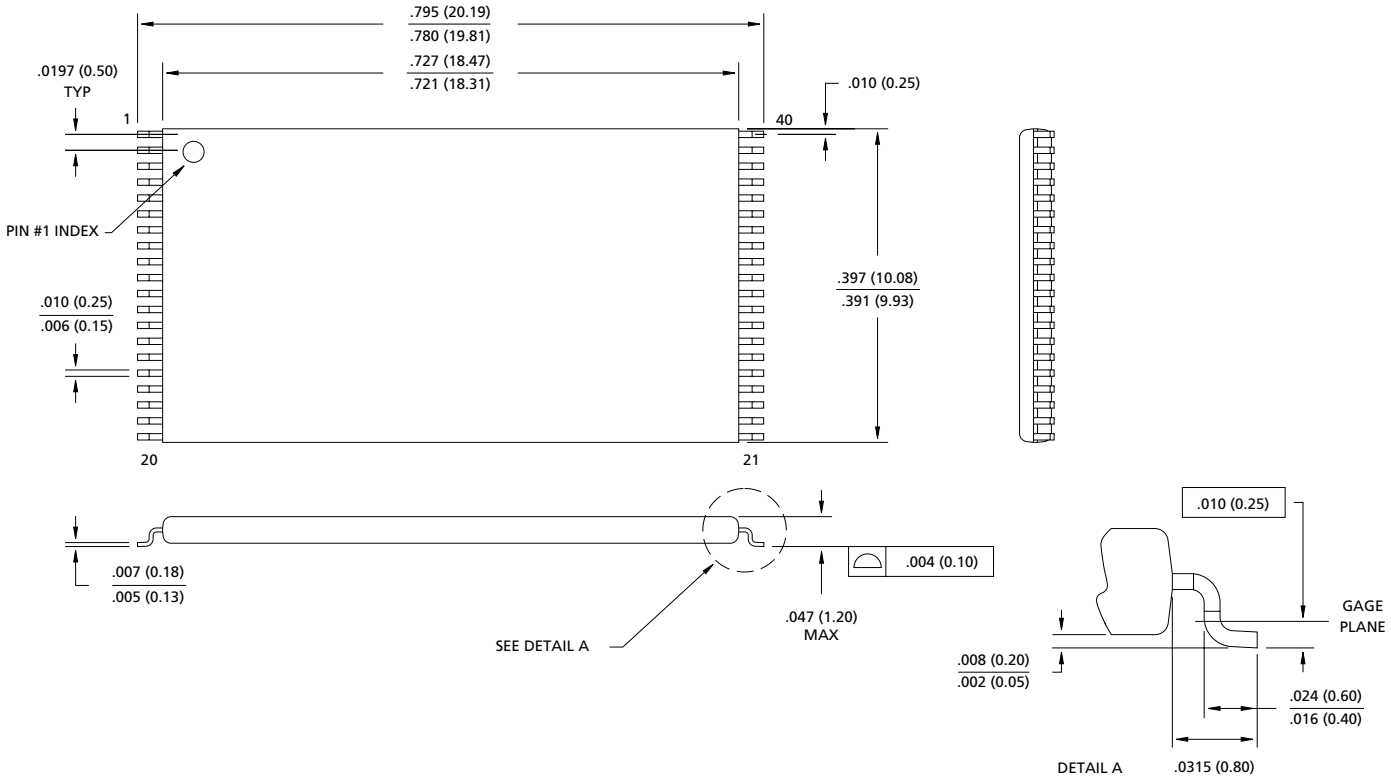
WRITE/ERASE TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
tWC	80		ns
tCPH	30		ns
tCP	50		ns
tAS	50		ns
tAH	0		ns
tDS	50		ns
tDH	0		ns
tWS	0		ns
tWH	0		ns
tVPS	200		ns

SYMBOL	-8 MIN	-8 MAX	UNITS
tRS	500		ns
tRHS	200		ns
tWED1	6		µs
tWED2	300		ms
tWED3	300		ms
tWED4	600		ms
tWB	200		ns
tVPH	0		ns
tRHH	0		ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.

40-PIN PLASTIC TSOP I
(10mm x 20mm)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01” per side.

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