

# M62320GP

## 8-bit I/O Expander for I<sup>2</sup>C BUS

REJ03D0909-0100

Rev.1.00

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### Description

The M62320GP is a CMOS 8-bit I/O expander, which has serial to parallel and parallel to serial data converting functions.

It can communicate with a microcontroller via few wiring thanks to the adoption of the two-line I<sup>2</sup>C BUS.

Parallel data I/O terminal can be set to input or output mode alternatively in individual bits.

Maximum 8 ICs can be connected to a bus by using three chip-select pins, so that it is possible to handle up to 64 bits data.

### Features

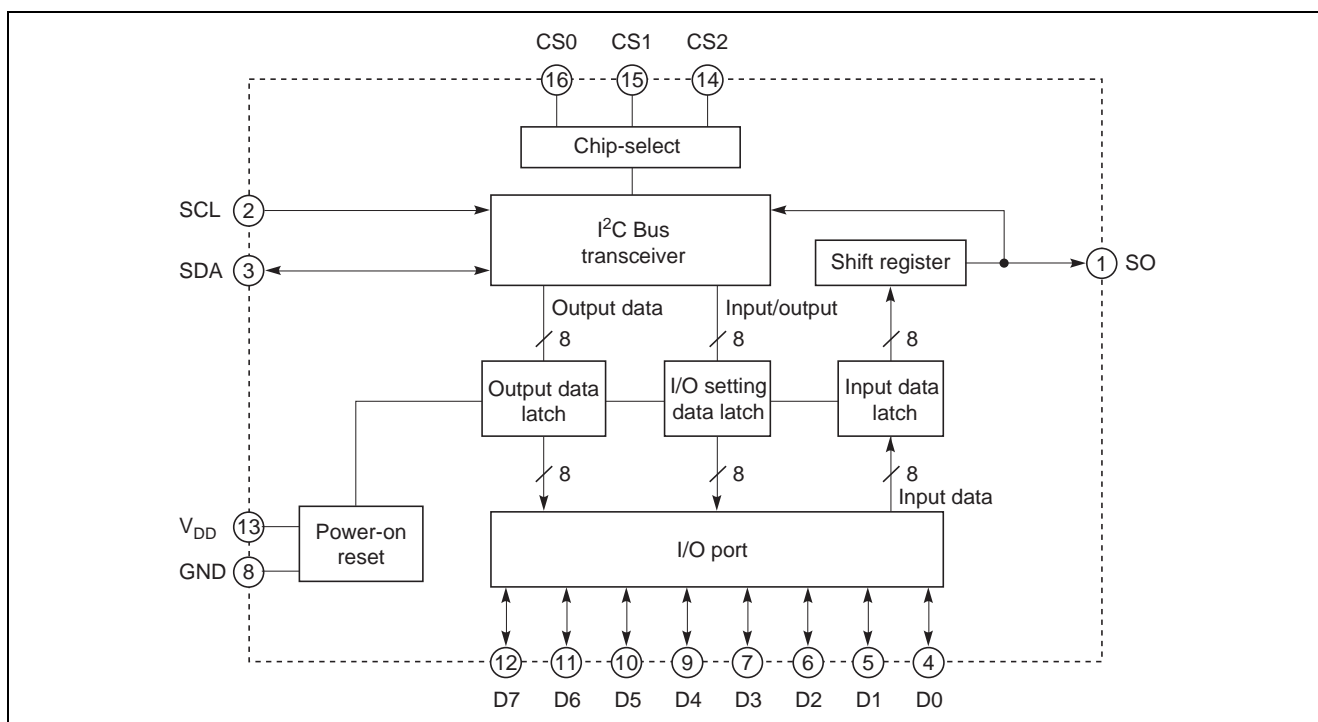
- Simple two-line (SCL and SDA) communication with a microcontroller.
- 8-bit data conversion between serial and parallel by I<sup>2</sup>C BUS.
- Built-in power-on reset.

### Application

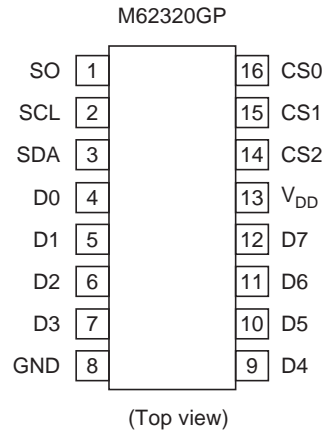
I/O port expansion for a microcontroller.

Data conversion between serial and parallel in microcontroller peripherals.

### Block Diagram



## Pin Arrangement



Outline: PRSP0016JA-A (16P2Z-A)

## Pin Description

Pin No.	Pin Name	I/O	Function
2	SCL	Input	Serial clock input
3	SDA	Input/Output	Serial data input/output
1	SO	Output	Serial data output
16	CS0	Input	Chip select data input
15	CS1		
14	CS2		
4	D0	Input/Output	Parallel data input/output
5	D1		
6	D2		
7	D3		
9	D4		
10	D5		
11	D6		
12	D7		
13	V <sub>DD</sub>	—	Power supply
8	GND	—	GND

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{DD}$	-0.3 to +7.0	V	
Input voltage	$V_I$	-0.3 to $V_{DD} + 0.3$	V	
Output voltage	$V_O$	-0.3 to $V_{DD} + 0.3$	V	
Output current "Low"	$I_{OH}$	-5 to 0	mA	D0 to D7
Output current "High"	$I_{OL}$	0 to 30	mA	D0 to D7
Power dissipation	$P_d$	761	mW	$T_a = 25^\circ\text{C}$
Operating temperature	$T_{opr}$	-20 to +85	$^\circ\text{C}$	
Storage temperature	$T_{stg}$	-40 to +125	$^\circ\text{C}$	

## Recommended Operating Conditions

- Supply voltage:  $V_{DD} = 3\text{V to } 5.5\text{ V}$
- Input high voltage:  $V_{IH} = 0.7 V_{DD} \text{ to } V_{DD}$
- Input low voltage:  $V_{IL} = 0 \text{ to } 0.2 V_{DD}$

## Electrical Characteristics

( $V_{DD} = 5\text{ V} \pm 10\%$ ,  $\text{GND} = 0\text{ V}$ ,  $T_a = -20 \text{ to } +85^\circ\text{C}$ , unless otherwise noted)

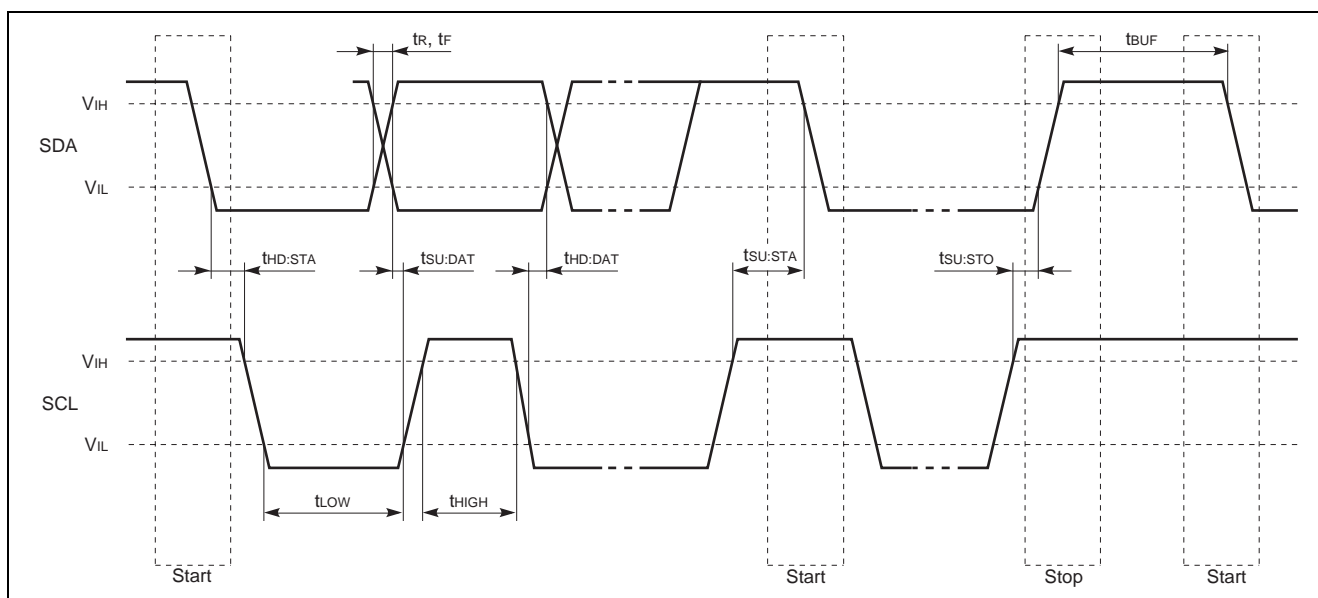
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Circuit current	$I_{DD}$	—	0.05	0.5	mA	$V_{IH} = V_{DD}$ , $V_{IL} = \text{GND}$ , $f_{SCL} = 400\text{ kHz}$
		—	0.1	1.0	$\mu\text{A}$	$V_{IH} = V_{DD}$ , $V_{IL} = \text{GND}$ , $f_{SCL} = \text{stop}$
Input leak current	$I_{ILK}$	-10	—	10	$\mu\text{A}$	
Output low voltage (SDA)	$V_{OL}$	—	—	0.4	V	$I_{\text{sink}} = 3\text{ mA}$
Input high voltage	$V_{IH}$	$0.7 V_{DD}$	—	$V_{DD}$	V	
Input low voltage	$V_{IL}$	—	—	$0.2 V_{DD}$	V	
Output high voltage (D0 to D7)	$V_{OH}$	$V_{DD} - 0.4$	—	$V_{DD}$	V	$I_{OH} = -1\text{ mA}$ , $V_{DD} = 5\text{ V}$
		$V_{DD} - 0.4$	—	$V_{DD}$		$I_{OH} = -500\text{ }\mu\text{A}$ , $V_{DD} = 3\text{ V}$
Output low voltage (D0 to D7)	$V_{OL}$	0	—	0.4	V	$I_{OL} = 5\text{ mA}$ , $V_{DD} = 5\text{ V}$
		0	—	0.4		$I_{OL} = 2.5\text{ mA}$ , $V_{DD} = 3\text{ V}$
Output current "Low" (D0 to D7)	$I_{OL}$	5	10	—	mA	$V_{OL} = 0.4\text{ V}$ , $V_{DD} = 5\text{ V}$
		2.5	5	—		$V_{OL} = 0.4\text{ V}$ , $V_{DD} = 3\text{ V}$
		15	25	—		$V_{OL} = 1.0\text{ V}$ , $V_{DD} = 5\text{ V}$
		5	10	—		$V_{OL} = 1.0\text{ V}$ , $V_{DD} = 3\text{ V}$

## I<sup>2</sup>C BUS Characteristics

Item	Symbol	Limits		Unit
		Min	Max	
SCL clock frequency	$f_{SCL}$	0	100	kHz
Free time: the bus must be free before a new transmission can start	$t_{BUF}$	4.7	—	$\mu s$
Hold time START Condition After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	—	$\mu s$
Low period of the clock	$t_{LOW}$	4.7	—	$\mu s$
High period of the clock	$t_{HIGH}$	4.0	—	$\mu s$
Set-up time for START condition Only relevant for a repeated START condition	$t_{SU:STA}$	4.7	—	$\mu s$
Data Hold time	$t_{HD:DAT}$	0	—	$\mu s$
Data Set-up time	$t_{SU:DAT}$	250	—	ns
Rise time of SDA and SCL signals	$t_R$	—	1000	ns
Fall time of SDA and SCL signals	$t_F$	—	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	—	$\mu s$

Note: Transmitter must internally provide at least a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

## Timing Chart



## Functional Blocks

### I<sup>2</sup>C BUS Interface

The I<sup>2</sup>C BUS interface recognizes start/stop conditions, a slave address and a write/read mode selection by receiving SDA, SCL, CS0, CS1 and CS2 signals and then the latch pulses, dedicated to each data latch are generated.

### Data Latch

This IC has 3 types of data latch: the I/O setting data latch, the input data latch and the output data latch and each latch is controlled by the I<sup>2</sup>C BUS interface.

- I/O setting data latch  
These latches set input- or output-state of each parallel data terminals (D0 to D7). They are set at the next byte after receiving the slave address byte in the write mode from the master. In case this latch is set to high, the data is transferred from the I<sup>2</sup>C BUS interface to the parallel data terminals. In the opposite transmission: from the parallel data terminals to the I<sup>2</sup>C BUS, it is set to low.
- Output data latch  
In the write mode, the data from the I<sup>2</sup>C BUS to the parallel data terminals is latched. When the master transmits output data after a setting in write mode, the output data is taken into the latches.
- Input data latch  
In the read mode, the data of parallel data terminals is latched in the input data latches. The input data is taken into the latches from the parallel data terminals on every 8th negative edge of SCL clock. The latched data is output to the master through the sift resistor. On the output terminal assigned by the I/O setting latch, the input data latch takes the state of the output terminal.

### Parallel Input/Output Port

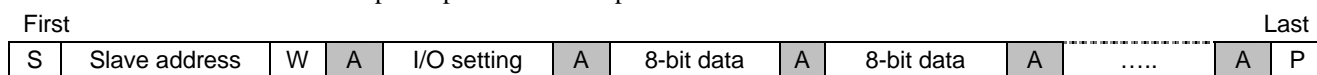
In case I/O setting latch is set to low (the input mode), each parallel terminal becomes hi-impedance and is able to accept an input. In another case I/O setting latch is set to high (output mode), each parallel terminal output a data according to the state of the output data latch.

### Power on Reset

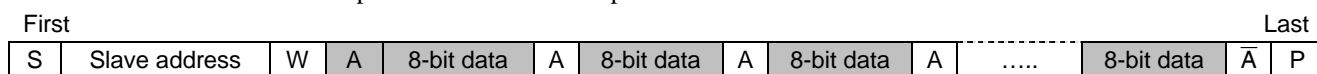
When power is turned on, each latch is reset and then the parallel data I/O terminals become hi-impedance (input mode).

## Digital Data Format

### 1. Write mode: I<sup>2</sup>C BUS data input to parallel data output



### 2. Read mode: Parallel data input to I<sup>2</sup>C BUS data output



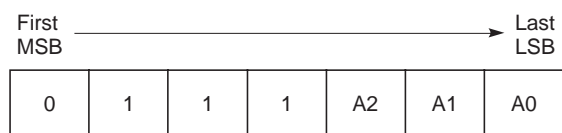
 Transmission from Master (MCU etc.) to Slave (M62320GP)

 Transmission from Slave (M62320GP) to Master (MCU etc.)

- S: Start condition

While SCL level is high, SDA line level should be changed from high to low.

- Slave address



Note: Lower three bits (A0, A1, A2) are a programmable address. This IC is accessed only when the lower 3 bits data of slave address coincide with the data of CS0 to CS2. (refer to the right table)

#### Chip select data

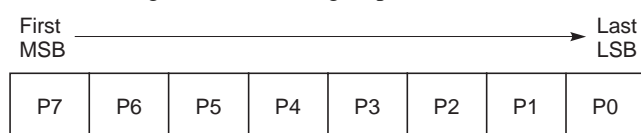
MSB			LSB		
A2	A1	A0	CS2	CS1	CS0
0	0	0	L	L	L
0	0	1	L	L	H
0	1	0	L	H	L
:	:	:	:	:	:
1	1	1	H	H	H

Note: L = Low, H = High

- W: Write (SDA = Low), R: Read (SDA = High)

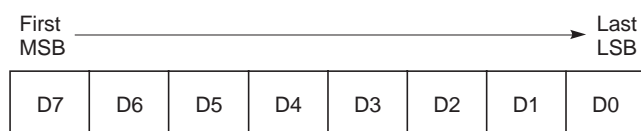
- A: Acknowledge bit

- I/O setting data (I/O setting of parallel data I/O terminals.)



Note: DATA INPUT from parallel data terminals = Low  
 DATA OUTPUT to parallel data terminals = High  
 Each bit data corresponds to the I/O state of the parallel data terminals.

- 8-bit data



- P: Stop condition

While SCL level is high, SDA level should be changed from low to high.

## Functional Description

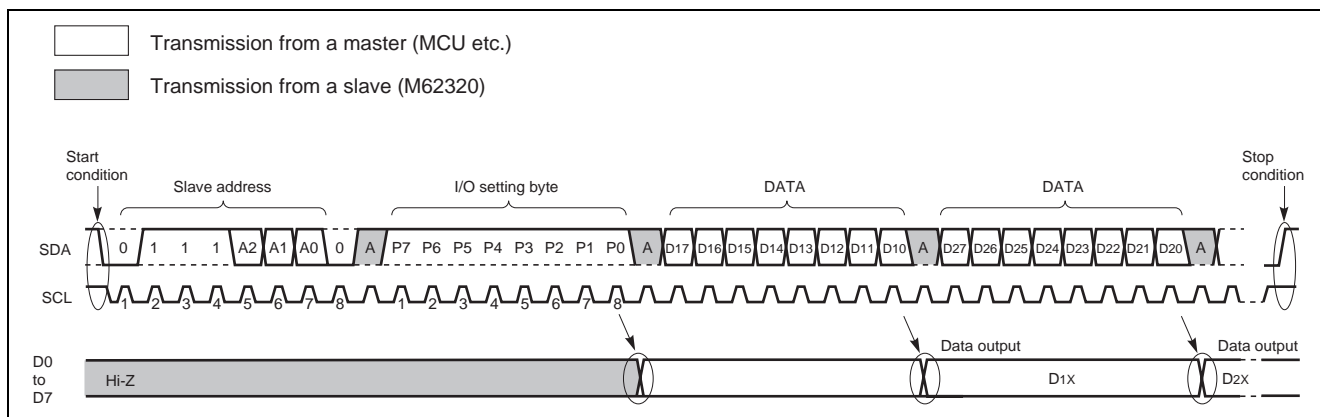
All parallel data I/O terminals are set to the input-state after power-on. In case any terminals need to be set to the output state, the corresponding terminals should be set during the write mode. This setting is hold until a next setting.

In the write mode, 8 bits data can be transmitted from the I<sup>2</sup>C BUS interface to the parallel ports continually after the slave address and I/O setting.

In the read mode, 8 bits data can be transmitted from the parallel ports to the I<sup>2</sup>C BUS interface continually after the slave address setting.

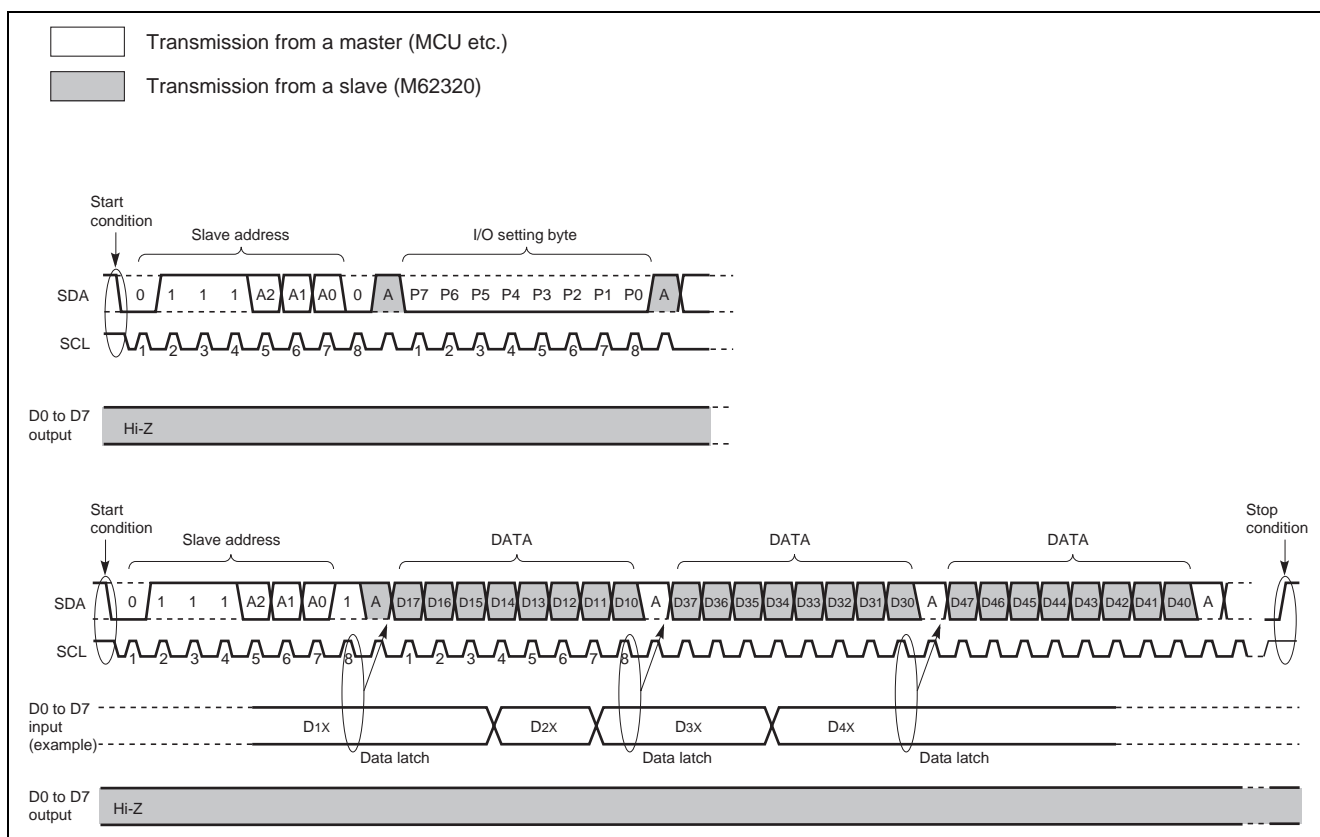
In the case of a changing between the write-and read-mode, the data must be transmitted again from the starting condition.

- In a case of a data conversion from serial to parallel.



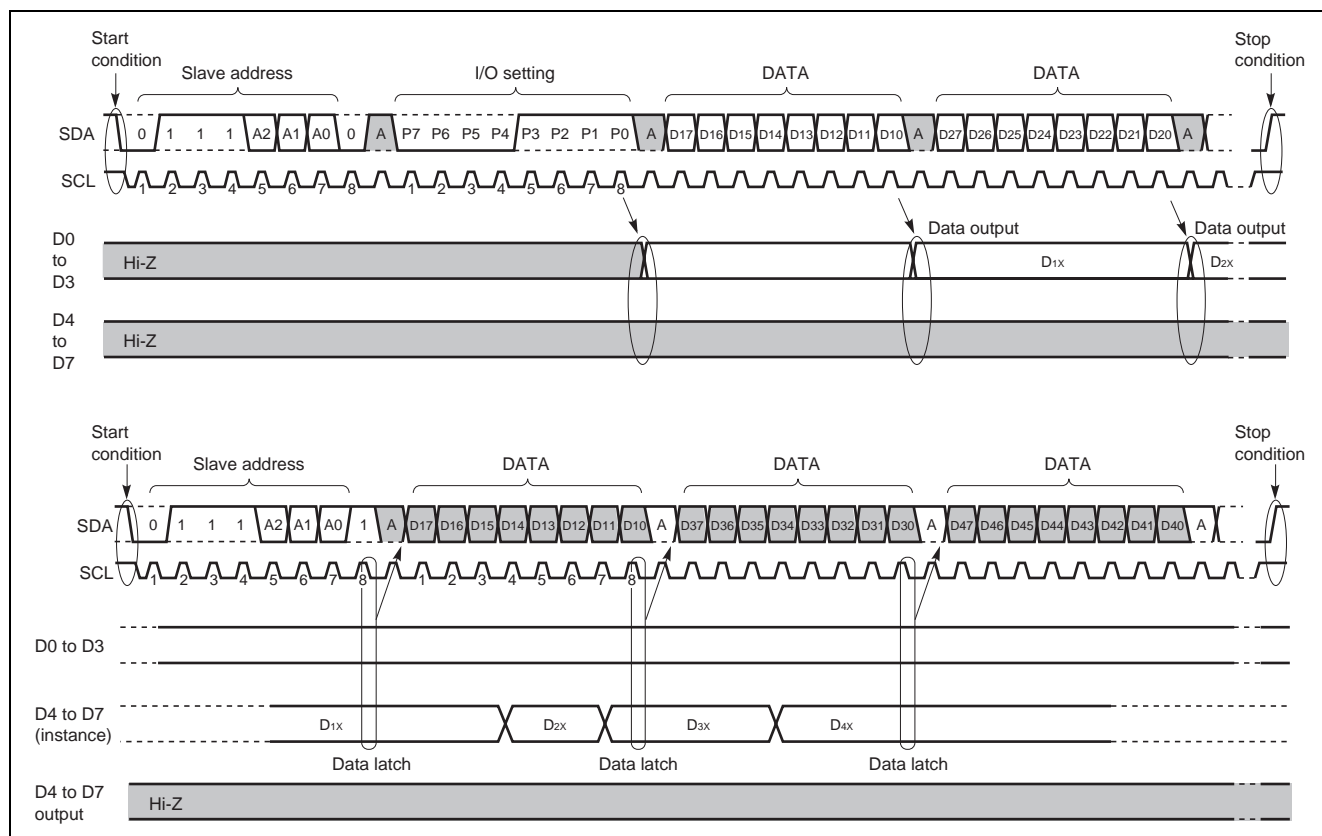
- In a case of a data conversion from parallel to serial.

All I/O setting resistors are set to low (input) in the write mode, before a parallel data is read. (All I/O setting resistors are set to the input mode after power-on).



- In case the I/O setting is different between each terminals.

An example: the parallel port terminals of D0 to D3 and D4 to D7 are assigned as output and input terminals, respectively.



- Write mode

The terminal assigned as an output provides the data written in the output data latch.

After power-on, all terminals are reset to the input-state. Then an initial data low of the output latch are output after the I/O setting has been done. Finally the assigned output are provided after the 8-bit data transmission.

The terminal assigned as an input keeps the input condition (high-impedance) regardless of 8-bit data setting.

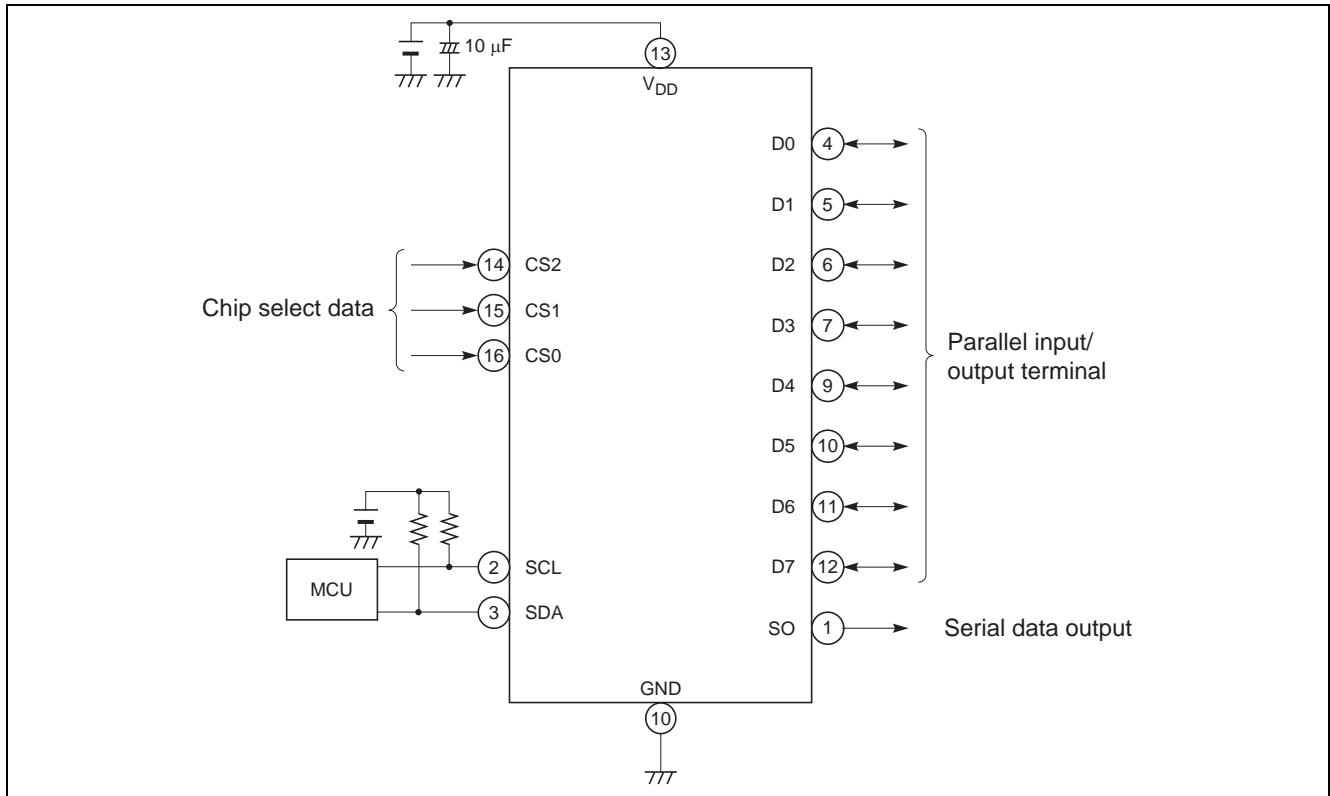
- Read mode

The input data is taken into the input latch on every 8th negative-going edge of the SCL clock through the terminal assigned as an input, and then the latched data is output via the SDA line.

The data of the output assigned terminal is also handled in the same procedures as above.



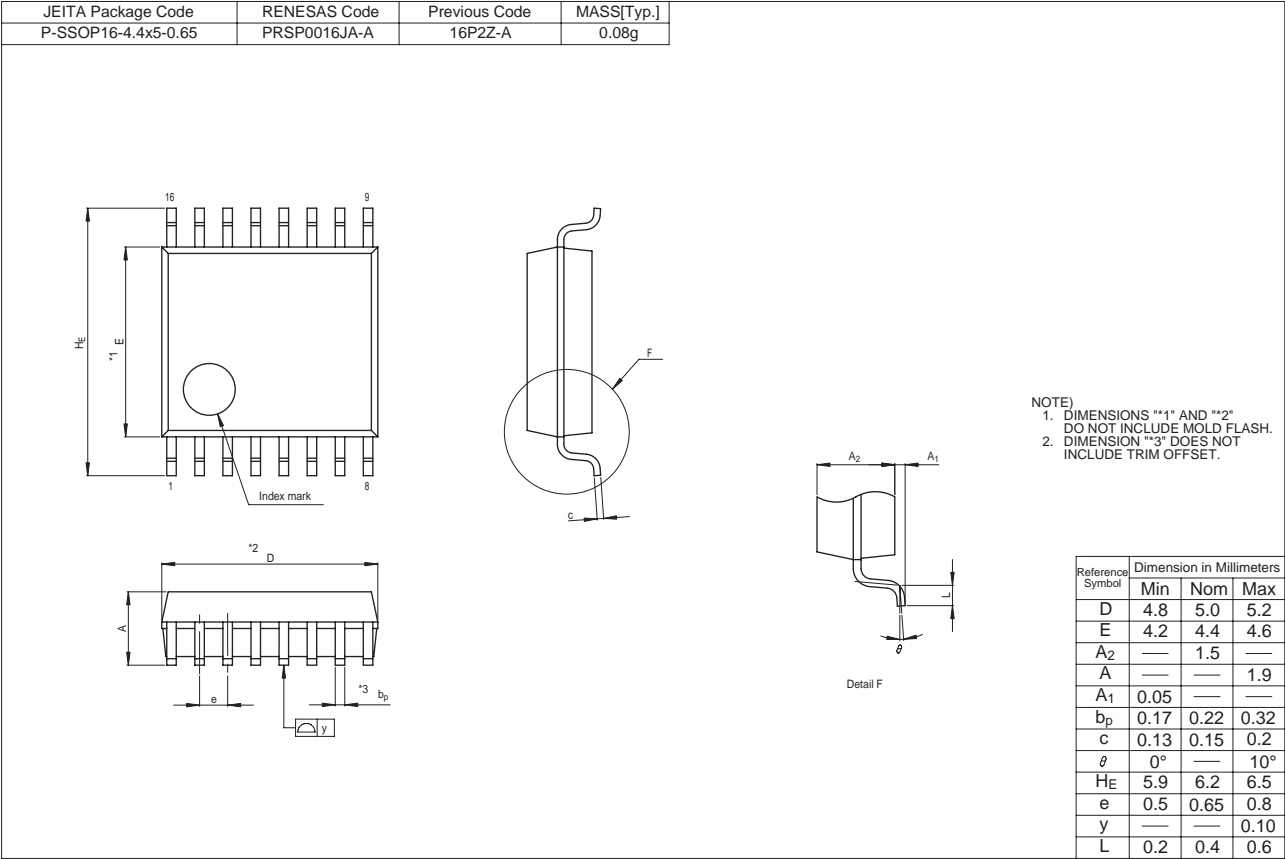
## Typical Application



## Precaution for Use

- Purchase of Renesas's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to I<sup>2</sup>C Standard Specification as defined by Philips.

Package Dimensions



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