☐ MN103002A

Type	MN103002A
Command Cache	4 K-byte (2-Way)
Data Cache	4 K-byte (2-Way)
Package **(Conventional Package)**	QFP160-P-2828F *Lead-free* (QFP160-P-2828B)
Minimum Instruction **Execution Time**	15 ns (at 3.3 V to lerance = ± 5%, 66 MHz)
Interrupts	• RESET • IRQ0 to 7 • NMI • Timer 0 to 8 • SIO0 to 5 • DMAC0 to 3 • WDT • System error

Timer Counter

Timer counter 0: 8-bit × 1
  (timer output, 16-bit timer clock source, interval timer, event count, clock source for serial I/F0)
    Clock source ···················· 1/(1, 8, 32) of I/O clock frequency; external clock input; underflow of timer 1, 2
    Interrupt source ··············· underflow of timer counter

Timer counter 1: 8-bit × 1
  (timer output, 16-bit timer clock source, interval timer, event count, clock source for serial I/F1)
    Clock source ···················· 1/(1, 8, 32) of I/O clock frequency; external clock input;
                                                output of timer counter 0; underflow of timer 0, 2
    Interrupt source ··············· underflow of timer counter

Timer counter 2: 8-bit × 1 (timer output; interval timer; event count; clock source for serial I/F 0, 2; DMA start)
    Clock source ···················· 1/(1, 8, 32) of I/O clock frequency; external clock input;
                                                output of timer counter 1; underflow of timer 0, 1
    Interrupt source ··············· underflow of timer counter

Timer counter 3: 8-bit × 1 (timer output; interval timer; event count; clock source for serial I/F 1, 2; DMA start)
    Clock source ···················· 1/(1, 8, 32) of I/O clock frequency; external clock input;
                                                output of timer counter 2; underflow of timer 0, 1, 2
    Interrupt source ··············· underflow of timer counter

Timer counter 4: 16-bit × 1 (timer output, down count, interval timer, event count)
    Clock source ···················· 1/(1, 8, 32) of I/O clock frequency; external clock input;
                                                underflow of timer 0, 1, 2
    Interrupt source ··············· underflow of timer counter

Timer counter 5: 16-bit × 1 (timer output, down count, interval timer, event count)
    Clock source ···················· 1/(1, 8, 32) of I/O clock frequency; external clock input;
                                                output of timer counter 4; underflow of timer 0, 1, 2
    Interrupt source ··············· underflow of timer counter

Timer counter 6: 16-bit × 1
  (event count, input capture, toggle output, PWM output, high-speed PWM output, up count, interval timer,
  one-shot output)
    Clock source ···················· 1/(1, 8, 32) of I/O clock frequency; external clock input;
                                                underflow of timer 0, 1, 2
    Interrupt source ··············· overflow of timer counter; compare capture A, B

Watchdog timer × 1 (watchdog overflow output)
    Clock source ···················· system clock
    Interrupt source ··············· overflow of watchdog timer

DMA Controller

Number of channels: 4
Unit of transfer: 8/16/32 bits
Max. Transfer cycles: 65536
Starting factor: external request, various types of interrupt, software
Transfer method: 2-bus cycle transfer, 1-bus cycle transfer
Transfer modes: word transfer, burst transfer, intermittent transfer

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■ **Serial Interface**

Serial 0: 8-bit × 1 (start-stop synchronous mode, clock synchronous mode, I²C mode)

Clock source ···················· I/O clock; timer counter 0, 2; external clock

Serial 1: 8-bit × 1 (start-stop synchronous mode, clock synchronous mode, I²C mode)

Clock source ···················· I/O clock; timer counter 1, 3; external clock

Serial 2: 8-bit × 1 (start-stop synchronous mode with CTS control)

Clock source ···················· I/O clock; timer counter 2, 3; external clock
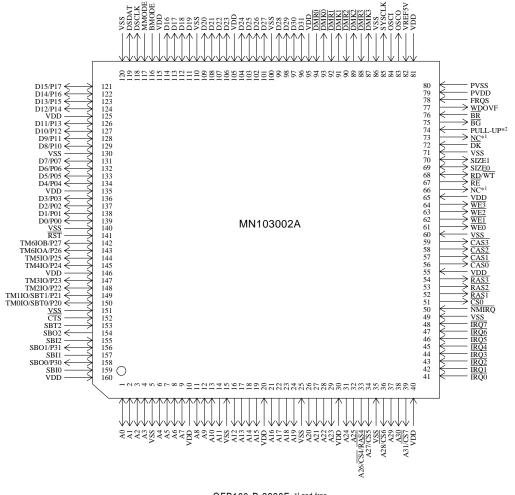
■ **I/O Pins**	**I/O**	26	• Common use

■ **Electrical Characteristics**

Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	fosc = 16.6 MHz FRQS pin = Hi level Output open			250	mA
Supply current at SLEEP	IDD2	fosc = 16.6 MHz FRQS pin = Hi level Output open			50	mA
Supply current at HALT	IDD3	fosc = 16.6 MHz FRQS pin = Hi level Output open			6	mA
Supply current at stopping	IDD4	fosc = oscillation stopped Output open			1.25	mA

(Ta = −20°C to +70°C, VDD = 3.3 V , VSS = 0 V)

Pin Assignment

Top pins (left to right, 120–81):
VSS, DSDAT, MMODE, BMODE, VDD, D16, D17, D18, D19, VSS, D20, D21, D22, D23, VDD, D24, D25, D26, D27, VSS, D28, D29, D30, D31, VDD, DMR0, DMK0, DMR1, DMK1, DMR2, DMK2, DMR3, DMK3, VSS, SYSCLK, OSCI, OSCO, VREF5V, VDD

Left pins (121–160):

Pin	Signal
121	D15/P17
122	D14/P16
123	D13/P15
124	D12/P14
125	VDD
126	D11/P13
127	D10/P12
128	D9/P11
129	D8/P10
130	VSS
131	D7/P07
132	D6/P06
133	D5/P05
134	D4/P04
135	VDD
136	D3/P03
137	D2/P02
138	D1/P01
139	D0/P00
140	VSS
141	RST
142	TM6IOB/P27
143	TM6IOA/P26
144	TM5IO/P25
145	TM4IO/P24
146	VDD
147	TM3IO/P23
148	TM2IO/P22
149	TM1IO/SBT1/P21
150	TM0IO/SBT0/P20
151	VSS
152	CTS
153	SBT2
154	SBO2
155	SBI2
156	SBO1/P31
157	SBI1
158	SBO0/P30
159	SBI0
160	VDD

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Right pins (80–41):

Pin	Signal
80	PVSS
79	PVDD
78	FRQS
77	WDOVF
76	BR
75	BG
74	PULL-UP*2
73	NC*1
72	DK
71	VSS
70	SIZE1
69	SIZE0
68	RD/WT
67	RE
66	NC*1
65	VDD
64	WE3
63	WE2
62	WE1
61	WE0
60	VSS
59	CAS3
58	CAS2
57	CAS1
56	CAS0
55	VDD
54	RAS3
53	RAS2
52	RAS1
51	CS0
50	NMIRQ
49	VSS
48	IRQ7
47	IRQ6
46	IRQ5
45	IRQ4
44	IRQ3
43	IRQ2
42	IRQ1
41	IRQ0

Bottom pins (left to right, 1–40):
A0, A1, A2, A3, VSS, A4, A5, A6, A7, VDD, A8, A9, A10, A11, VSS, A12, A13, A14, A15, VDD, A16, A17, A18, A19, VSS, A20, A21, A22, A23, VDD, A24, A25, A26/CS4/RAS4, A27/CS5, VSS, A28/CS6, A29, A30, A31/CS7, VDD

QFP160-P-2828F *Lead-free
(QFP160-P-2828B)

*1: Set to open.

*2: Pull up via the resistor.

Support Tool

In-circuit Emulator	PX-ICE103002-QFP160-P-2828B
ROM Emulator	Partner ET-II (KMC product), ROMICE64 (Computex Co., Ltd, product)
On-board Development Tools	PX-ODB103S-O CSIDE-MN10300 (Computex Co., Ltd, product)

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