

## High-Speed PWM Controller

### 1 Features

- Improved versions of the UC3823/UC3825 PWMs
- Compatible with voltage-mode or current-mode control methods
- Practical operation at switching frequencies to 1 MHz
- 50-ns propagation delay to output
- High-current dual totem pole outputs (2-A peak)
- Trimmed oscillator discharge current
- Low 100- $\mu$ A startup current
- Pulse-by-pulse current limiting comparator
- Latched overcurrent comparator with full cycle restart

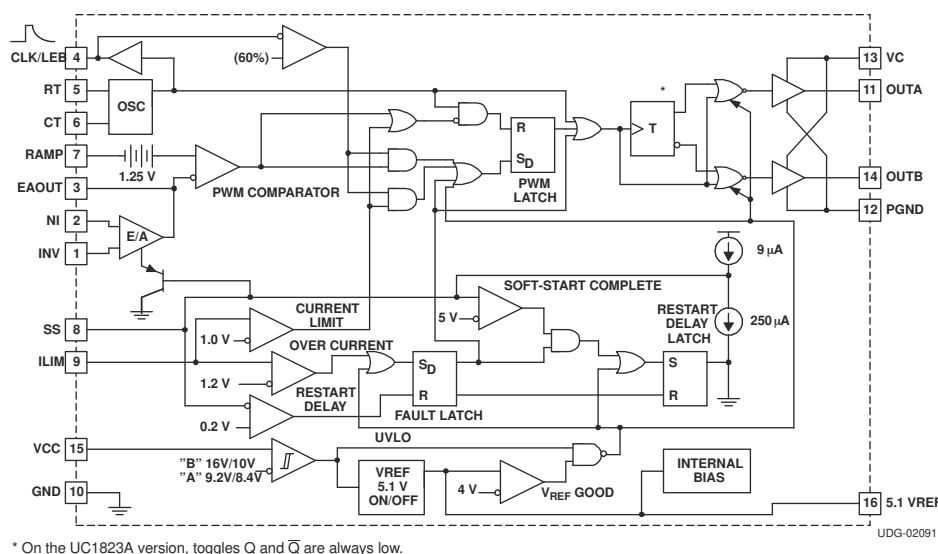
### 2 Description

The UC3823A and UC3823B and the UC3825A and UC3825B family of PWM controllers are improved versions of the standard UC3823 and UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12 MHz, while input offset voltage is 2 mV. Current limit threshold is assured to a tolerance of 5%. Oscillator discharge current is specified at 10 mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100  $\mu$ A, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2-A peak currents during transitions.

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2 V. The overcurrent comparator sets a latch that ensures full discharge of the soft-start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft-start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 CLOCK pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

The UC3825A and UC3825B have dual alternating outputs and the same pin configuration of the UC3825. The UC3823A and UC3823B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A and UC3823B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. A version parts have UVLO thresholds identical to the original UC3823 and UC3825. The *B* versions have UVLO thresholds of 16 V and 10 V, intended for ease of use in off-line applications.

Consult the application note, *The UC3823A,B and UC3825A,B Enhanced Generation of PWM Controllers (SLUA125)* for detailed technical and applications information.



**Figure 2-1. Block Diagram**



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## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision E (September 2010) to Revision F (August 2022)</b> | <b>Page</b> |
|-----------------------------------------------------------------------------|-------------|
| • Added SOIC package.....                                                   | <b>3</b>    |
| • Added Thermal Information.....                                            | <b>5</b>    |

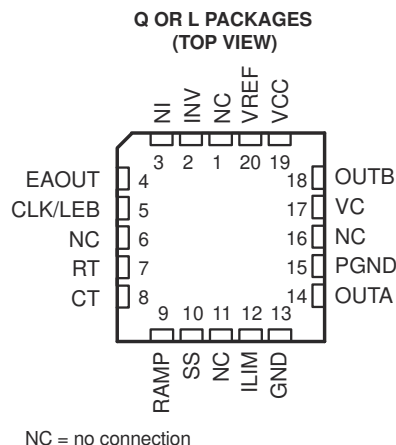
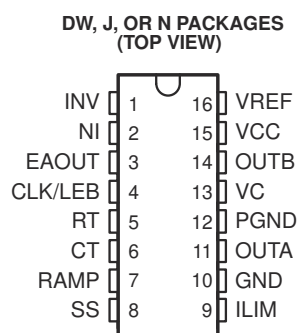
## 4 Ordering Information

| T <sub>A</sub> | MAXIMUM<br>DUTY CYCLE | UVLO                           |                |                               |                 |                |                               |
|----------------|-----------------------|--------------------------------|----------------|-------------------------------|-----------------|----------------|-------------------------------|
|                |                       | 9.2 V / 8.4 V                  |                |                               | 16 V / 10 V     |                |                               |
|                |                       | SOIC-16 <sup>(1)</sup><br>(DW) | PDIP-16<br>(N) | PLCC-20 <sup>(1)</sup><br>(Q) | SOIC-16<br>(DW) | PDIP-16<br>(N) | PLCC-20 <sup>(1)</sup><br>(Q) |
| 40°C to 85°C   | < 100%                | UC2823ADW                      | UC2823AN       | UC2823AQ                      | UC2823BDW       | UC2823BN       |                               |
|                | < 50%                 | UC2825ADW                      | UC2825AN       | UC2825AQ                      | UC2825BDW       | UC2825BN       |                               |
| 0°C to 70°C    | < 100%                | UC3823ADW                      | UC3823AN       | UC3823AQ                      | UC3823BDW       | UC3823BN       |                               |
|                | < 50%                 | UC3825ADW                      | UC3825AN       | UC3825AQ                      | UC3825BDW       | UC3825BN       | UC3825BQ                      |

(1) The DW and Q packages are also available taped and reeled. Add TR suffix to the device type (i.e., UC2823ADWR). To order quantities of 1000 devices per reel for the Q package and 2000 devices per reel for the DW package.

## 5 Pin Configuration and Functions

| T <sub>A</sub> | MAXIMUM<br>DUTY CYCLE | UVLO (9.2 V/8.4 V)                   |                                      |
|----------------|-----------------------|--------------------------------------|--------------------------------------|
|                |                       | CDIP-16 (J)                          | LCCC-20 (L)                          |
| 55°C to 125°C  | < 100%                | UC1823AJ, UC1823AJ883B, UC1823AJQMLV | UC1823AL, UC1823AL883B               |
|                | < 50%                 | UC1825AJ, UC1825AJ883B, UC1825AJQMLV | UC1825AL, UC1825AL883B, UC1825ALQMLV |



## Terminal Functions

| TERMINAL |             |        | I/O | DESCRIPTION                                                                                                                                                                                                                                                       |
|----------|-------------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME     | NO.         |        |     |                                                                                                                                                                                                                                                                   |
|          | J, N, or DW | Q or L |     |                                                                                                                                                                                                                                                                   |
| CLK/LEB  | 4           | 5      | O   | Output of the internal oscillator                                                                                                                                                                                                                                 |
| CT       | 6           | 8      | I   | Timing capacitor connection pin for oscillator frequency programming. The timing capacitor should be connected to the device ground using minimal trace length.                                                                                                   |
| EAOUT    | 3           | 4      | O   | Output of the error amplifier for compensation                                                                                                                                                                                                                    |
| GND      | 10          | 13     |     | Analog ground return pin                                                                                                                                                                                                                                          |
| ILIM     | 9           | 12     | I   | Input to the current limit comparator                                                                                                                                                                                                                             |
| INV      | 1           | 2      | I   | Inverting input to the error amplifier                                                                                                                                                                                                                            |
| NI       | 2           | 3      | I   | Non-inverting input to the error amplifier                                                                                                                                                                                                                        |
| OUTA     | 11          | 14     | O   | High current totem pole output A of the on-chip drive stage.                                                                                                                                                                                                      |
| OUTB     | 14          | 18     | O   | High current totem pole output B of the on-chip drive stage.                                                                                                                                                                                                      |
| PGND     | 12          | 15     |     | Ground return pin for the output driver stage                                                                                                                                                                                                                     |
| RAMP     | 7           | 9      | I   | Non-inverting input to the PWM comparator with 1.25-V internal input offset. In voltage mode operation, this serves as the input voltage feed-forward function by using the CT ramp. In peak current mode operation, this serves as the slope compensation input. |
| RT       | 5           | 7      | I   | Timing resistor connection pin for oscillator frequency programming                                                                                                                                                                                               |
| SS       | 8           | 10     | I   | Soft-start input pin which also doubles as the maximum duty cycle clamp.                                                                                                                                                                                          |
| VC       | 13          | 17     |     | Power supply pin for the output stage. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths.                                                                                                                 |
| VCC      | 15          | 19     |     | Power supply pin for the device. This pin should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor with minimal trace lengths                                                                                                                        |
| VREF     | 16          | 20     | O   | 5.1-V reference. For stability, the reference should be bypassed with a 0.1-μF monolithic ceramic low ESL capacitor and minimal trace length to the ground plane.                                                                                                 |

## 6 Specifications

### 6.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

|                    |                                                               |               | VALUE      | UNIT |
|--------------------|---------------------------------------------------------------|---------------|------------|------|
| V <sub>IN</sub>    | Supply voltage,                                               | VC, VCC       | 22         | V    |
| I <sub>O</sub>     | Source or sink current,DC                                     | OUTA, OUTB    | 0.5        | A    |
| I <sub>O</sub>     | Source or sink current, pulse (0.5 μs)                        | OUTA, OUTB    | 2.2        | A    |
| Analog inputs      |                                                               | INV, NI, RAMP | –0.3 to 7  | V    |
|                    |                                                               | ILIM, SS      | –0.3 to 6  | V    |
| Power ground       |                                                               | PGND          | ±0.2       | V    |
| I <sub>CLK</sub>   | Clock output current                                          | CLK/LEB       | –5         | mA   |
| I <sub>O(EA)</sub> | Error amplifier output current                                | EAOUT         | 5          | mA   |
| I <sub>SS</sub>    | Soft-start sink current                                       | SS            | 20         | mA   |
| I <sub>OSC</sub>   | Oscillator charging current                                   | RT            | –5         | mA   |
| T <sub>J</sub>     | Operating virtual junction temperature range                  |               | –55 to 150 | °C   |
| T <sub>stg</sub>   | Storage temperature                                           |               | –65 to 150 | °C   |
|                    | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds  |               | –55 to 150 | °C   |
| t <sub>STG</sub>   | Storage temperature                                           |               | –65 to 150 | °C   |
|                    | Lead temperature 1,6 mm (1/16 inch) from cases for 10 seconds |               | 300        | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 Thermal Information

| PACKAGE             | θ <sub>JA</sub>      | θ <sub>JC</sub>   |
|---------------------|----------------------|-------------------|
| J-16                | 80-120               | 28 <sup>(2)</sup> |
| N-16                | 90 <sup>(1)</sup>    | 45                |
| DW-16               | 45-90 <sup>(1)</sup> | 25                |
| PLCC-20 (Q package) | 43-75 <sup>(1)</sup> | 34                |
| LCC-20 (L package)  | 70-80                | 20 <sup>(2)</sup> |

- (1) Specified θ<sub>JA</sub> (junction to ambient) is for devices mounted to 5 in2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in2 aluminum PC board. Test PWB was 0.062" thick and typically used 0.635 mm trace widths for power packages and 1.3 mm trace widths for non-power packages with 100 x 100 mil probe land area at the end of each trace.
- (2) θ<sub>JC</sub> data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states, "The baseline values shown are worst case (mean + 2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die size greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W".

## 6.3 ELECTRICAL CHARACTERISTICS

$T_A = -55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  for the UC1823A/UC1825A,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  for the UC2823x/UC2825x,  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  for the UC3823x/UC3825x,  $R_T = 3.65\text{ k}\Omega$ ,  $C_T = 1\text{ nF}$ ,  $V_{CC} = 12\text{ V}$ ,  $T_A = T_J$  (unless otherwise noted)

| PARAMETER                              |                                      | TEST CONDITIONS                                                                 | MIN  | TYP       | MAX  | UNIT                       |
|----------------------------------------|--------------------------------------|---------------------------------------------------------------------------------|------|-----------|------|----------------------------|
| <b>REFERENCE, <math>V_{REF}</math></b> |                                      |                                                                                 |      |           |      |                            |
| $V_O$                                  | Output voltage range                 | $T_J = 25^{\circ}\text{C}$ , $I_O = 1\text{ mA}$                                | 5.05 | 5.1       | 5.15 | V                          |
|                                        | Line regulation                      | $12\text{ V} \leq V_{CC} \leq 20\text{ V}$                                      |      | 2         | 15   | mV                         |
|                                        | Load regulation                      | $1\text{ mA} \leq I_O \leq 10\text{ mA}$                                        |      | 5         | 20   |                            |
|                                        | Total output variation               | Line, load, temperature                                                         | 5.03 |           | 5.17 | V                          |
|                                        | Temperature stability <sup>(1)</sup> | $T_{(min)} < T_A < T_{(max)}$                                                   |      | 0.2       | 0.4  | mV/ $^{\circ}\text{C}$     |
|                                        | Output noise voltage <sup>(1)</sup>  | $10\text{ Hz} < f < 10\text{ kHz}$                                              |      | 50        |      | $\mu\text{V}_{\text{RMS}}$ |
|                                        | Long term stability <sup>(1)</sup>   | $T_J = 125^{\circ}\text{C}$ , 1000 hours                                        |      | 5         | 25   | mV                         |
|                                        | Short circuit current                | $V_{REF} = 0\text{ V}$                                                          | 30   | 60        | 90   | mA                         |
| <b>OSCILLATOR</b>                      |                                      |                                                                                 |      |           |      |                            |
| $f_{\text{OSC}}$                       | Initial accuracy <sup>(1)</sup>      | $T_J = 25^{\circ}\text{C}$                                                      | 375  | 400       | 425  | kHz                        |
|                                        |                                      | $R_T = 6.6\text{ k}\Omega$ , $C_T = 220\text{ pF}$ , $T_A = 25^{\circ}\text{C}$ | 0.9  | 1         | 1.1  | MHz                        |
|                                        | Total variation <sup>(1)</sup>       | Line, temperature                                                               | 350  |           | 450  | kHz                        |
|                                        |                                      | $R_T = 6.6\text{ k}\Omega$ , $C_T = 220\text{ pF}$                              | 0.85 |           | 1.15 | MHz                        |
|                                        | Voltage stability                    | $12\text{ V} < V_{CC} < 20\text{ V}$                                            |      |           | 1%   |                            |
|                                        | Temperature stability <sup>(1)</sup> | $T_{(min)} < T_A < T_{(max)}$                                                   |      | $\pm 5\%$ |      |                            |
|                                        | High-level output voltage, clock     |                                                                                 | 3.7  | 4         |      | V                          |
|                                        | Low-level output voltage, clock      |                                                                                 |      | 0         | 0.2  |                            |
|                                        | Ramp peak                            |                                                                                 | 2.6  | 2.8       | 3    |                            |
|                                        | Ramp valley                          |                                                                                 | 0.7  | 1         | 1.25 |                            |
|                                        | Ramp valley-to-peak                  |                                                                                 | 1.6  | 1.8       | 2    |                            |
| $I_{\text{OSC}}$                       | Oscillator discharge current         | $R_T = \text{OPEN}$ , $V_{CT} = 2\text{ V}$                                     | 9    | 10        | 11   | mA                         |
| <b>ERROR AMPLIFIER</b>                 |                                      |                                                                                 |      |           |      |                            |
|                                        | Input offset voltage                 |                                                                                 |      | 2         | 10   | mV                         |
|                                        | Input bias current                   |                                                                                 |      | 0.6       | 3    | $\mu\text{A}$              |
|                                        | Input offset current                 |                                                                                 |      | 0.1       | 1    |                            |
|                                        | Open loop gain                       | $1\text{ V} < V_O < 4\text{ V}$                                                 | 60   | 95        |      | dB                         |
| CMRR                                   | Common mode rejection ratio          | $1.5\text{ V} < V_{CM} < 5.5\text{ V}$                                          | 75   | 95        |      |                            |
| PSRR                                   | Power supply rejection ratio         | $12\text{ V} < V_{CC} < 20\text{ V}$                                            | 85   | 110       |      |                            |
| $I_{O(\text{sink})}$                   | Output sink current                  | $V_{EAOUT} = 1\text{ V}$                                                        | 1    | 2.5       |      | mA                         |
| $I_{O(\text{src})}$                    | Output source current                | $V_{EAOUT} = 4\text{ V}$                                                        |      | -1.3      | -0.5 |                            |
|                                        | High-level output voltage            | $I_{EAOUT} = -0.5\text{ mA}$                                                    | 4.5  | 4.7       | 5    | V                          |
|                                        | Low-level output voltage             | $I_{EAOUT} = -1\text{ mA}$                                                      | 0    | 0.5       | 1    |                            |
|                                        | Gain bandwidth product               | $f = 200\text{ kHz}$                                                            | 6    | 12        |      | Mhz                        |
|                                        | Slew rate <sup>(1)</sup>             |                                                                                 | 6    | 9         |      | V/ $\mu\text{s}$           |

(1) Ensured by design. Not production tested.

## 6.4 ELECTRICAL CHARACTERISTICS

$T_A = -55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  for the UC1823A/UC1825A,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  for the UC2823x/UC2825x,  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  for the UC3823x/UC3825x,  $R_T = 3.65\text{ k}\Omega$ ,  $C_T = 1\text{ nF}$ ,  $V_{CC} = 12\text{ V}$ ,  $T_A = T_J$  (unless otherwise noted)

| PARAMETER                              |                                                     | TEST CONDITIONS                                                 | MIN  | TYP  | MAX  | UNIT |
|----------------------------------------|-----------------------------------------------------|-----------------------------------------------------------------|------|------|------|------|
| PWM COMPARATOR                         |                                                     |                                                                 |      |      |      |      |
| I <sub>BIAS</sub>                      | Bias current, RAMP                                  | V <sub>RAMP</sub> = 0 V                                         |      | –1   | –8   | μA   |
|                                        | Minimum duty cycle                                  |                                                                 |      |      | 0%   |      |
|                                        | Maximum duty cycle                                  |                                                                 | 85%  |      |      |      |
| t <sub>LEB</sub>                       | Leading edge blanking time                          | R <sub>LEB</sub> = 2 kΩ, C <sub>LEB</sub> = 470 pF              | 300  | 375  | 450  | ns   |
| R <sub>LEB</sub>                       | Leading edge blanking resistance                    | V <sub>CLK/LEB</sub> = 3 V                                      | 8.5  | 10.0 | 11.5 | kΩ   |
| V <sub>ZDC</sub>                       | Zero dc threshold voltage, EAOUT                    | V <sub>RAMP</sub> = 0 V                                         | 1.10 | 1.25 | 1.4  | V    |
| t <sub>DELAY</sub>                     | Delay-to-output time <sup>(1)</sup>                 | V <sub>EAOUT</sub> = 2.1 V, V <sub>ILIM</sub> = 0 V to 2 V step |      | 50   | 80   | ns   |
| CURRENT LIMIT / START SEQUENCE / FAULT |                                                     |                                                                 |      |      |      |      |
| I <sub>SS</sub>                        | Soft-start charge current                           | V <sub>SS</sub> = 2.5 V                                         | 8    | 14   | 20   | μA   |
| V <sub>SS</sub>                        | Full soft-start threshold voltage                   |                                                                 | 4.3  | 5    |      | V    |
| I <sub>DSCH</sub>                      | Restart discharge current                           | V <sub>SS</sub> = 2.5 V                                         | 100  | 250  | 350  | μA   |
| I <sub>SS</sub>                        | Restart threshold voltage                           |                                                                 |      | 0.3  | 0.5  | V    |
| I <sub>BIAS</sub>                      | ILIM bias current                                   | V <sub>ILIM</sub> = 0 V to 2 V step                             |      |      | 15   | μA   |
| I <sub>CL</sub>                        | Current limit threshold voltage                     |                                                                 | 0.95 | 1    | 1.05 | V    |
|                                        | Overcurrent threshold voltage                       |                                                                 | 1.14 | 1.2  | 1.26 |      |
| t <sub>d</sub>                         | Delay-to-output time, ILIM <sup>(1)</sup>           | V <sub>ILIM</sub> = 0 V to 2 V step                             |      | 50   | 80   | ns   |
| OUTPUT                                 |                                                     |                                                                 |      |      |      |      |
|                                        | Low-level output saturation voltage                 | I <sub>OUT</sub> = 20 mA                                        |      | 0.25 | 0.4  | V    |
|                                        |                                                     | I <sub>OUT</sub> = 200 mA                                       |      | 1.2  | 2.2  |      |
|                                        | High-level output saturation voltage                | I <sub>OUT</sub> = -20 mA                                       |      | 1.9  | 2.9  |      |
|                                        |                                                     | I <sub>OUT</sub> = -200 mA                                      |      | 2    | 3    |      |
| t <sub>r</sub> , t <sub>f</sub>        | Rise/fall time <sup>(1)</sup>                       | C <sub>L</sub> = 1 nF                                           |      | 20   | 45   | ns   |
| UNDERVOLTAGE LOCKOUT (UVLO)            |                                                     |                                                                 |      |      |      |      |
| Start threshold voltage                | UC2823B, UC2825B, UC3825B, UC3825B                  |                                                                 |      | 16   | 17   | V    |
|                                        | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A |                                                                 | 8.4  | 9.2  | 9.6  |      |
| Stop threshold voltage                 | UC2823B, UC2825B, UC3825B, UC3825B                  |                                                                 | 9    | 10   |      |      |
| OVLO hysteresis                        | UC1823A, UC1825A, UC2823A, UC2825A UC3825A, UC3825A |                                                                 | 0.4  | 0.8  | 1.2  |      |
|                                        | UC2823B, UC2825B, UC3825B, UC3825B                  |                                                                 | 5    | 6    | 7    |      |
| SUPPLY CURRENT                         |                                                     |                                                                 |      |      |      |      |
| I <sub>su</sub>                        | Startup current                                     | VC = VCC = V <sub>TH</sub> (start) –0.5 V                       |      | 100  | 300  | μA   |
| I <sub>CC</sub>                        | Input current                                       |                                                                 |      | 28   | 36   | mA   |

(1) Ensured by design. Not production tested.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 LEADING EDGE BLANKING

The UC3823A, UC2823B, UC3825A, and UC3825B perform fixed frequency pulse width modulation control. The UC3823A, and UC3823B outputs operate together at the switching frequency and can vary from zero to some value less than 100%. The UC3825A and UC3825B outputs are alternately controlled. During every other cycle, one output is off. Each output then switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator senses a ramp crossing a control voltage (error amplifier output) and terminates the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

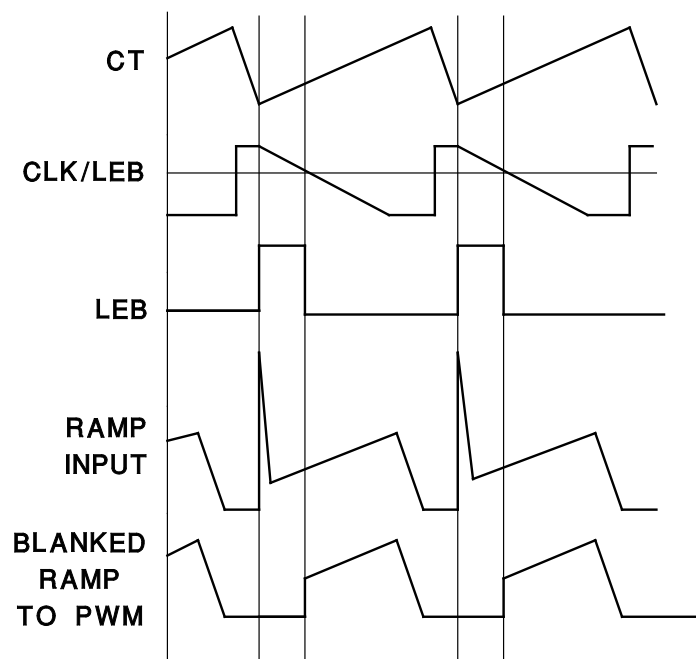
To program a leading edge blanking (LEB) period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10-k $\Omega$  resistor determines the blanked interval. The 10-k $\Omega$  resistor has a 10% tolerance. For more accuracy, an external 2-k $\Omega$  1% resistor (R) can be added, resulting in an equivalent resistance of 1.66 k $\Omega$  with a tolerance of 2.4%. The design equation is:

$$t_{LEB} = 0.5 \times (R \parallel 10 \text{ k}\Omega) \times C \quad (1)$$

Values of R less than 2 k $\Omega$  should not be used.

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the 1-V threshold, the pulse is terminated. The overcurrent comparator, however, is not blanked. It catches catastrophic overcurrent faults without a blanking delay. Any time the ILIM pin exceeds 1.2 V, the fault latch is set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.





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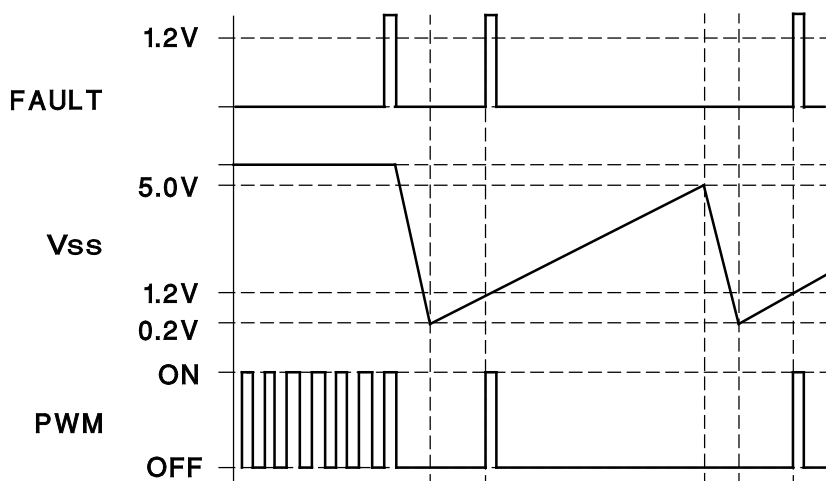
**Figure 7-1. Leading Edge Blanking Operational Waveforms**

## 7.2 UVLO, SOFT-START AND FAULT MANAGEMENT

Soft-start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amplifier output is also forced low. While the internal 9- $\mu$ A source charges the SS pin, the error amplifier output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2 V, the fault latch is set and the output pins are driven low. The soft-start cap is then discharged by a 250- $\mu$ A current sink. No more output pulses are allowed until soft-start is fully discharged and ILIM is below 1.2 V. At this point the fault latch resets and the chip executes a soft-start.

Should the fault latch get set during soft-start, the outputs are immediately terminated, but the soft-start capacitor does not discharge until it has been fully charged first. This results in a controlled hiccup interval for continuous fault conditions.



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**Figure 7-2. Soft-Start and Fault Waveforms**

### 7.3 ACTIVE LOW OUTPUTS DURING UVLO

The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

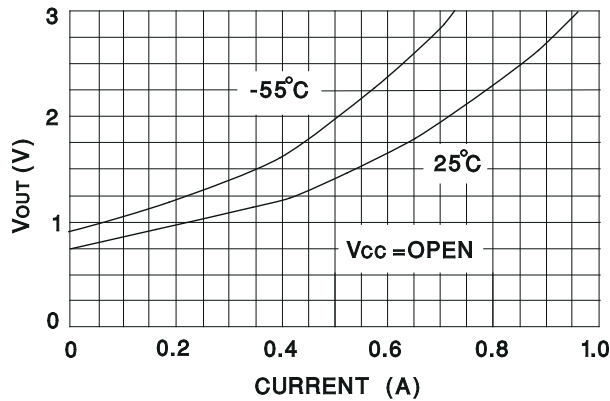


Figure 7-3. Output Voltage vs Output Current

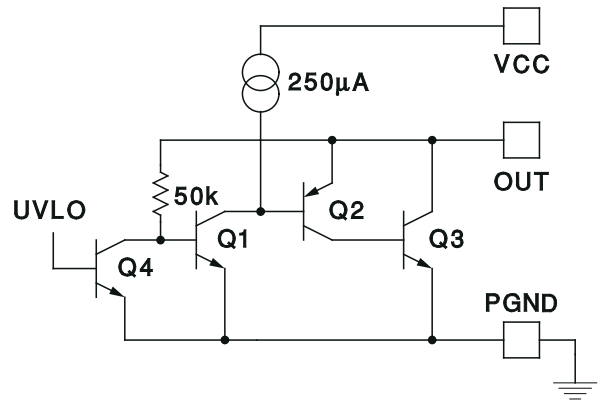


Figure 7-4. Output V and I During UVLO

### 7.4 CONTROL METHODS

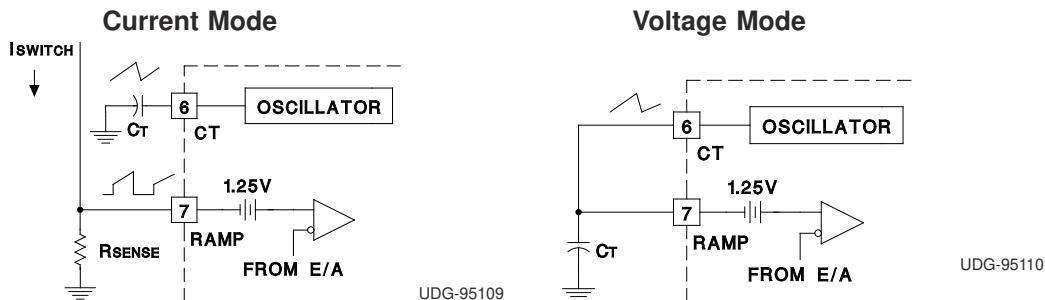


Figure 7-5. Control Methods

### 7.5 SYNCHRONIZATION

The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10% to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10 ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that the CLK/LEB pin no longer accepts an incoming synchronizing signal.

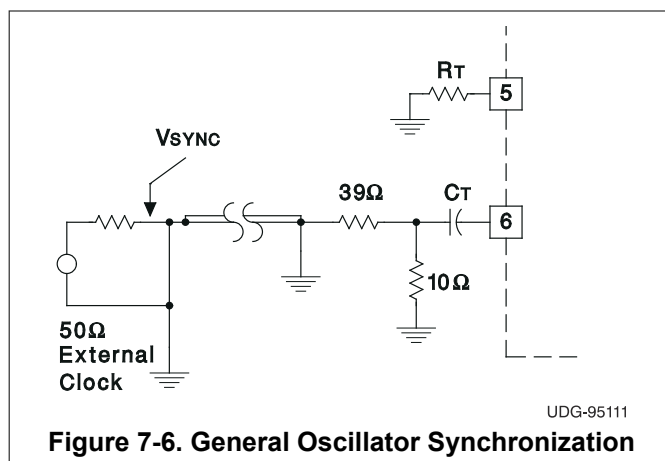


Figure 7-6. General Oscillator Synchronization

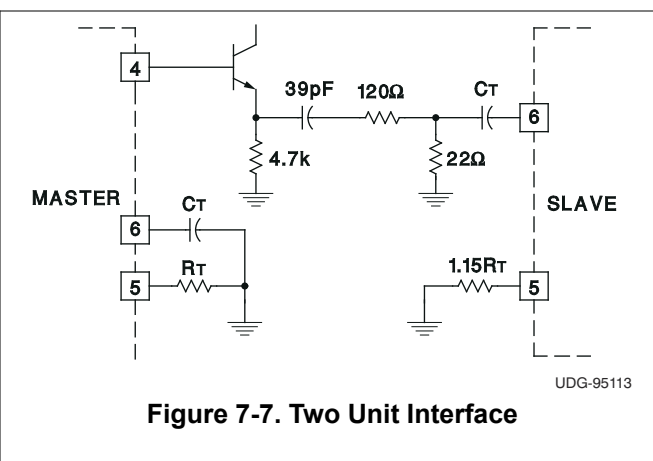


Figure 7-7. Two Unit Interface

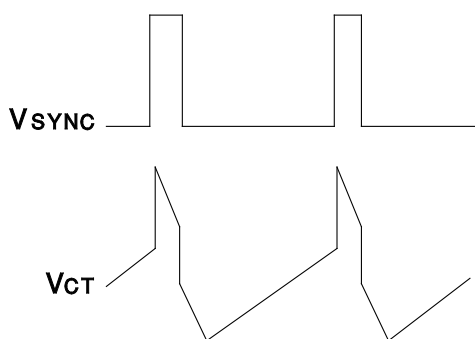
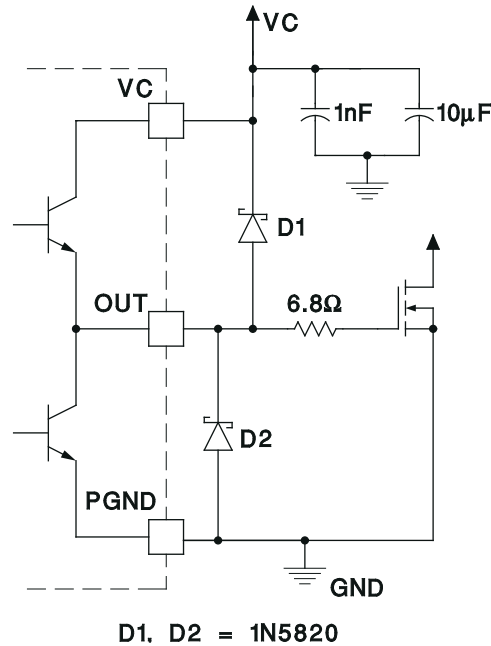


Figure 7-8. Operational Waveforms

## 7.6 HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A and UC3823AB, UC3825A, and UC3825B can deliver a 2-A peak current into a capacitive load. The output can slew a 1000-pF capacitor by 15 V in approximately 20 ns. Separate collector supply (VC) and power ground (PGND) pins help decouple the device's analog circuitry from the high-power gate drive noise. The use of 3-A Schottky diodes (1N5120, USD245, or equivalent) as shown in the Figure 7-10 from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although they are *single-ended* devices, two output drivers are available on the UC3823A and UC3823B devices. These can be *paralleled* by the use of a 0.5 Ω (noninductive) resistor connected in series with each output for a combined peak current of 4 A.



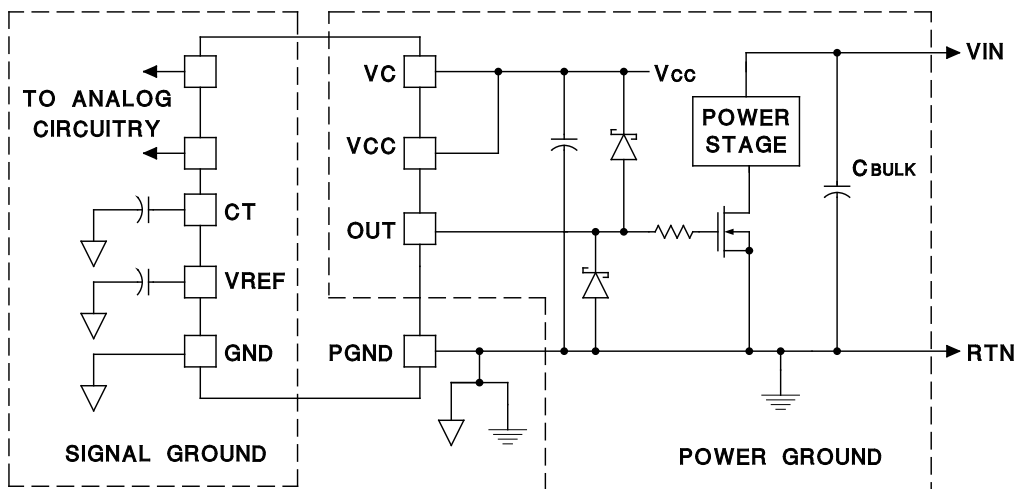
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**Figure 7-9. Power MOSFET Drive Circuit**

## 7.7 GROUND PLANES

Each output driver of these devices is capable of 2-A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1-mF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.

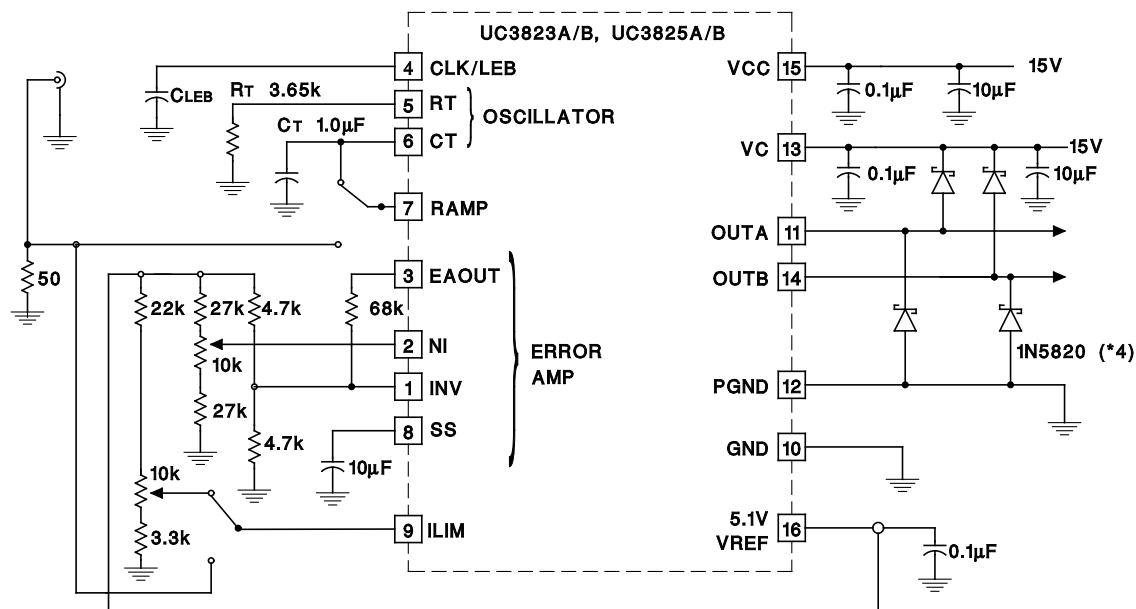


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**Figure 7-10. Ground Planes Diagram**

## 7.8 OPEN LOOP TEST CIRCUIT

This test fixture is useful for exercising many functions of this device family and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.



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**Figure 7-11. Open Loop Test Circuit Schematic**

## 8 Device and Documentation Support

### 8.1 Documentation Support

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                     |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------------------------|
| <a href="#">5962-87681022A</a>  | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87681022A<br>UC1825AL/<br>883B |
| <a href="#">5962-8768102EA</a>  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8768102EA<br>UC1825AJ/883B         |
| <a href="#">5962-89905022A</a>  | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>89905022A<br>UC1823AL/<br>883B |
| <a href="#">5962-8990502EA</a>  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8990502EA<br>UC1823AJ/883B         |
| <a href="#">5962-8990502VEA</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8990502VE<br>A<br>UC1823AJQMLV     |
| 5962-8990502VEA.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8990502VE<br>A<br>UC1823AJQMLV     |
| <a href="#">UC1823AJ</a>        | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1823AJ                                |
| UC1823AJ.A                      | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1823AJ                                |
| <a href="#">UC1823AJ883B</a>    | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8990502EA<br>UC1823AJ/883B         |
| UC1823AJ883B.A                  | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8990502EA<br>UC1823AJ/883B         |
| <a href="#">UC1823AL</a>        | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1823AL                                |
| UC1823AL.A                      | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1823AL                                |
| <a href="#">UC1823AL883B</a>    | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>89905022A<br>UC1823AL/<br>883B |
| UC1823AL883B.A                  | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>89905022A<br>UC1823AL/<br>883B |



| Orderable part number        | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                     |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------------------------|
| <a href="#">UC1825AJ</a>     | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1825AJ                                |
| UC1825AJ.A                   | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1825AJ                                |
| <a href="#">UC1825AJ883B</a> | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8768102EA<br>UC1825AJ/883B         |
| UC1825AJ883B.A               | Active        | Production           | CDIP (J)   16  | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8768102EA<br>UC1825AJ/883B         |
| <a href="#">UC1825AL</a>     | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1825AL                                |
| UC1825AL.A                   | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | UC1825AL                                |
| <a href="#">UC1825AL883B</a> | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87681022A<br>UC1825AL/<br>883B |
| UC1825AL883B.A               | Active        | Production           | LCCC (FK)   20 | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>87681022A<br>UC1825AL/<br>883B |
| <a href="#">UC2823ADW</a>    | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2823ADW                               |
| UC2823ADW.A                  | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2823ADW                               |
| <a href="#">UC2823ADWTR</a>  | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2823ADW                               |
| UC2823ADWTR.A                | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2823ADW                               |
| <a href="#">UC2823AN</a>     | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2823AN                                |
| UC2823AN.A                   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2823AN                                |
| <a href="#">UC2823BDW</a>    | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2823BDW                               |
| UC2823BDW.A                  | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2823BDW                               |
| <a href="#">UC2825ADW</a>    | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825ADW                               |
| UC2825ADW.A                  | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825ADW                               |
| UC2825ADWG4                  | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825ADW                               |
| <a href="#">UC2825ADWTR</a>  | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825ADW                               |
| UC2825ADWTR.A                | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825ADW                               |
| UC2825ADWTRG4                | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825ADW                               |
| <a href="#">UC2825AN</a>     | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2825AN                                |
| UC2825AN.A                   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2825AN                                |
| UC2825ANG4                   | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2825AN                                |

| Orderable part number       | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">UC2825BDW</a>   | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825BDW           |
| UC2825BDW.A                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825BDW           |
| UC2825BDWG4                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | UC2825BDW           |
| <a href="#">UC2825BN</a>    | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2825BN            |
| UC2825BN.A                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | UC2825BN            |
| <a href="#">UC3823ADW</a>   | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823ADW           |
| UC3823ADW.A                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823ADW           |
| <a href="#">UC3823ADWTR</a> | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823ADW           |
| UC3823ADWTR.A               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823ADW           |
| <a href="#">UC3823AN</a>    | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3823AN            |
| UC3823AN.A                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3823AN            |
| <a href="#">UC3823BDW</a>   | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823BDW           |
| UC3823BDW.A                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823BDW           |
| <a href="#">UC3823BDWTR</a> | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823BDW           |
| UC3823BDWTR.A               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3823BDW           |
| <a href="#">UC3825ADW</a>   | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825ADW           |
| UC3825ADW.A                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825ADW           |
| UC3825ADWG4                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825ADW           |
| <a href="#">UC3825ADWTR</a> | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825ADW           |
| UC3825ADWTR.A               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825ADW           |
| UC3825ADWTRG4               | Active        | Production           | SOIC (DW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825ADW           |
| <a href="#">UC3825AN</a>    | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3825AN            |
| UC3825AN.A                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3825AN            |
| UC3825ANG4                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3825AN            |
| <a href="#">UC3825BDW</a>   | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825BDW           |
| UC3825BDW.A                 | Active        | Production           | SOIC (DW)   16 | 40   TUBE             | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | 0 to 70      | UC3825BDW           |
| <a href="#">UC3825BDWTR</a> | Obsolete      | Production           | SOIC (DW)   16 | -                     | -           | Call TI                              | Call TI                           | 0 to 70      | UC3825BDW           |
| <a href="#">UC3825BN</a>    | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3825BN            |
| UC3825BN.A                  | Active        | Production           | PDIP (N)   16  | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | UC3825BN            |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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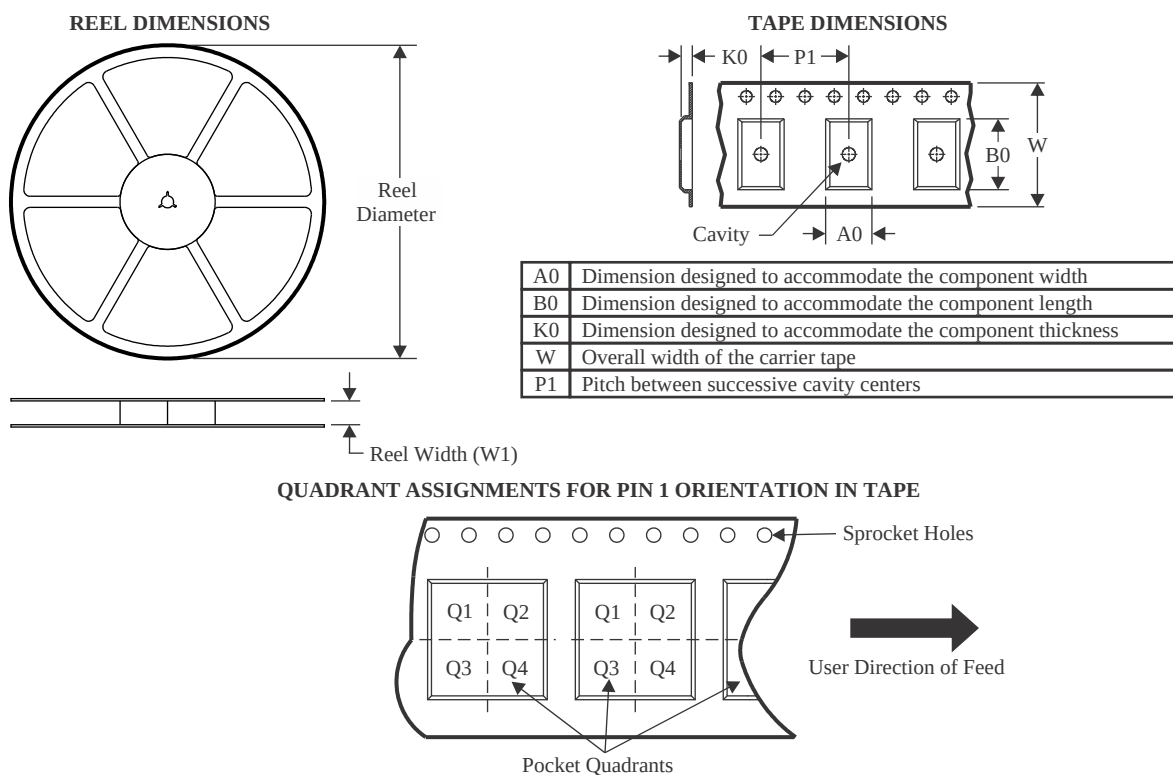
**OTHER QUALIFIED VERSIONS OF UC1823A, UC1823A-SP, UC1825A, UC2825A, UC3823A, UC3825A :**

- Catalog : [UC3823A](#), [UC1823A](#), [UC3825A](#)
- Automotive : [UC2825A-Q1](#)
- Enhanced Product : [UC2825A-EP](#)
- Military : [UC1823A](#), [UC1825A](#)
- Space : [UC1823A-SP](#), [UC1825A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

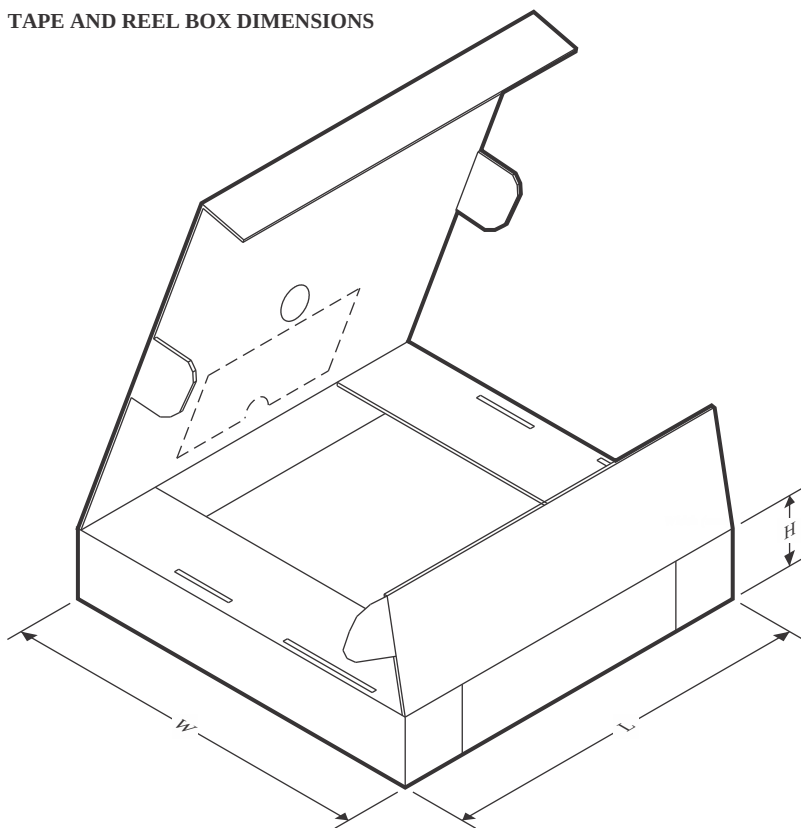
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

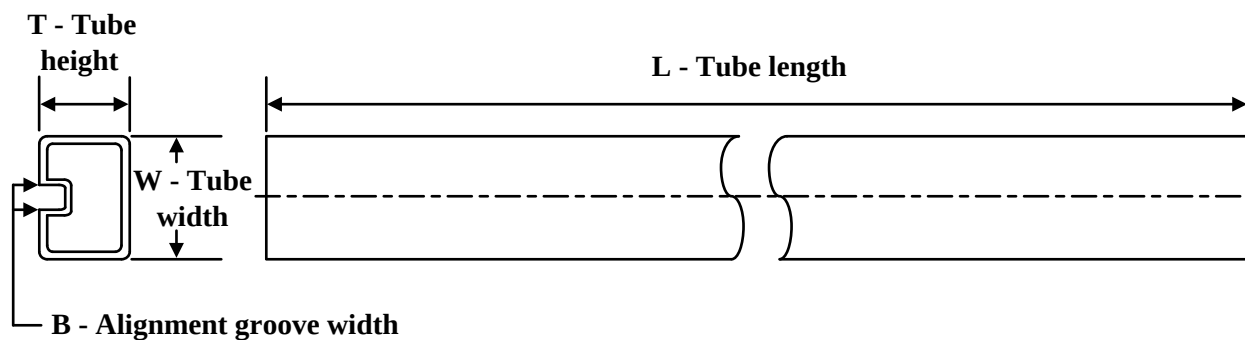
| Device      | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC2823ADWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| UC2825ADWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| UC3823ADWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| UC3823BDWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |
| UC3825ADWTR | SOIC         | DW              | 16   | 2000 | 330.0              | 16.4               | 10.75   | 10.7    | 2.7     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device      | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC2823ADWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| UC2825ADWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| UC3823ADWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| UC3823BDWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| UC3825ADWTR | SOIC         | DW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device         | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87681022A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-89905022A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1823AL       | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1823AL.A     | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1823AL883B   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1823AL883B.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1825AJ       | J            | CDIP         | 16   | 25  | 506.98 | 15.24  | 13440  | NA     |
| UC1825AJ.A     | J            | CDIP         | 16   | 25  | 506.98 | 15.24  | 13440  | NA     |
| UC1825AL       | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1825AL.A     | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1825AL883B   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC1825AL883B.A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| UC2823ADW      | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2823ADW.A    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2823AN       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2823AN.A     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2823BDW      | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2823BDW.A    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2825ADW      | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2825ADW.A    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2825ADWG4    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2825AN       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2825AN.A     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2825ANG4     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2825BDW      | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2825BDW.A    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2825BDWG4    | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC2825BN       | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC2825BN.A     | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| UC3823ADW   | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3823ADW.A | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3823AN    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3823AN.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3823BDW   | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3823BDW.A | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3825ADW   | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3825ADW.A | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3825ADWG4 | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3825AN    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3825AN.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3825ANG4  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3825BDW   | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3825BDW.A | DW           | SOIC         | 16   | 40  | 507    | 12.83  | 5080   | 6.6    |
| UC3825BN    | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| UC3825BN.A  | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |



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