SMBus Dual Monolithic High Side Switch

FEATURES

- **Two 0.4Ω/300mA N-Channel Switches**
- **Available in MS8 and SO-8 Packages**
- **SMBus and I²C Compatible**
- **0.6V V_{IL} and 1.4V V_{IH} for DATA and CLK**
- Low Standby Current: 14µA
- Separate Drain Connection to SW0
- Three Addresses from One Three-State Address Pin
- Independent Control of Up to Six Switches
- Built-In Power-On Reset Timer
- Built-In Undervoltage Lockout

APPLICATIONS

- Handheld Computer Power Management
- Computer Peripheral Control
- Laptop Computer Power Plane Switching
- Portable Equipment Power Control
- Industrial Control Systems
- ACPI SMBus Interface

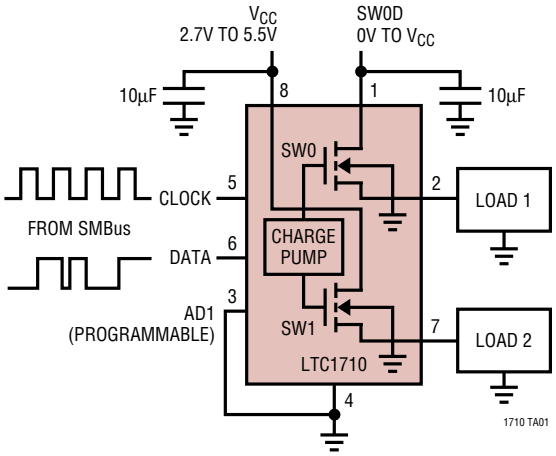
DESCRIPTION

The LTC®1710 SMBus dual switch has two built-in 0.4Ω/300mA switches that are controlled by a 2-wire SMBus interface. With a low standby current of 14µA (3.3V), the LTC1710 operates over an input voltage range of 2.7V to 5.5V while maintaining the SMBus specified 0.6V V_{IL} and 1.4V V_{IH} input thresholds.

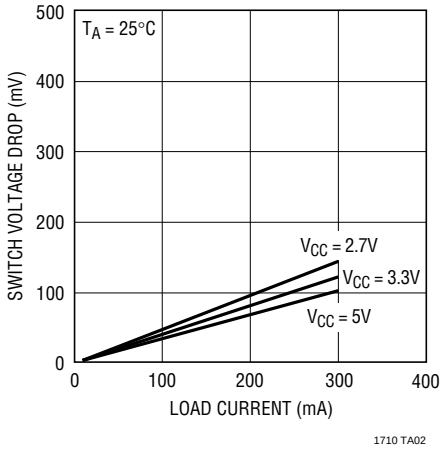
Using the 2-wire interface, CLK and DATA, the LTC1710 follows SMBus's Send Byte Protocol to independently control the two 0.4Ω internal N-channel power switches, which are fully enhanced by onboard charge pumps.

The LTC1710 has one three-state programmable address pin that allows three different addresses for a total of six available switches on the same bus. The LTC1710 also features a separate user-controlled drain supply (SW0D) to Switch 0 so that it can be used to control SMBus peripherials using a different power supply.

TYPICAL APPLICATION



Switch Voltage Drop vs Load Current



ABSOLUTE MAXIMUM RATINGS

(Voltages Referred to GND Pin) (Note 1)

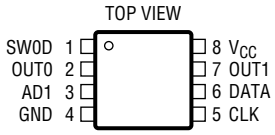
Input Supply Voltage (V_{CC}) ..... –0.3V to 6V
Input Supply Voltage (V_{CC}) with SW0 Connected
as a Low Side Switch ..... –0.3V to 3.6V
DATA, CLK (Bus Pins 6, 5)..... –0.3V to 6V*
AD1 (Address Pin 3) ..... –0.3V to V_{CC} + 0.3V
OUT0, OUT1 (Output Pins 2, 7) ..... –0.3V to 6V
SW0D (Switch 0 Drain Pin 1)..... –0.3V to 6V
OUT0, OUT1 (Output Pins 2, 7)
Continuous 300mA
Pulsed, <10µs (nonrepetitive) 1A

Operating Temperature Range
LTC1710C..... 0°C to 70°C
LTC1710I..... –40°C to 85°C
Junction Temperature** ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

*Supply rails to DATA and CLK are independent of V_{CC} to LTC1710.

**Although the LTC1710 can sustain T_{JMAX} = 125°C without damage, its internal protection circuitry is set to shut down the switches at T_J = 120°C with 15°C hysteresis.

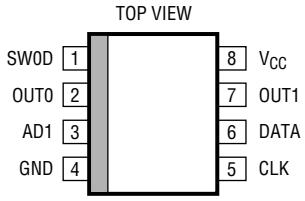
PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 110°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1710CMS8
MS8 PART MARKING
LTDZ



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1710CS8 LTC1710IS8
S8 PART MARKING
1710 1710I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = SW0D = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Operating Supply Voltage Range		●	2.7		5.5	V
I_{VCC}	Supply Current	Charge Pump Off, AD1 High or Low, DATA and CLK High					
		V_{CC} = 5V	●		17	30	µA
		V_{CC} = 3.3V	●		14	30	µA
		V_{CC} = 2.7V	●		11	30	µA
		OUT0 or OUT1 High (Command Byte XXXXXX01 or XXXXXX10)	●		200	300	µA
		Both Outputs High (Command Byte XXXXXX11)	●		250	500	µA
$R_{DS(ON)}$	Power Switch On Resistance	V_{CC} = 2.7V, I_{OUT} = 300mA			0.55		Ω
		V_{CC} = 3.3V, I_{OUT} = 300mA			0.46	0.7	Ω
		V_{CC} = 5V, I_{OUT} = 300mA			0.40	0.6	Ω
V_{UVLO}	Undervoltage Lockout	Falling Edge (Note 2)	●	1.5	2.0	2.5	V
t_{POR}	Power-On Reset Delay Time	V_{CC} = 2.7V (Note 3)			300	1000	µs
		V_{CC} = 5.5V			300	1000	µs
f_{OSC}	Charge Pump Oscillator Frequency (Note 3)				300		kHz

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = SWOD = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Output Turn-On Time (100Ω/1µF Load)	V_{CC} = 2.7V (From ON (Note 6) to V_{OUT} = 90% V_{CC}) V_{CC} = 5.5V (From ON (Note 6) to V_{OUT} = 90% V_{CC})			200 160		µs µs
t_{OFF}	Output Turn-Off Time (100Ω/1µF Load)	V_{CC} = 2.7V (From OFF (Note 7) to V_{OUT} = 10% V_{CC}) V_{CC} = 5.5V (From OFF (Note 7) to V_{OUT} = 10% V_{CC})			250 250		µs µs
V_{IL}	DATA/CLK Input Low Voltage AD1 Input Low Voltage	V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 5.5V	● ●			0.6 0.2	V V
V_{IH}	DATA/CLK High Voltage AD1 Input High Voltage	V_{CC} = 2.7V to 5.5V V_{CC} = 2.7V to 5.5V	● ●	1.4 V_{CC} – 0.2			V V
V_{OL}	Data Output Low Voltage	V_{CC} = 2.7V to 5.5V, $I_{PULL-UP}$ = 350µA	●		0.18	0.4	V
C_{IN}	Input Capacitance (DATA, CLK, AD1)				5		pF
I_{IN}	Input Leakage Current (DATA, CLK)		●			±1	µA
	Input Leakage Current (AD1)		●			±250	nA
SMBus Related Specifications (Note 5)							
f_{SMB}	SMBus Operating Frequency			10		100	kHz
t_{BUF}	Bus Free Time Between Stop and Start			4.7			µs
$t_{SU:STA}$	Start Condition Setup Time			4.7			µs
$t_{HD:STA}$	Start Condition Hold Time			4.0			µs
$t_{SU:STO}$	Stop Condition Setup Time			4.0			µs
$t_{HD: DAT}$	Data Hold Time			300			ns
$t_{SU:DAT}$	Data Setup Time			250			ns
t_{LOW}	Clock Low Period			4.7			µs
t_{HIGH}	Clock High Period			4.0		50	µs
t_f	Clock/Data Fall Time					300	ns
t_r	Clock/Data Rise Time					1000	ns
$I_{PULL-UP}$	Current Through External Pull-Up Resistor on DATA Pin	V_{CC} = 2.7V to 5.5V (Open-Drain Data Pull-Down Current Capacity)		100		350	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Approximately 3% hysteresis is provided to ensure stable operation and eliminate false triggering by minor V_{CC} glitches.

Note 3: Measured from V_{CC} > V_{UVLO} to SMBus ready for DATA input.

Note 4: The oscillator frequency is not tested directly but is inferred from turn-on time.

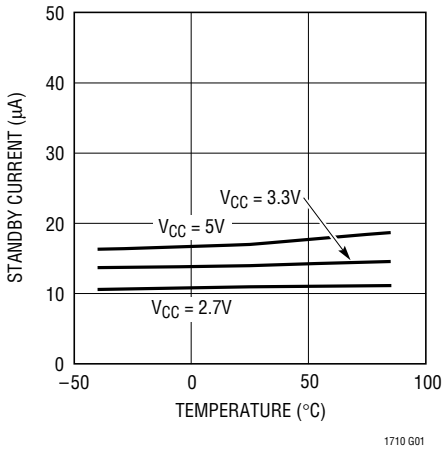
Note 5: SMBus timing specifications are guaranteed but not tested.

Note 6: ON is enabled upon receiving the Stop condition from the SMBus master.

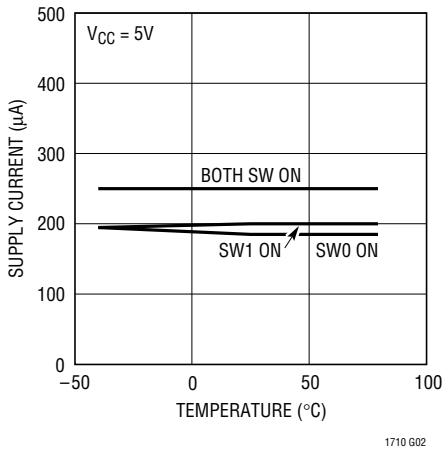
Note 7: OFF is enabled upon receiving the Stop condition from the SMBus master.

TYPICAL PERFORMANCE CHARACTERISTICS

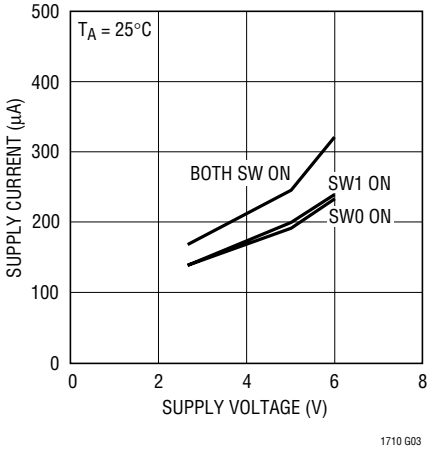
Standby Current vs Temperature



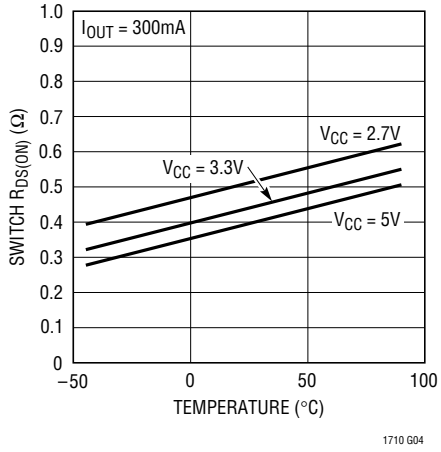
Supply Current (I_Q) vs Temperature



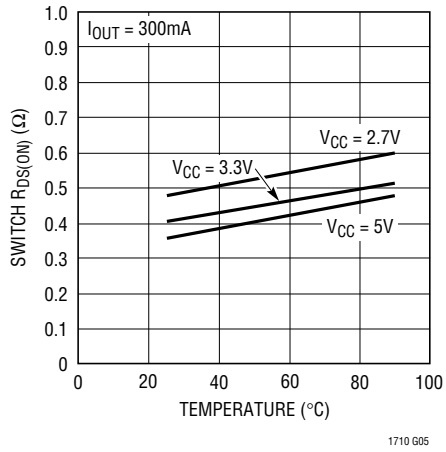
Supply Current (I_Q) vs Supply Voltage



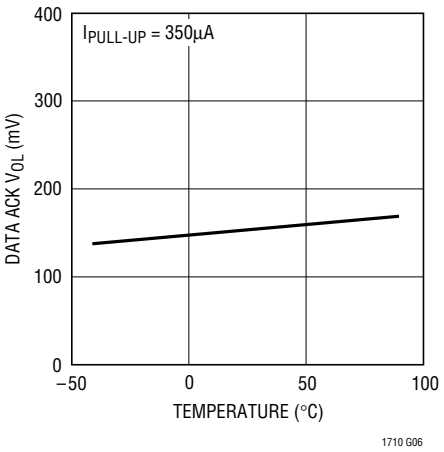
Switch $R_{DS(ON)}$ vs Temperature (SO-8 Package)



Switch $R_{DS(ON)}$ vs Temperature (MSOP Package)



Data ACK V_{OL} vs Temperature



PIN FUNCTIONS

SW0D (Pin 1): Drain Supply of Switch 0. User-programmable from 0V to V_{CC}.

OUT0 (Pin 2): Source Output of Switch 0. Maximum load of 300mA; controlled by LSB of command byte.

AD1 (Pin 3): Three-State Programmable Address Pin. Must be connected directly to V_{CC}, GND or $V_{CC}/2$ (using two resistors ≤1M). Do not float this pin.

GND (Pin 4): Ground Connection.

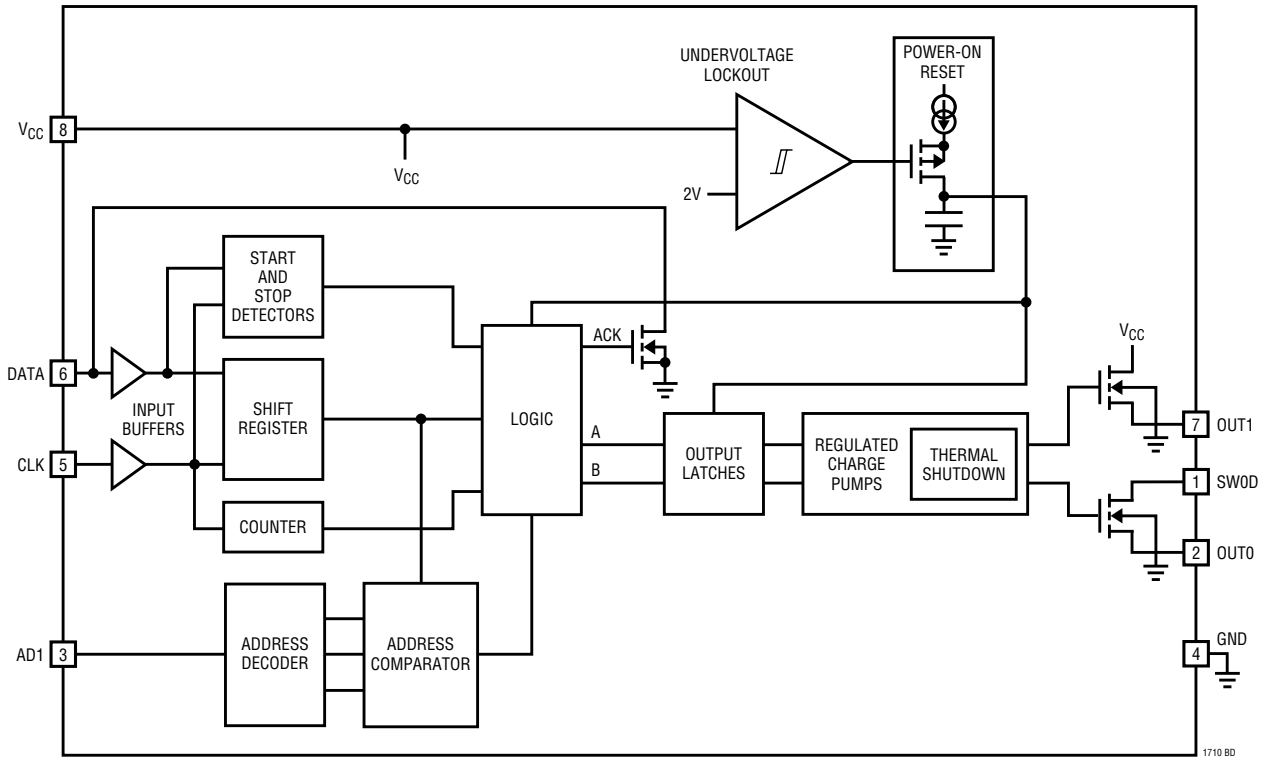
CLK (Pin 5): Serial Clock Interface. Must be pulled high to V_{CC} with external resistor. The pull-up current must be limited to 350µA.

DATA (Pin 6): Open-Drain Connected Serial Data Interface. Must be pulled high to V_{CC} with external resistor. The pull-up current must be limited to 350µA.

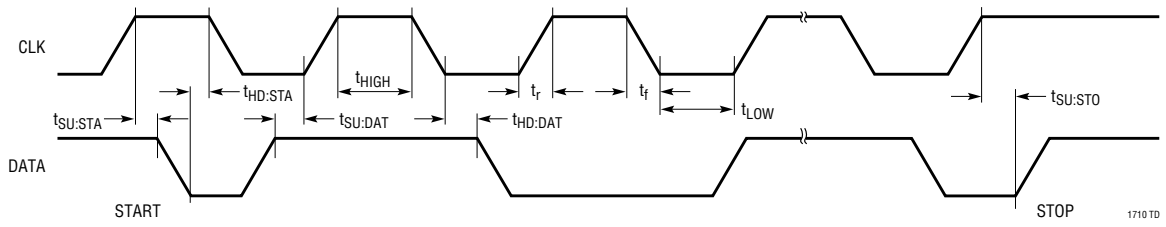
OUT1 (Pin 7): Source Output of Switch 1. Maximum load of 300mA; controlled by 2nd LSB of command byte.

V_{CC} (Pin 8): Input Supply Voltage. Operating range from 2.7V to 5.5V.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

SMBus Operation

SMBus is a serial bus interface that uses only two bus lines, DATA and CLK, to control low power peripheral devices in portable equipment. It consists of masters, also known as hosts, and slave devices. The master of the SMBus is always the one to initiate communications to the slave devices by varying the status of the DATA and CLK lines. The SMBus specification establishes a set of protocols that devices on the bus must follow for communications.

The protocol that the LTC1710 uses is the Send Byte Protocol. In this protocol, the master first sends out a Start signal by switching the DATA line from high to low while CLK is high. (Because there may be more than one master on the same bus, an arbitration process takes place if two masters attempt to take control of the DATA line simultaneously; the first master that outputs a one while the other master is zero loses the arbitration and becomes a slave itself.) Upon detecting this Start signal, all slave devices on the bus wake up and prepare to shift in the next byte of data.

OPERATION

The master then sends out the first byte. The first seven bits of this byte consist of the address of the device that the master wishes to communicate with. The last bit indicates whether the command will be a read (logic one) or write (logic zero). Because the LTC1710 is a slave device that can only be written to by a master, it will ignore the ensuing commands of the master if it wants to read from the LTC1710, even if the address sent by the master matches that of the LTC1710. After reception of the first byte, the slave device (LTC1710) with the matching address then acknowledges the master by pulling the DATA line low before the next rising clock edge.

By now all other nonmatching slave devices will have gone back to their original standby states to wait for the next Start signal. Meanwhile, upon receiving the acknowledge from the matching slave, the master then sends out the command byte (see Table 1).

Table 1. Switch Control Table

COMMAND	XXXXXX00	XXXXXX01	XXXXXX10	XXXXXX11
Switch 0	SW0 Off	SW0 On	SW0 Off	SW0 On
Switch 1	SW1 Off	SW1 Off	SW1 On	SW1 On

After receiving the command byte, the slave device (LTC1710) needs to acknowledge the master again by pulling the DATA line low on the following clock cycle. The master then ends this Send Byte Protocol by sending the Stop signal, which is a transition from low to high on the DATA line while the CLK line is high. Valid data is shifted into the output latch on the last acknowledge signal; the output switch will not turn on, however, until the Stop signal is detected. This double buffering feature of the output latch allows the user to "daisy-chain" multiple SMBus devices such that their outputs are synchronously executed on the Stop signal despite the fact that valid data were loaded into their output latches at different times. An example is shown in Figure 1. If somehow either the Start or the Stop signal is detected in the middle of a byte, the slave device (LTC1710) will regard this as an error and reject all previous data.

Address

The LTC1710 has an address of 10110XX; the five MSBs are hardwired, but the two LSBs are programmable by the user with the help of a three-state address pin. Refer to Table 2 for the pin configurations and their corresponding addresses.

Table 2. Address Pin Truth Table

AD1	ADDRESS
GND	1011000
$V_{CC}/2$	1011001
V_{CC}	1011010

To conserve standby current, it is preferable to tie the address pins to either V_{CC} or GND. If three LTC1710s are needed, then the address pin can be tied to the third state of $V_{CC}/2$ by using two equal value resistors (≤1M), see Figure 2.

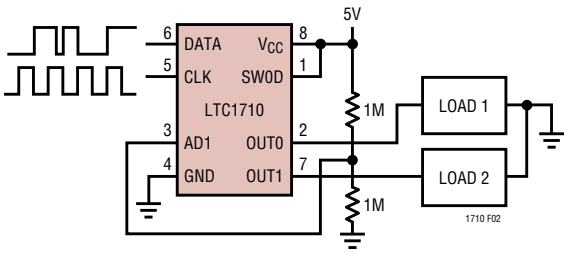
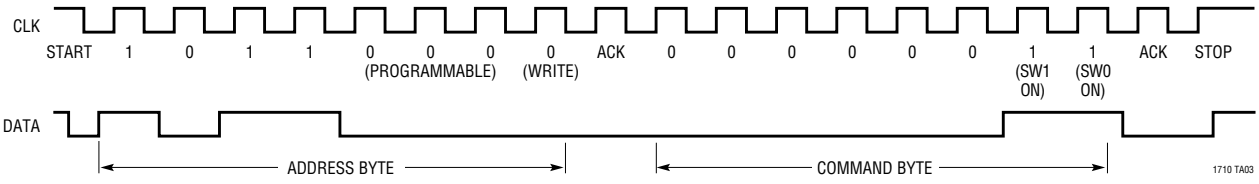


Figure 2. The LTC1710 Programmed with Address 1011001

Figure 1. Daisy-Chain Example

Example of Send Byte Protocol to Slave Address 1011000 Turning SW0 and SW1 On



OPERATION

Charge Pump

To fully enhance the internal N-channel power switches, an internal charge pump is used to boost the gate drive to a maximum of 6V above V_{CC}. The reason for the maximum charge pump output voltage limit is to protect the internal switches from excessive gate overdrive. A feedback network is used to limit the charge pump output once it is 6V above V_{CC}. To prevent the power switches from turning on too fast, an internal current source is placed between the output of the charge pump and the gate of the power switch to control the ramp rate.

Since the charge pumps are driving just the gates of the internal switches, only a small amount of current is required. Therefore, all the charge pump capacitors are integrated onboard. The drain of switch 1 is internally connected to V_{CC}, however, the drain of switch 0 is user controlled through Pin 1. In other words, SMBus devices using different power supply voltages can be simultaneously switched by the same LTC1710.

Power-On Reset and Undervoltage Lockout

The LTC1710 starts up with both gate drives low. An internal power-on reset (POR) signal inhibits operation until about 300µs after V_{CC} crosses the undervoltage lockout threshold (typically 2V). The circuit includes some hysteresis and delay to avoid nuisance resets. Once operation begins, V_{CC} must drop below the threshold for at least 100µs to trigger another POR sequence.

Input Threshold

Anticipating the trend of lower and lower supply voltages, the SMBus is specified with a V_{IH} of 1.4V and a V_{IL} of 0.6V. While some SMBus parts may violate this stringent SMBus specification by specifying a higher V_{IH} value for a corresponding higher input supply voltage, the LTC1710 meets and maintains the constant SMBus input threshold specification throughout the entire supply voltage range of 2.7V to 5.5V.

Thermal Shutdown

In the unlikely event that either power switch overheats, a thermal shutdown circuit, which is placed closely to the two switches, will activate and turn off the gate drives to both switches. The thermal shutdown circuit has a threshold of 120°C with a 15°C hysteresis.

TYPICAL APPLICATIONS

The LTC1710, when used with the LT®1521-3.3, can switch a regulated 3.3V/300mA supply to a load (Figure 3). Also, with the help of the LT1304-5, the LTC1710 can be used to make a boost switching regulator with output disconnect and a low standby current of 22µA (Figure 5).

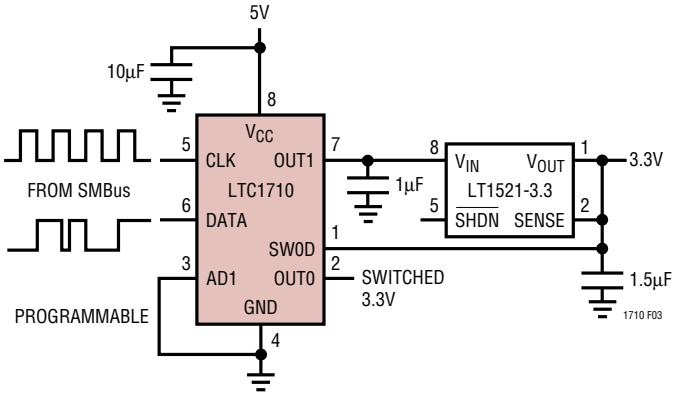


Figure 3. Low Dropout Regulator Switching a 3.3V/300mA Supply

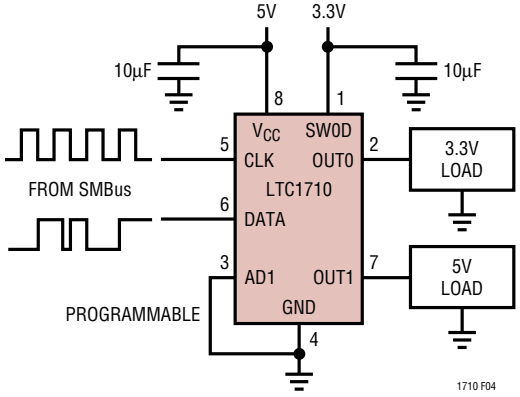


Figure 4. The LTC1710 Switching Two Different Voltage Loads

TYPICAL APPLICATIONS

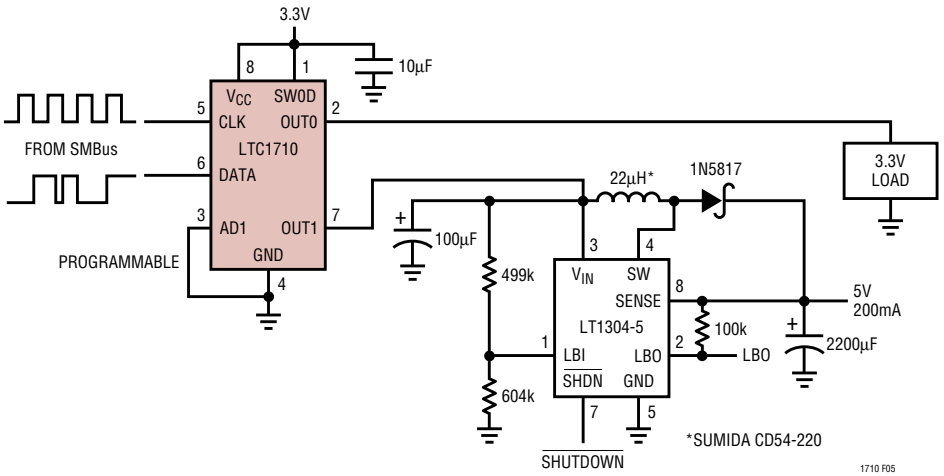
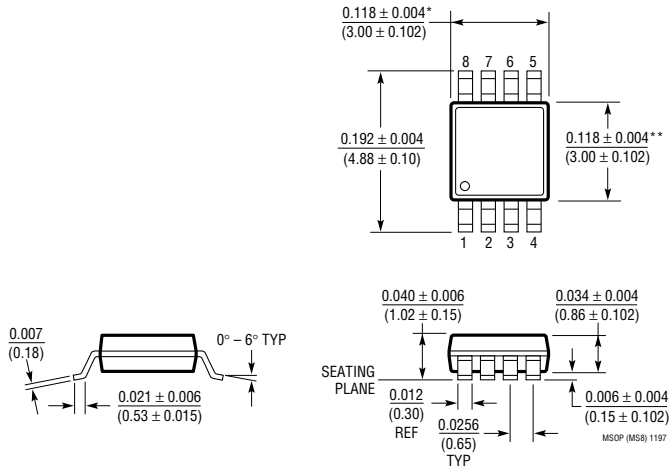


Figure 5. Switching Regulator with Low-Battery Detect Using 22µA of Standby Current

PACKAGE DESCRIPTION

Dimensions in inches (millimeters), unless otherwise noted.

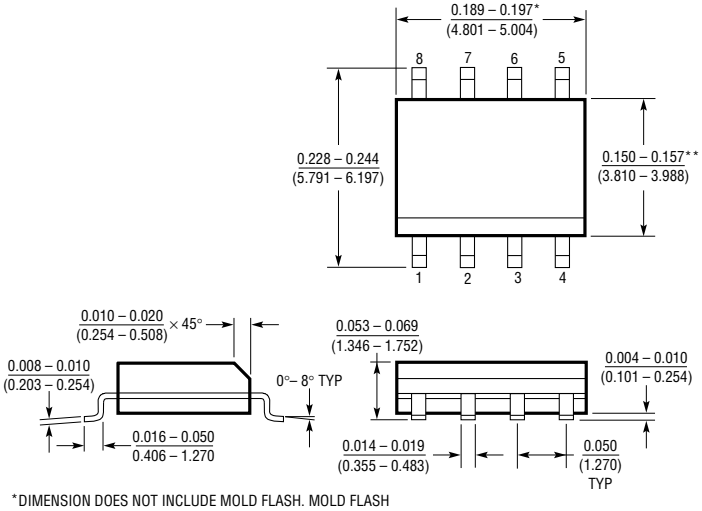
MS8 Package
8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1304	Micropower DC/DC Converter	Low-Battery Detector Active in Shutdown
LTC1470/LTC1471	Single and Dual PCMCIA Protected 3.3V/5V V_{CC} Switches	Current Limit
LTC1473	Dual PowerPath™ Switch Matrix	Current Limit with Timer
LTC1623	SMBus Dual High Side Switch Controller	Uses External Switches, Two Three-State Address Pins

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