

# MTD5P06V

Preferred Device

## Power MOSFET 5 A, 60 V, P-Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

### Features

- Avalanche Energy Specified
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature
- Pb-Free Packages are Available

**MAXIMUM RATINGS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	Vdc
Drain-to-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-to-Source Voltage – Continuous – Non-repetitive ( $t_p \leq 10 \text{ ms}$ )	$V_{GS}$ $V_{GSM}$	$\pm 15$ $\pm 25$	Vdc Vpk
Drain Current – Continuous @ $25^\circ\text{C}$ – Continuous @ $100^\circ\text{C}$ – Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_D$ $I_D$ $I_{DM}$	5 4 18	Adc Adc Apk
Total Power Dissipation @ $25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 0.27	W W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)		2.1	W
Operating and Storage Temperature Range	$T_J$ , $T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , Peak $I_L = 5 \text{ Apk}$ , $L = 10 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	125	mJ
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.75 100 71.4	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR-4 board using the 0.5 sq in drain pad size.

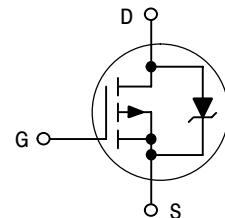


**ON Semiconductor®**

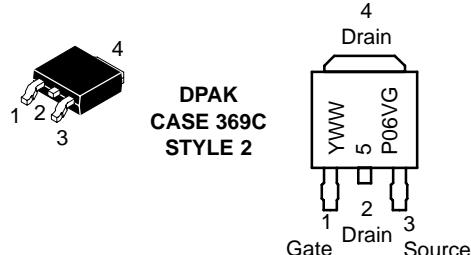
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
60 V	340 m $\Omega$	5.0 A

### P-Channel



### MARKING DIAGRAM



Y = Year  
WW = Work Week  
5P06V = Device Code  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MTD5P06V	DPAK	75 Units/Rail
MTD5P06VT4	DPAK	2500/Tape & Reel
MTD5P06VT4G	DPAK (Pb-Free)	2500/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**Preferred** devices are recommended choices for future use and best overall value.

# MTD5P06V

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-Source Breakdown Voltage ( $V_{GS} = 0 \text{ Vdc}$ , $I_D = 0.25 \text{ mA}$ )	$V_{(BR)DSS}$	60 —	— 61.2	— —	Vdc $\text{mV}/^\circ\text{C}$
Temperature Coefficient (Positive)					
Zero Gate Voltage Drain Current ( $V_{DS} = 60 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc}$ ) ( $V_{DS} = 60 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc}$ , $T_J = 150^\circ\text{C}$ )	$I_{DSS}$	— —	— —	10 100	$\mu\text{A}$
Gate-Body Leakage Current ( $V_{GS} = \pm 15 \text{ Vdc}$ , $V_{DS} = 0 \text{ Vdc}$ )	$I_{GSS}$	—	—	100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$ ) Threshold Temperature Coefficient (Negative)	$V_{GS(\text{th})}$	2.0 —	2.8 4.7	4.0 —	Vdc $\text{mV}/^\circ\text{C}$
Static Drain-Source On-Resistance ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 2.5 \text{ A}$ )	$R_{DS(\text{on})}$	—	0.34	0.45	$\Omega$
Drain-Source On-Voltage ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 5 \text{ A}$ ) ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 2.5 \text{ A}$ , $T_J = 150^\circ\text{C}$ )	$V_{DS(\text{on})}$	— —	— —	2.7 2.6	Vdc
Forward Transconductance ( $V_{DS} = 15 \text{ Vdc}$ , $I_D = 2.5 \text{ A}$ )	$g_{FS}$	1.5	3.6	—	Mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$C_{iss}$	—	367	510	pF
Output Capacitance		$C_{oss}$	—	140	200	
Transfer Capacitance		$C_{rss}$	—	29	60	

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{DD} = 30 \text{ Vdc}$ , $I_D = 5 \text{ A}$ , $V_{GS} = 10 \text{ Vdc}$ , $R_G = 9.1 \Omega$ )	$t_{d(\text{on})}$	—	11	20	ns
Rise Time		$t_r$	—	26	50	
Turn-Off Delay Time		$t_{d(\text{off})}$	—	17	30	
Fall Time		$t_f$	—	19	40	
Gate Charge (See Figure 8)	$(V_{DS} = 48 \text{ Vdc}$ , $I_D = 5 \text{ A}$ , $V_{GS} = 10 \text{ Vdc}$ )	$Q_T$	—	12	20	nC
		$Q_1$	—	3.0	—	
		$Q_2$	—	5.0	—	
		$Q_3$	—	5.0	—	

## SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 5 \text{ A}$ , $V_{GS} = 0 \text{ Vdc}$ ) $(I_S = 5 \text{ A}$ , $V_{GS} = 0 \text{ Vdc}$ , $T_J = 150^\circ\text{C}$ )	$V_{SD}$	— —	1.72 1.34	3.5 —	Vdc	
Reverse Recovery Time		$t_{rr}$	—	97	—	ns	
$(I_S = 5 \text{ A}$ , $V_{GS} = 0 \text{ Vdc}$ , $dI_S/dt = 100 \text{ A}/\mu\text{s}$ )		$t_a$	—	73	—		
		$t_b$	—	24	—		
		$Q_{RR}$	—	0.42	—		
						$\mu\text{C}$	

## INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)	$L_D$	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	$L_S$	—	7.5	—	nH

3. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

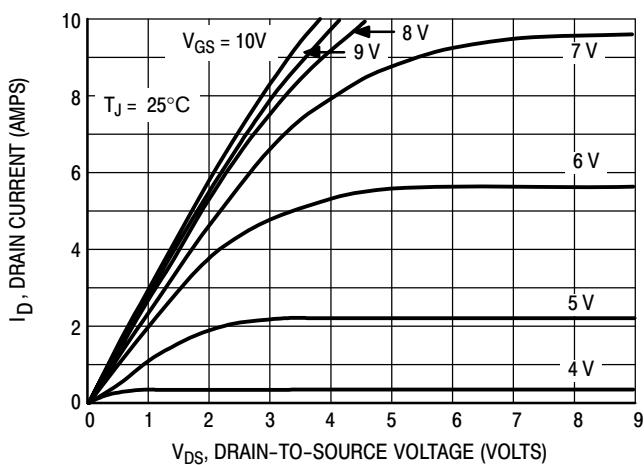


Figure 1. On-Region Characteristics

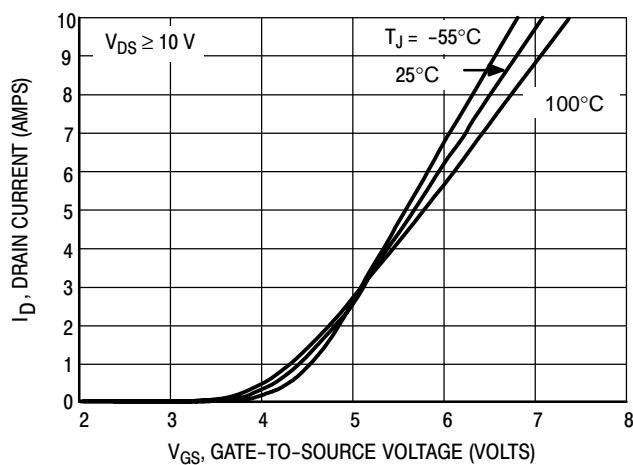


Figure 2. Transfer Characteristics

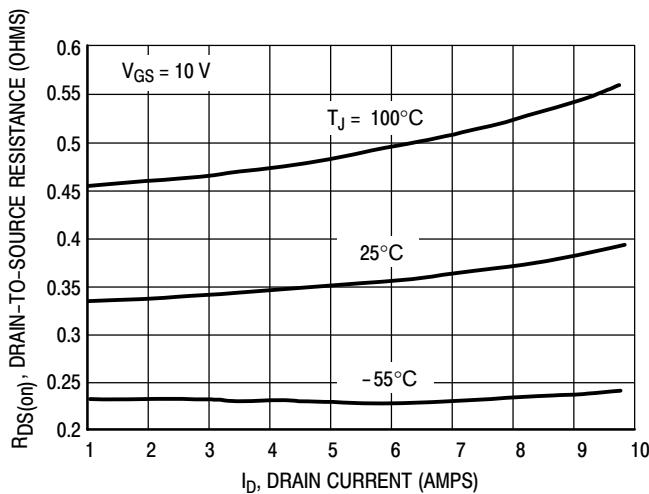


Figure 3. On-Resistance versus Drain Current and Temperature

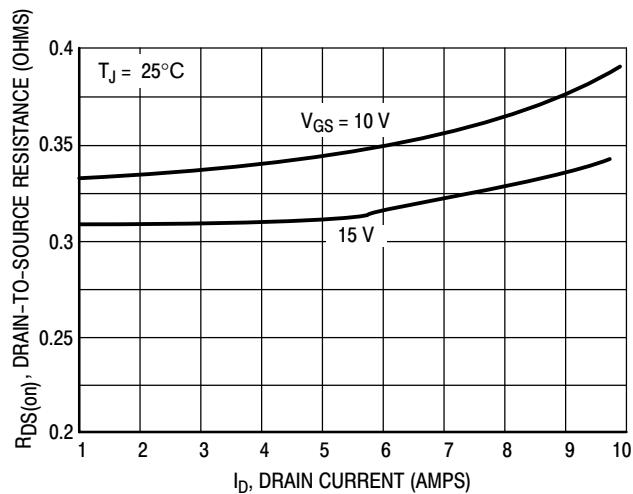


Figure 4. On-Resistance versus Drain Current and Gate Voltage

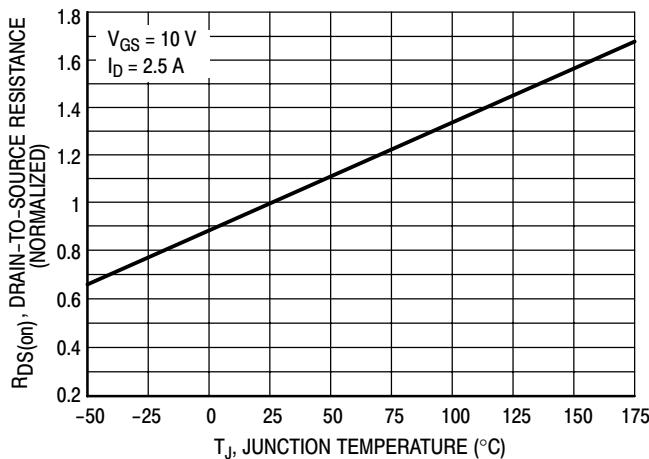


Figure 5. On-Resistance Variation with Temperature

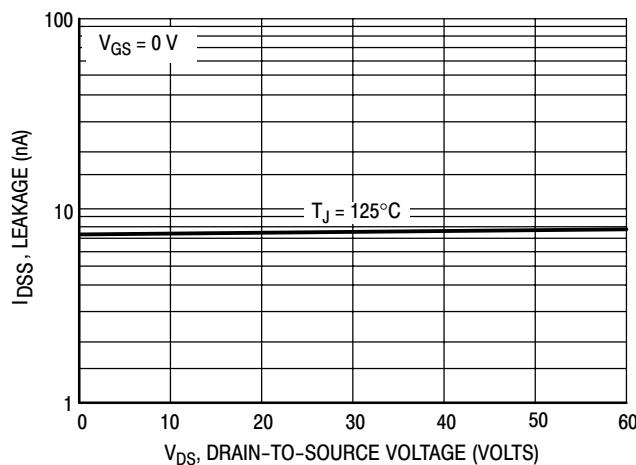


Figure 6. Drain-to-Source Leakage Current versus Voltage

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ( $\Delta t$ ) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain-gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ( $I_{G(AV)}$ ) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load,  $V_{GS}$  remains virtually constant at a level known as the plateau voltage,  $V_{GSP}$ . Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G / (V_{GG} - V_{GSP})$$

$$t_f = Q_2 \times R_G / V_{GSP}$$

where

$V_{GG}$  = the gate drive voltage, which varies from zero to  $V_{GG}$

$R_G$  = the gate drive resistance

and  $Q_2$  and  $V_{GSP}$  are read from the gate charge curve.

During the turn-on and turn-off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$$

$$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$$

The capacitance ( $C_{iss}$ ) is read from the capacitance curve at a voltage corresponding to the off-state condition when calculating  $t_{d(on)}$  and is read at a voltage corresponding to the on-state when calculating  $t_{d(off)}$ .

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by  $Ldi/dt$ , but since  $di/dt$  is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

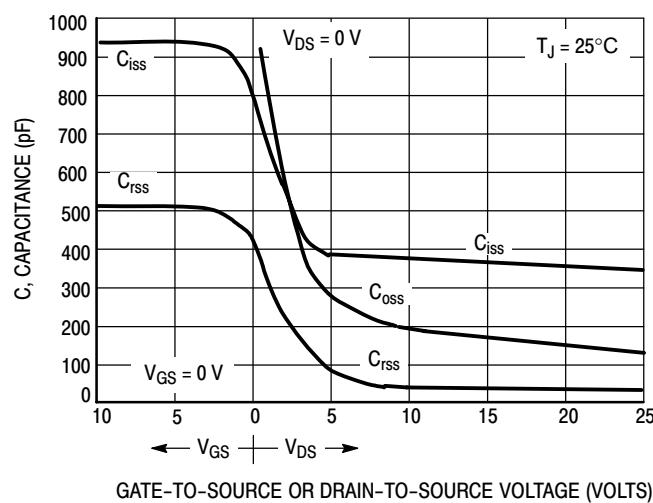
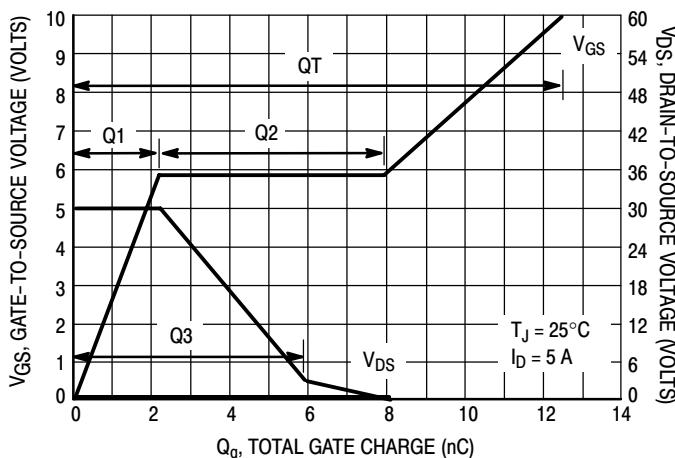
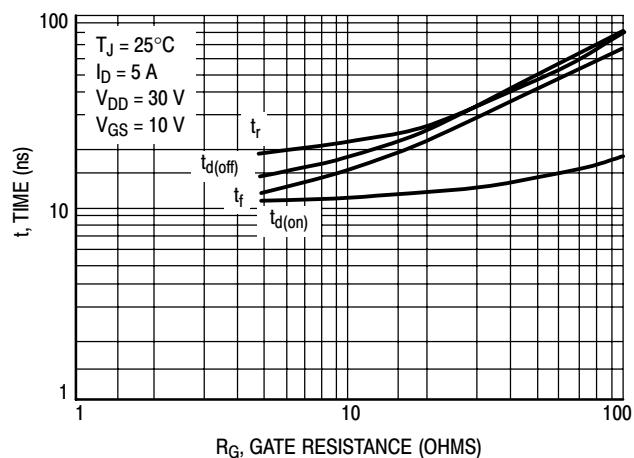


Figure 7. Capacitance Variation

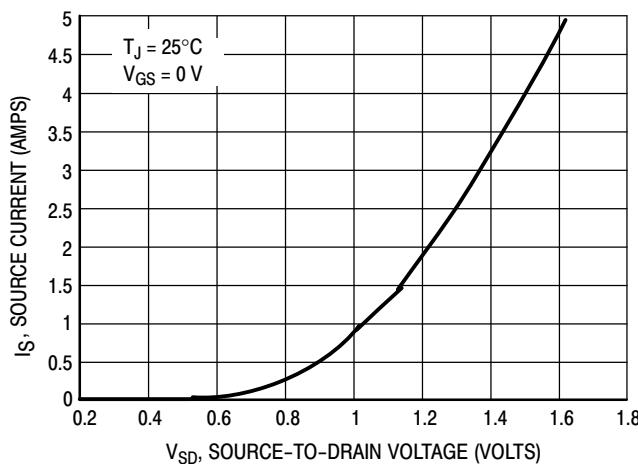


**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance-General Data and Its Use."

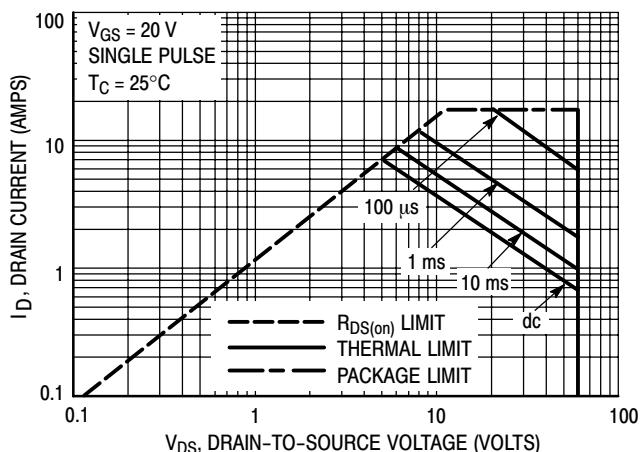
Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded and the transition time ( $t_r, t_f$ ) do not exceed 10  $\mu$ s. In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(MAX)} - T_C)/(R_{\theta JC})$ .

A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For

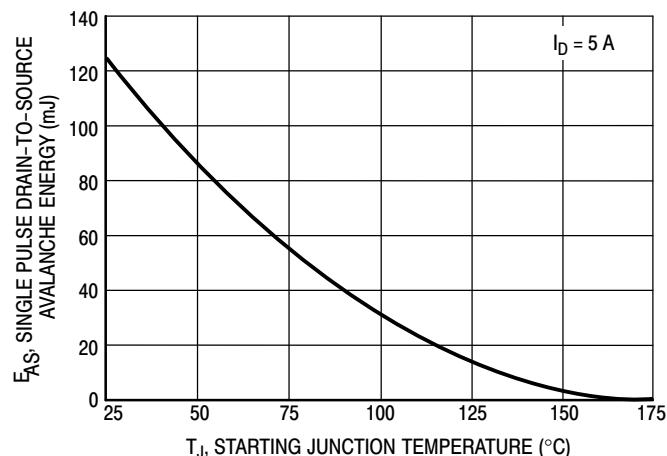
reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

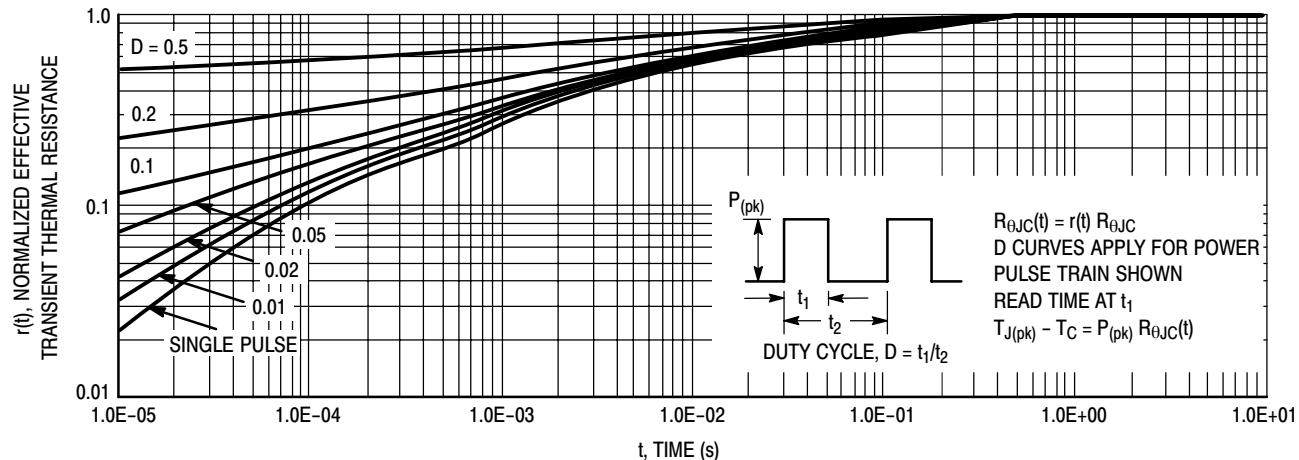
## SAFE OPERATING AREA



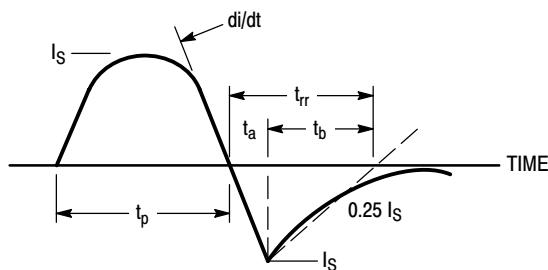
**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



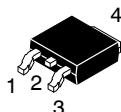
**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**



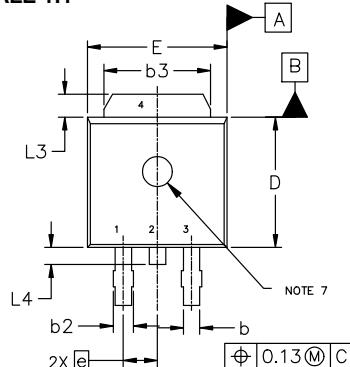
**Figure 13. Thermal Response**



**Figure 14. Diode Reverse Recovery Waveform**



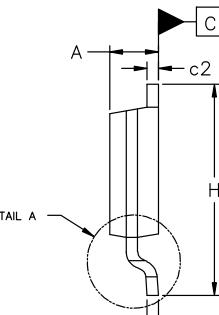
SCALE 1:1



TOP VIEW

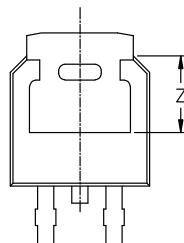
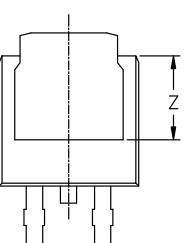
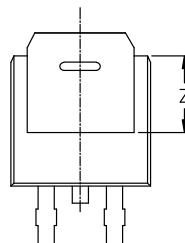
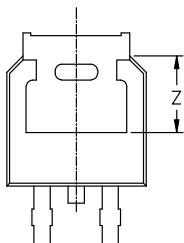
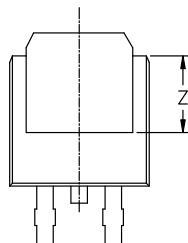
**DPAK3 6.10x6.54x2.28, 2.29P**  
CASE 369C  
ISSUE J

DATE 12 AUG 2025



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29	2.29 BSC	
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

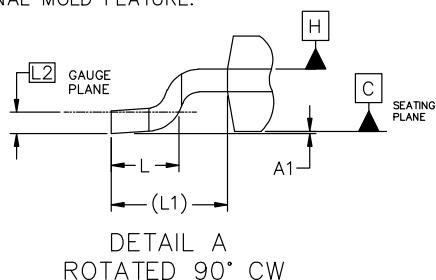
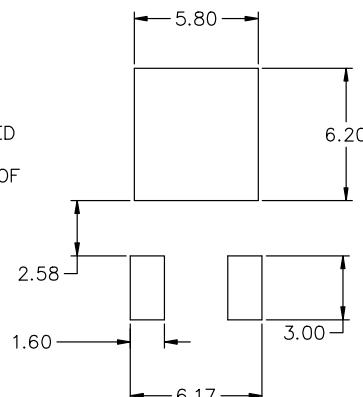


BOTTOM VIEW

ALTERNATE CONSTRUCTIONS

## NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DETAIL A  
ROTATED 90° CW

RECOMMENDED MOUNTING FOOTPRINT\*

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

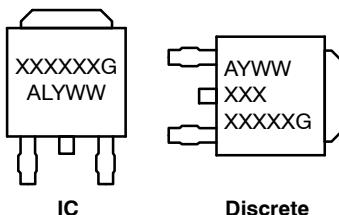
DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

onsemi and Onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**DPAK3 6.10x6.54x2.28, 2.29P**  
**CASE 369C**  
**ISSUE J**

DATE 12 AUG 2025

## GENERIC MARKING DIAGRAM\*



XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. BASE	STYLE 2: PIN 1. GATE	STYLE 3: PIN 1. ANODE	STYLE 4: PIN 1. CATHODE	STYLE 5: PIN 1. GATE
2. COLLECTOR	2. DRAIN	2. CATHODE	2. ANODE	2. ANODE
3. Emitter	3. SOURCE	3. ANODE	3. GATE	3. CATHODE
4. COLLECTOR	4. DRAIN	4. CATHODE	4. ANODE	4. ANODE

STYLE 6: PIN 1. MT1	STYLE 7: PIN 1. GATE	STYLE 8: PIN 1. N/C	STYLE 9: PIN 1. ANODE	STYLE 10: PIN 1. CATHODE
2. MT2	2. COLLECTOR	2. CATHODE	2. CATHODE	2. ANODE
3. GATE	3. Emitter	3. ANODE	3. RESISTOR ADJUST	3. CATHODE
4. MT2	4. COLLECTOR	4. CATHODE	4. CATHODE	4. ANODE

<b>DOCUMENT NUMBER:</b>	<b>98AON10527D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DPAK3 6.10x6.54x2.28, 2.29P</b>	<b>PAGE 2 OF 2</b>

**onsemi** and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

**onsemi**, **ONSEMI**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)

