



**DUAL CHANNEL, HIGH CMR, VERY
HIGH SPEED OPTICALLY COUPLED
ISOLATOR LOGIC GATE OUTPUT**

APPROVALS

- UL recognised, File No. E91231

DESCRIPTION

The ICPL2630 / ICPL2631 are dual channel optocouplers consisting of GaAsP light emitting diodes and high gain integrated photo detectors to provide 3500Volts_{RMS} electrical isolation between input and output. The output of the detector I.C.'s are open collector Schottky clamped transistors. The ICPL2631 has an internal shield which provides a guaranteed common mode transient immunity specification of 1000V/μs minimum. This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The coupled parameters are guaranteed over the temperature range of 0°C to 70°C, such that a maximum input signal of 5mA will provide a minimum output sink current of 13mA (equivalent to fan-out of eight gates)

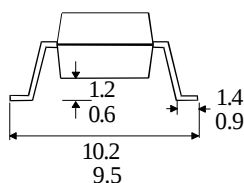
FEATURES

- High speed - 10MBit/s
- High Common Mode Transient Immunity 10kV/μs typical
- Logic gate output
- ICPL2631 has improved noise shield for superior common mode rejection
- Options :-
10mm lead spread - add G after part no.
Surface mount - add SM after part no.
Tape&reel - add SMT&R after part no.

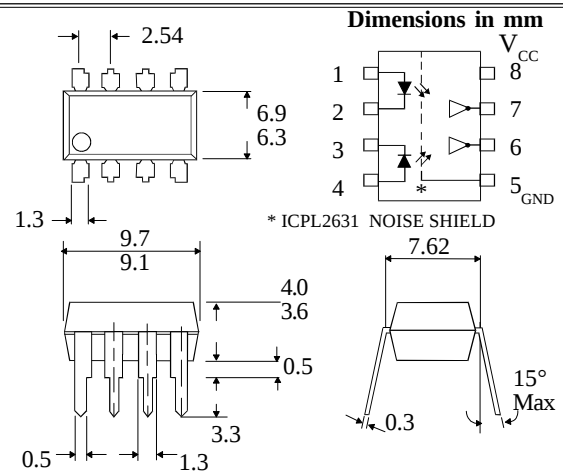
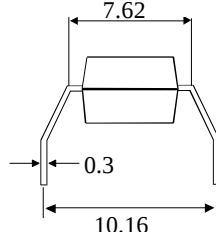
APPLICATIONS

- Line receiver, data transmission
- Computer-peripheral interface
- Data multiplexing
- Pulse transformer replacement

**OPTION SM
SURFACE MOUNT**



OPTION G



**ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise specified)**

Storage Temperature _____ -55°C to + 125°C
Operating Temperature _____ 0°C to + 70°C
Lead Soldering Temperature
(1/16 inch (1.6mm) from case for 10 secs) 260°C

INPUT DIODE

Average Forward Current _____ 15mA
(note 5)
Peak Forward Current _____ 30mA
(less than 1msec duration)(note 5)
Reverse Voltage _____ 5V
(note 5)

DETECTOR

Supply Voltage(V_{CC}) _____ 7V
(1 minute maximum)
Output Current (I_O) _____ 16mA
(note 5)
Output Voltage (V_O) _____ 7V
(note 5)
Collector Output Power Dissipation _____ 60mW

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ELECTRICAL CHARACTERISTICS ($T_A = 0^{\circ}\text{C}$ to 70°C Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP*	MAX	UNITS	TEST CONDITION
High Level Output Current (note 5)	I_{OH}			2	250	μA	$V_{CC} = 5.5\text{V}$, $V_O = 5.5\text{V}$ $I_F = 250\mu\text{A}$
Low Level Output Voltage (note 5)	V_{OL}			0.4	0.6	V	$V_{CC} = 5.5\text{V}$, $I_F = 5\text{mA}$ I_{OL} (sinking) = 13mA
High Level Supply Current (both channels)	I_{CCH}			14	30	mA	$V_{CC} = 5.5\text{V}$, $I_F = 0\text{mA}$
Low Level Supply Current (both channels)	I_{CCL}			26	36	mA	$V_{CC} = 5.5\text{V}$, $I_F = 10\text{mA}$
Input Forward Voltage	V_F			1.55	1.75	V	$I_F = 10\text{mA}$, $T_A = 25^{\circ}\text{C}$
Input Reverse Breakdown Voltage	V_{BR}		5			V	$I_R = 10\mu\text{A}$, $T_A = 25^{\circ}\text{C}$
Input Capacitance	C_{IN}			60		pF	$V_F = 0$, $f = 1\text{MHz}$
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.4		mV/ $^{\circ}\text{C}$	$I_F = 10\text{mA}$
Input-output Isolation Voltage (note 4)	V_{ISO}		2500	5000		V_{RMS}	R.H.equal to or less than 50%, $t = 1\text{min}$. $T_A = 25^{\circ}\text{C}$
Input-output Insulation Leakage Current (note 4)	I_{I-O}				1	μA	R.H = 45% $t = 5\text{s}$, $T_A = 25^{\circ}\text{C}$ $V_{I-O} = 3000\text{V dc}$
Resistance (Input to Output) (note 4)	R_{I-O}			10^{12}		Ω	$V_{I-O} = 500\text{V dc}$
Capacitance (Input to Output) (note 4)	C_{I-O}			0.6		pF	$f = 1\text{MHz}$
Input-input Insulation Leakage Current (note 6)	I_{I-I}			0.005		μA	R.H = 45% $t = 5\text{s}$, $T_A = 25^{\circ}\text{C}$ $V_{I-O} = 500\text{V dc}$
Resistance (Input to input) (note 6)	R_{I-I}			10^{11}		Ω	$V_{I-O} = 500\text{V dc}$
Capacitance (Input to input) (note 6)	C_{I-I}			0.6		pF	$f = 1\text{MHz}$

* All typicals at $T_A = 25^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	$^{\circ}\text{C}$

*6.3mA is a guard banded
value which allows for at least
20% CTR degradation.
Initial input current threshold
value is 5.0mA or less

SWITCHING SPECIFICATIONS AT $T_A = 25^\circ\text{C}$ ($V_{CC} = 5\text{V}$, $I_F = 7.5\text{mA}$ Unless otherwise noted)

PARAMETER	SYM	DEVICE	MIN	TYP	MAX	UNITS	TEST CONDITION
Propagation Delay Time to Logic Low at Output (fig 1)(note2)	t_{PHL}			55	75	ns	$R_L = 350\Omega$, $C_L = 15\text{pF}$
Propagation Delay Time to Logic High at Output (fig 1)(note3)	t_{PLH}			45	75	ns	$R_L = 350\Omega$, $C_L = 15\text{pF}$
Common Mode Transient Immunity at Logic High Level Output (fig 2)(note7)	CM_H	ICPL2630 ICPL2631	1000	10000 10000		V/ μs V/ μs	$I_F = 0\text{mA}$, $V_{CM} = 50V_{PP}$ $R_L = 350\Omega$, $V_{OH} = 2V_{min.}$
Common Mode Transient Immunity at Logic Low Level Output (fig 2)(note8)	CM_L	ICPL2630 ICPL2631	-1000	-10000 -10000		V/ μs V/ μs	$V_{CM} = 50V_{PP}$ $R_L = 350\Omega$, $V_{OL} = 0.8V_{max.}$

NOTES:-

- 1 Bypassing of the power supply line is required, with a $0.01\mu\text{F}$ ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolator(s) should be separate from the bus for any active loads. Otherwise a larger value of bypass capacitor (up to $0.1\mu\text{F}$) may be needed to suppress regenerative feedback via the power supply.
- 2 The t_{PHL} propagation delay is measured from the 3.75mA level Low to High transition of the input current pulse to the 1.5V level on the High to Low transition of the output voltage pulse.
- 3 The t_{PLH} propagation delay is measured from the 3.75mA level High to Low transition of the input current pulse to the 1.5V level on the Low to High transition of the output voltage pulse.
- 4 Device considered a two terminal device; pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
- 5 Each channel.
- 6 Measured between pins 1 and 2 shorted together and pins 3 and 4 shorted together.
- 7 CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (ie $V_{out} > 2.0\text{V}$).
- 8 CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (ie $V_{out} < 0.8\text{V}$)

FIG.1 SWITCHING TEST CIRCUIT

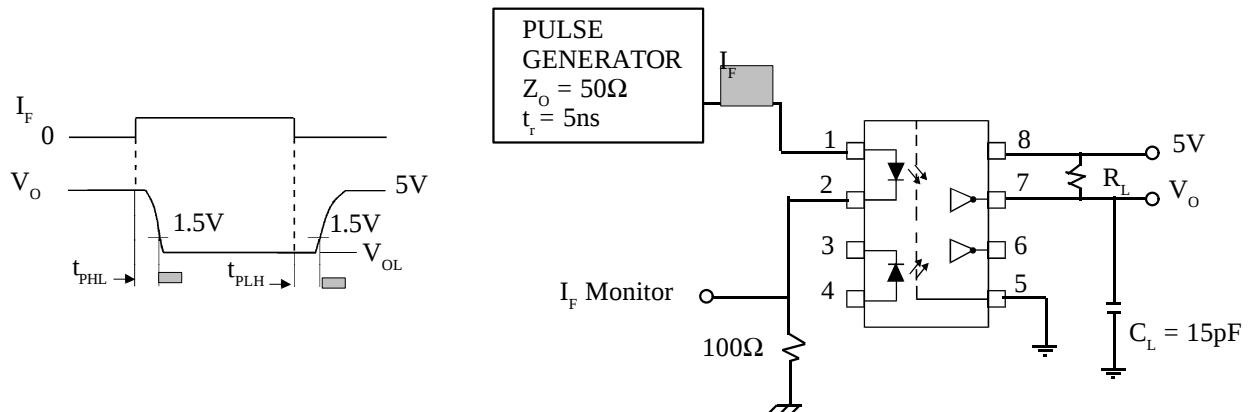


FIG. 2 TEST CIRCUIT FOR TRANSIENT IMMUNITY AND TYPICAL WAVEFORMS

