



DualCool™ N-Channel NexFET™ Power MOSFET

Check for Samples: [CSD16407Q5C](#)

FEATURES

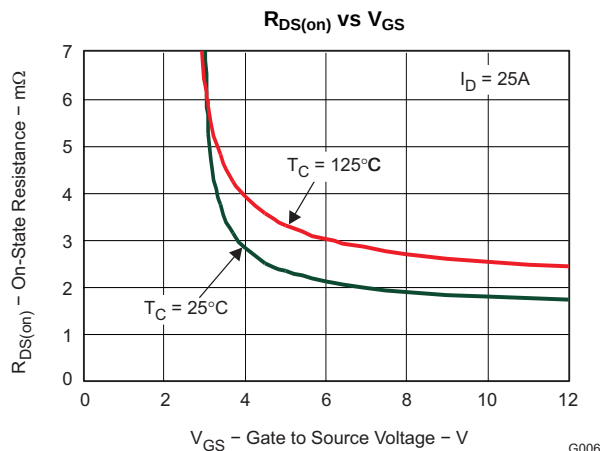
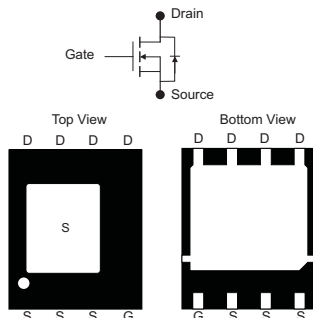
- Ultralow Q_g and Q_{gd}
- DualCool™ Package
- Optimized for Two Sided Cooling
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25	V
Q_g	Gate Charge Total (4.5V)	13.3	nC
Q_{gd}	Gate Charge Gate to Drain	3.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V$	2.5 mΩ
		$V_{GS} = 10V$	1.8 mΩ
V_{th}	Threshold Voltage	1.6	V

ORDERING INFORMATION

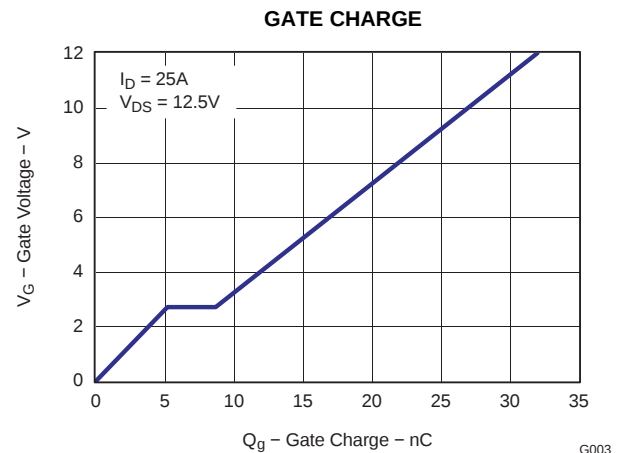
Device	Package	Media	Qty	Ship
CSD16407Q5C	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ C$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / -12	V
I_D	Continuous Drain Current, $T_C = 25^\circ C$	100	A
	Continuous Drain Current ⁽¹⁾	31	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ C$ ⁽²⁾	200	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$
E_{AS}	Avalanche Energy, single pulse $I_D = 66A, L = 0.1mH, R_G = 25\Omega$	218	mJ

(1) Typical $R_{\theta JA} = 40^\circ C/W$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu s$, duty cycle $\leq 2\%$



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Characteristics							
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	25			V	
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V	1			μA	
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +16V / −12V	100			nA	
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	1.3	1.6	1.9	V	
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _D = 25A	2.5			3.3	mΩ
		V _{GS} = 10V, I _D = 25A	1.8			2.4	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 25A	111			S	
Dynamic Characteristics							
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 12.5V , f = 1MHz	2040			2660	pF
C _{OSS}	Output Capacitance		1600			2080	pF
C _{RSS}	Reverse Transfer Capacitance		115			160	pF
R _g	Series Gate Resistance		1.2			2.4	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 12.5V, I _D = 25A	13.3			18	nC
Q _{gd}	Gate Charge Gate to Drain		3.5				nC
Q _{gs}	Gate Charge Gate to Source		5.3				nC
Q _{g(th)}	Gate Charge at V _{th}		3.1				nC
Q _{OSS}	Output Charge	V _{DS} = 13.5V, V _{GS} = 0V	33				nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5V, V _{GS} = 4.5V, I _D = 25A, R _G = 2Ω	11.9				ns
t _r	Rise Time		18.4				ns
t _{d(off)}	Turn Off Delay Time		16				ns
t _f	Fall Time		9				ns
Diode Characteristics							
V _{SD}	Diode Forward Voltage	I _S = 25A, V _{GS} = 0V	0.8			1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13.5V, I _F = 25A, di/dt = 300A/μs	42				nC
t _{rr}	Reverse Recovery Time	V _{DD} = 13.5V, I _F = 25A, di/dt = 300A/μs	34				ns

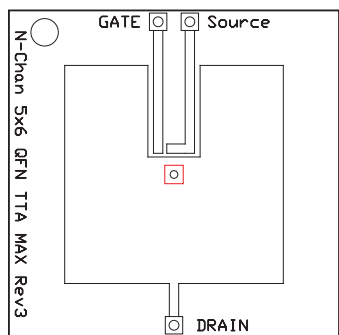
THERMAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case (Top Source) ⁽¹⁾			1.2	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction to Case (Bottom Drain) ⁽¹⁾			1.1	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			51	$^\circ\text{C/W}$

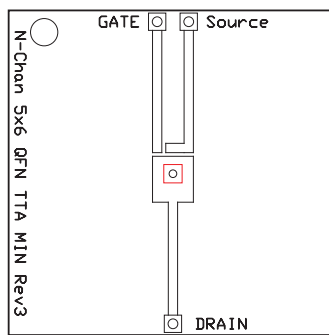
(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 51^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

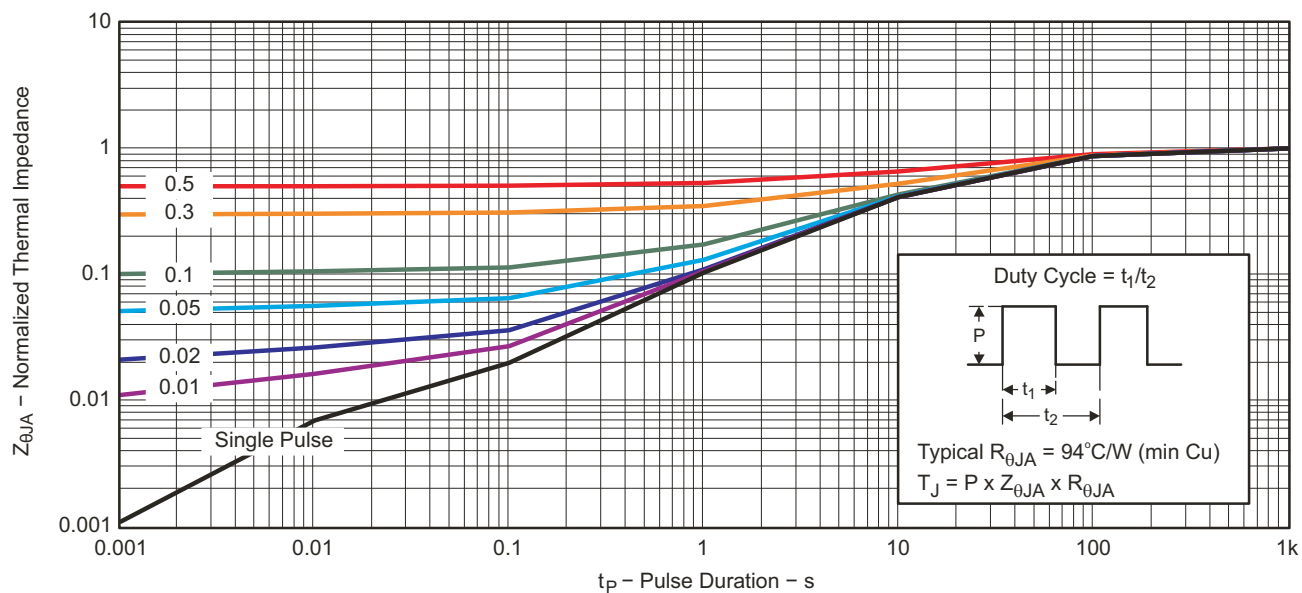


M0137-02

Max $R_{\theta JA} = 121^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$, unless otherwise specified



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, unless otherwise specified

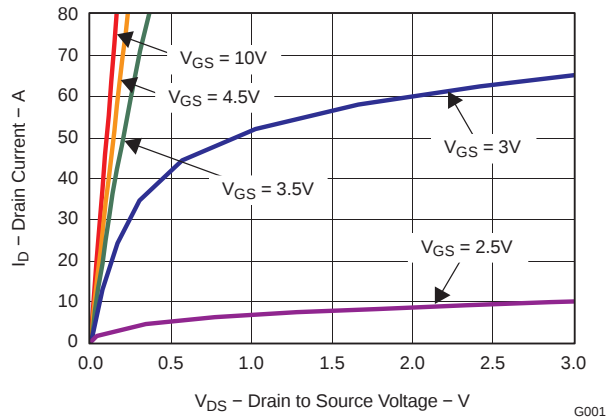


Figure 2. Saturation Characteristics

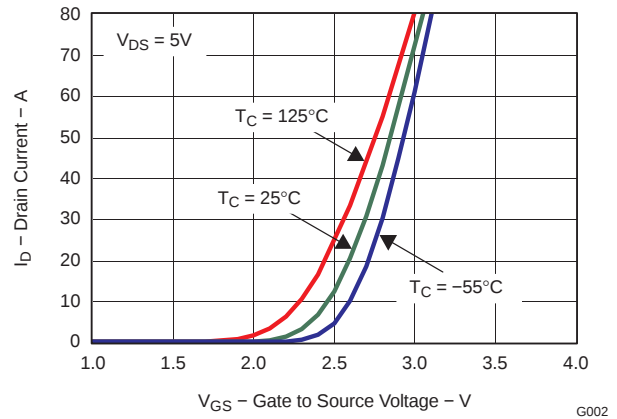


Figure 3. Transfer Characteristics

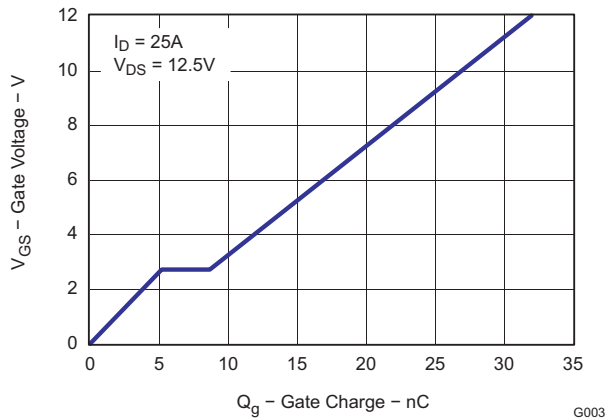


Figure 4. Gate Charge

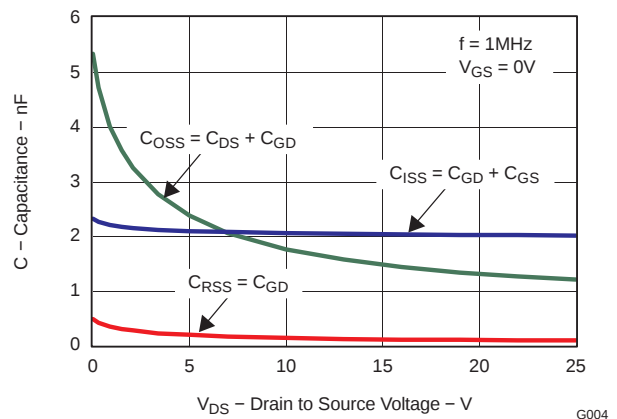


Figure 5. Capacitance

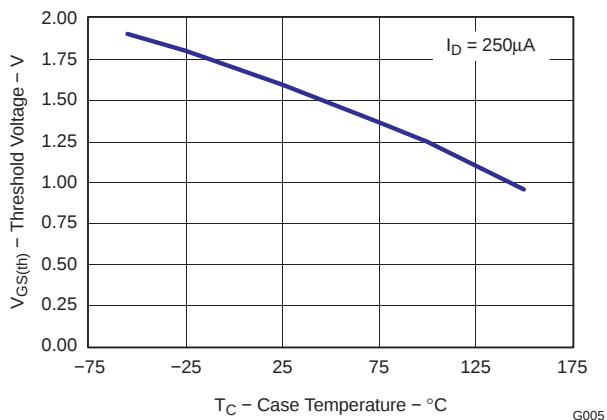


Figure 6. Threshold Voltage vs. Temperature

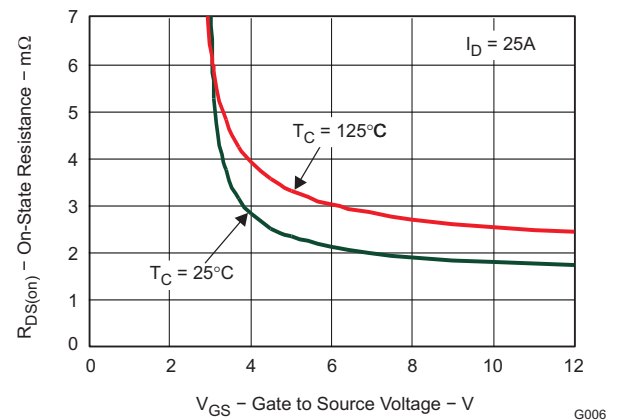


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$, unless otherwise specified

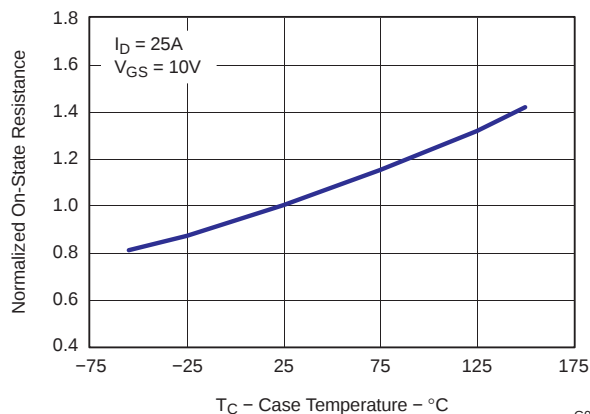


Figure 8. Normalized On-State Resistance vs. Temperature

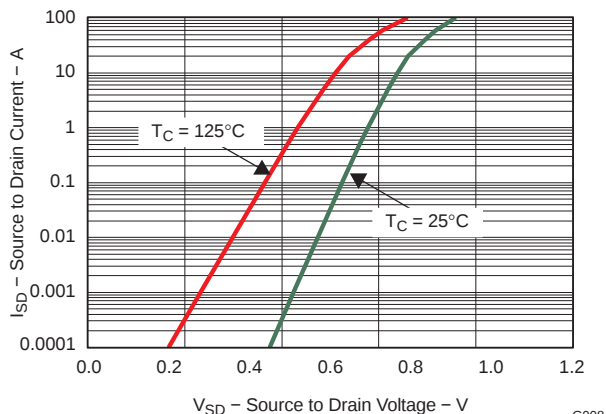


Figure 9. Typical Diode Forward Voltage

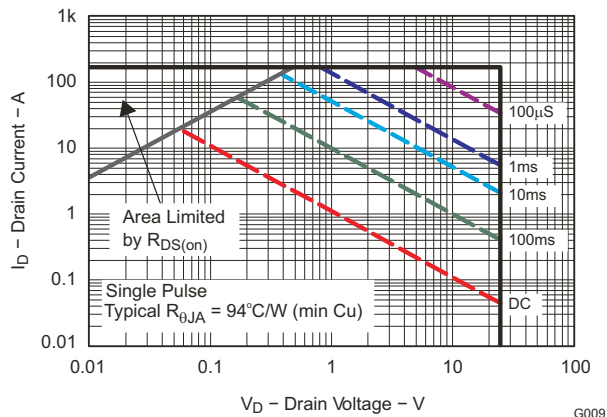


Figure 10. Maximum Safe Operating Area

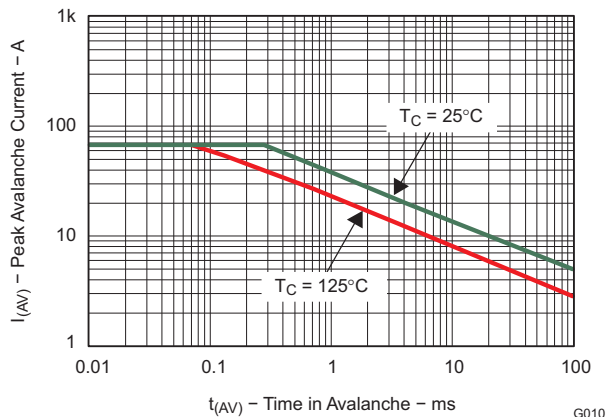


Figure 11. Single Pulse Unclamped Inductive Switching

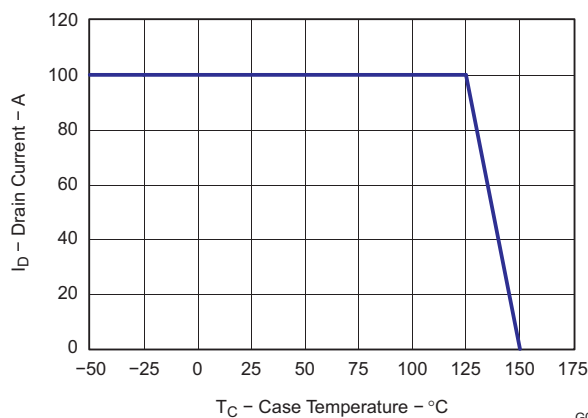
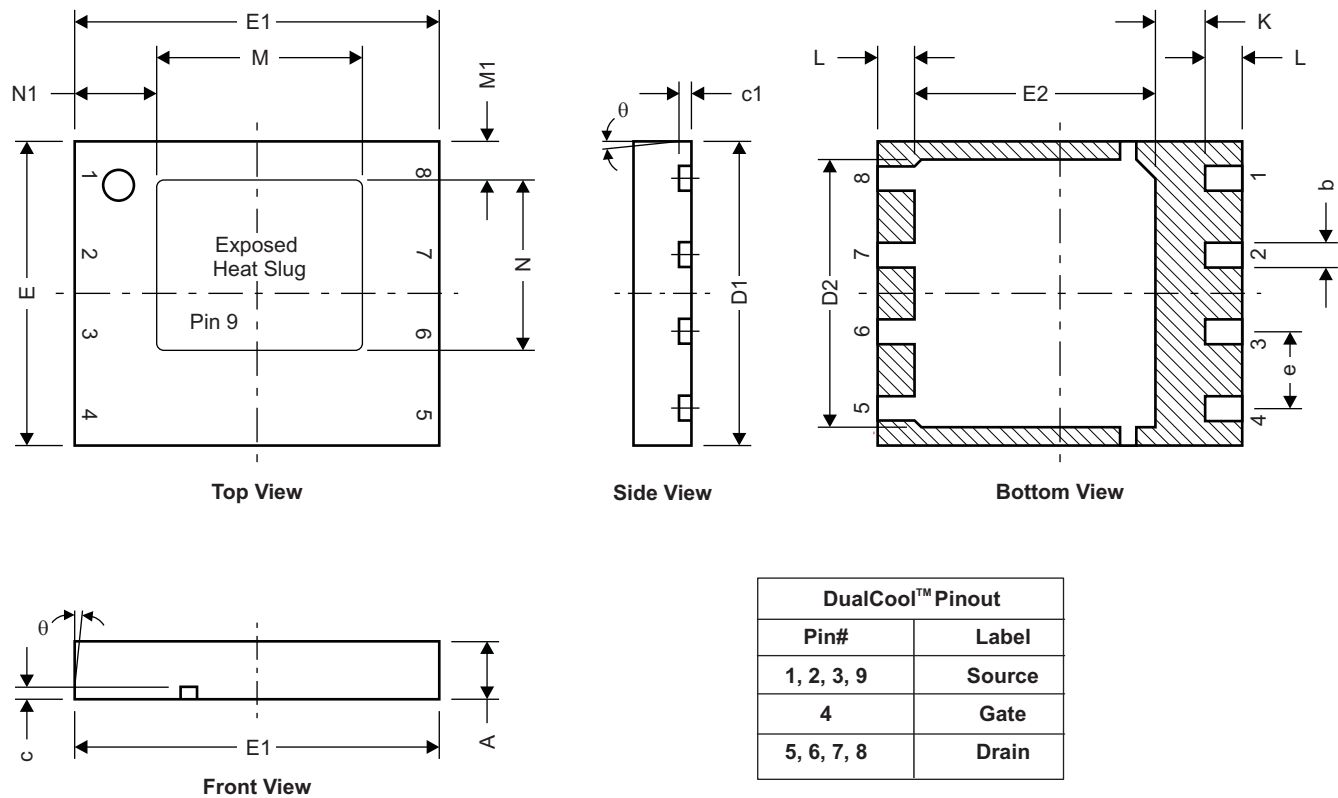
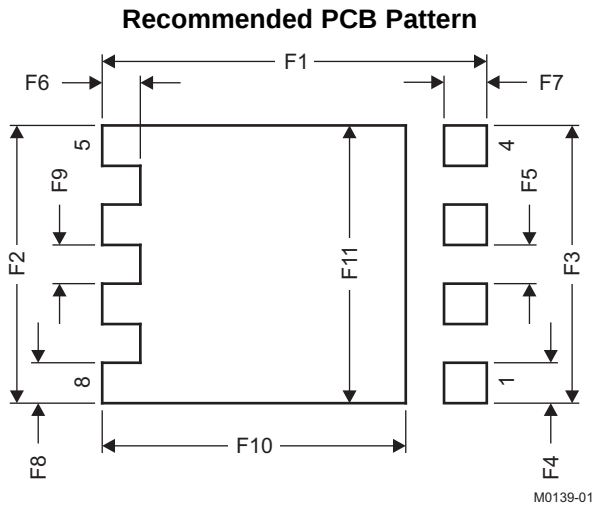


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA**Q5C Package Dimensions**

M0162-01

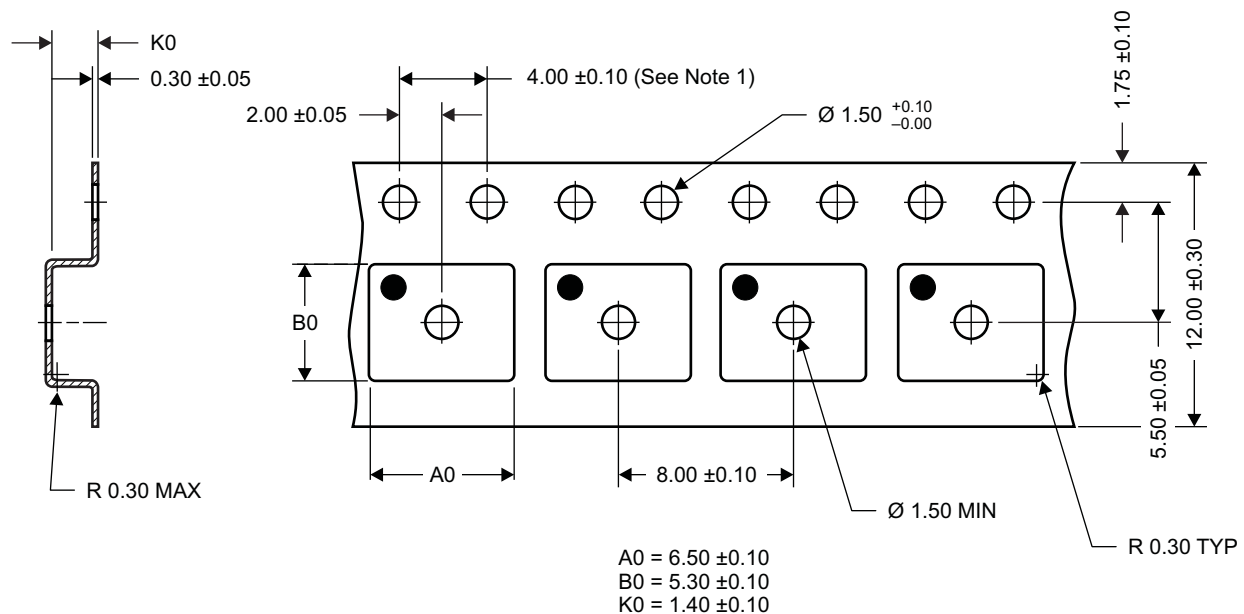
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760	–	0.030	–
L	0.510	0.710	0.020	0.028
θ	–	–	–	–
M	3.260	3.460	0.128	0.136
M1	0.520	0.720	0.020	0.028
N	2.720	2.920	0.107	0.115
N1	1.227	1.427	0.048	0.056



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Q5C Tape and Reel Information



Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm, unless otherwise specified.
- Thickness: 0.30 ± 0.05 mm
- MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (October 2009) to Revision A	Page
- Changed the device From: Procut Preview To: Production 1 - Changed Application - From: Optimized for Control FET Applications To: Optimized for Synchronous FET Applications 1 - Changed the pinout illustration. 1 - Changed the Q5C Package Dimensions illustration 6	
Changes from Revision A (December 2009) to Revision B	Page
- Changed the ABSOLUTE MAXIMUM RATINGS table, I_D - Continuous Drain Current value From: 30A To: 31A 1 - Changed Note 1 of the ABSOLUTE MAXIMUM RATINGS table From: Typical $R_{\theta JA} = 41^\circ\text{C}$ To: Typical $R_{\theta JA} = 40^\circ\text{C}$ 1 - Changed Figure 1 - From: Typical $R_{\theta JA} = 98^\circ\text{C/W}$ To: Typical $R_{\theta JA} = 94^\circ\text{C/W}$ 3 - Changed Figure 10 - From: Typical $R_{\theta JA} = 98^\circ\text{C/W}$ To: Typical $R_{\theta JA} = 94^\circ\text{C/W}$ 5 - Changed Figure 11 - X axis values 5	
Changes from Revision B (January 2010) to Revision C	Page
Changed the labels on the Bottom View pinout image 1	
Changes from Revision C (February 2010) to Revision D	Page
Deleted the Package Marking Information section 7	

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