User's Manual

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M68EML08GZ
Emulation Module

User's Manual

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Make sure that power is disconnected from your M68EML08GZ Emulator Module and from your target system. Then follow these quick-start steps to make your M68EML08GZ ready for use as quickly as possible.

1 - Set jumpers W4, W5, and W6

Jumper header W4 specifies the clock source for the MCU when you enable its external clock.

- Place the jumper between pins 3 and 4 (factory default) to specify the debugger-controlled oscillator from the platform board or place the jumper between pins 1 and 2 to specify oscillator Y2, which can be replaced with an oscillator of a different value.

Jumper headers W5 and W6 specify the emulation MCU.

- Place jumper W5 in the position for the flash size of the part you want to emulate. Valid emulation MCUs are MC68HC908GZ60, MC68HC908GZ48, MC68HC908GZ16, MC68HC908GR16, MC68HC908GZ8, MC68HC908GR8, and MC68HC908GR4. MC68HC908GZ60 is the factory default.
- Place jumper W6 between pins 2 and 3 to specify a HC08GZ family MCU or place the jumper between pins 1 and 2 to specify a HC08GR family MCU. GZ family emulation is the factory default.

2 - Install the emulation module into your development system

To use the M68EML08GZ in an MMDS0508 Motorola Modular Development System (MMDS) or MMEVS0508 Motorola Modular Evaluation System (MMEVS):

- Remove the access panel of the MMDS station-module enclosure.
- Insert the M68EML08GZ through the access-panel opening.

- Fit together M68EML08GZ connectors P1 and P2 (on the bottom of the board) to connectors P11 and P12, respectively, of the MMDS or MMEVS (P6 and P7 on some MMEVS boards) control board and snap the corners of the M68EML08GZ onto the plastic standoffs.

3 - Connect the emulation module to your target system

Use the supplied target flex cable, appropriate target head adapter, and surface mount adapter. Plug the appropriate end of the flex cable plugs into M68EML08GZ connectors J2 and J3.

- If the M68EML08GZ is in an MMDS station module, run the flex cable through the slit in the station-module enclosure, then replace the access panel.
- Plug the other end of the flex cable into the target head. Solder the appropriate surface mount adapter to your target if necessary. Then plug the target head into the surface mount adapter on your target system.

4 - Install the development software

5 - Copy personality files to your computer

The factory ships M68EML08GZ MCU personality files on the documentation CD-ROM.

- If you're using the CodeWarrior IDE, find the installation directory and copy the personality files named 00C35Vxx.mem, 00C36Vxx.mem, 00C38Vxx.mem, 00C3DVxx.mem, 00C3CVxx.mem, 00C77Vxx.mem, and 00C78Vxx.mem from the documentation CD-ROM to the `...\prog\mem` subdirectory of the CodeWarrior IDE main directory.
- If you're using the P&E debugger, copy these files to the installation directory that contains MMDS08.EXE or MMEVS08.EXE and rename them from 00C35Vxx.mem, 00C36Vxx.mem, 00C38Vxx.mem, 00C3CVxx.mem, 00C3DVxx.mem, 00C77Vxx.mem, and 00C78Vxx.mem to 00435Vxx.mem, 00436Vxx.mem, 00438Vxx.mem, 0043CVxx.mem, 0043DVxx.mem, 00477Vxx.mem, and 00478Vxx.mem respectively.

6 - Connect MMDS or MMEVS to your computer and apply power

This completes the quick start for your M68EML08GZ. When you make sure that cable connections between your development system and your computer are sound, you are ready to apply power and use your M68EML08GZ.

M68EML08GZ Quick Start Guide

Section 1. General Information

1.1 Introduction

This user's manual explains connection and configuration of the Motorola M68EML08GZ Emulator Module (EML08GZ). The EML08GZ makes possible emulation and debugging of target systems based on an MC68HC908GZ60, MC68HC908GZ48, MC68HC908GZ16, MC68HC908GR16, MC68HC908GZ8, MC68HC908GR8, or MC68HC908GR4 microcontroller unit (MCU).

The M68EML08GZ can be part of two development systems. This section describes those systems and explains the layout of the EML08GZ.

1.2 Development Systems

Your EML08GZ can be part of two Motorola HC08 processor family development systems: the MMDS0508 Motorola Modular Development System (MMDS) or the MMEVS0508 Evaluation System (MMEVS). Refer to the specific development system user's manual for more information.

1.2.1 Motorola Modular Development System (MMDS0508)

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows for designing and debugging a target system. A complete MMDS consists of:

- **a station module** — the metal MMDS enclosure, containing the platform board and the internal power supply. Most system cables connect to the MMDS station module.
- **an emulator module (EM)** — such as the EML08GZ, a separately-purchased printed circuit board that enables system functionality for a specific set of MCUs. The EM fits into the station module through a removable panel in the enclosure top. The EM has connectors for a target cable and for cables to a logic analyzer. The cable runs to an optional target system through an aperture in the station-module enclosure, to connect directly to the emulator module.

- **two logic clip cable assemblies** — twisted-pair cables that connect the station module to your target system, a test fixture, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies and may be attached to the female probe tips.
- **a 9-lead RS-232 serial cable** — the cable that connects the MMDS to the host computer RS-232 port.
- **system software** — development software, on CD-ROM.
- **MMDS0508 documentation** — an MMDS operations manual (MMDS0508OM/D) and the appropriate EM user's manual.

You select the MMDS baud rate: 1200, 2400, 4800, 9600, 19200, 38400, or 57600.

Substituting a different EM enables your MMDS to emulate target systems based on different MCUs or MCU families. (Your Motorola representative can explain all the EMs available.)

1.2.2 Motorola Modular Evaluation System (MMEVS0508)

An MMEVS is an economical tool for designing, debugging, and evaluating target systems. A complete MMEVS consists of:

- **a platform board (PFB)** — the bottom board, which supports the emulator module. The platform board has connectors for power and the the terminal or host computer.
- **an emulator module (EM)** — such as the EML08GZ, a separately purchased printed circuit board that enables system functionality for a specific set of MCUs. The EM fits onto the PFB. The EM has connectors for the target cable and for cables to a logic analyzer.
- **a 9-to-25-pin adapter** — a molded assembly that lets you connect the 9-pin cable to a 25-pin serial port.
- **a 9-lead RS-232 serial cable** — the cable that connects the station module to the host computer RS-232 port.
- **system software** — development software, on CD-ROM.

- **MMEVS0508 documentation** — an MMEVS operations manual (MMEVSOM/D) and the appropriate EM user's manual.

An MMEVS features automatic baud rate selection: 2400, 4800, 9600, 19200, 38400, or 57600.

Substituting a different EM enables your MMEVS to emulate target systems based on different MCUs or MCU families. (Your Motorola representative can explain all the EMs available.).

1.3 System Requirements

An IBM PC or compatible running Windows® 98, Windows 2000, or Windows NT® (version 4.0) with at least 32MB of RAM and an RS-232 serial port.

1.4 EM Layout

Figure 1-1 shows the layout of the EML08GZ. Jumper header W1 specifies the operating voltage. Jumper W2 selects the PLL filter. Jumper header W3 controls unification of analog ground references. Jumper header W4 specifies the clock signal source. Jumper headers W5 and W6 specify flash size and the MCU family to be emulated.

Target interface connectors J2 and J3 connect the EML08GZ to a target system, via the included target cable assembly. If you use your EML08GZ as part of an MMDS, run the target cable assembly through the slit in the station module enclosure.

Connectors J1 and J13 connect to a logic analyzer. Connector J12 is the source for an inverted clock signal. DIN connectors P1 and P2, on the bottom of the board connect the EML08GZ to the platform board. The emulation MCU is at location U3. Connector J14 is for EM board design and factory use only.

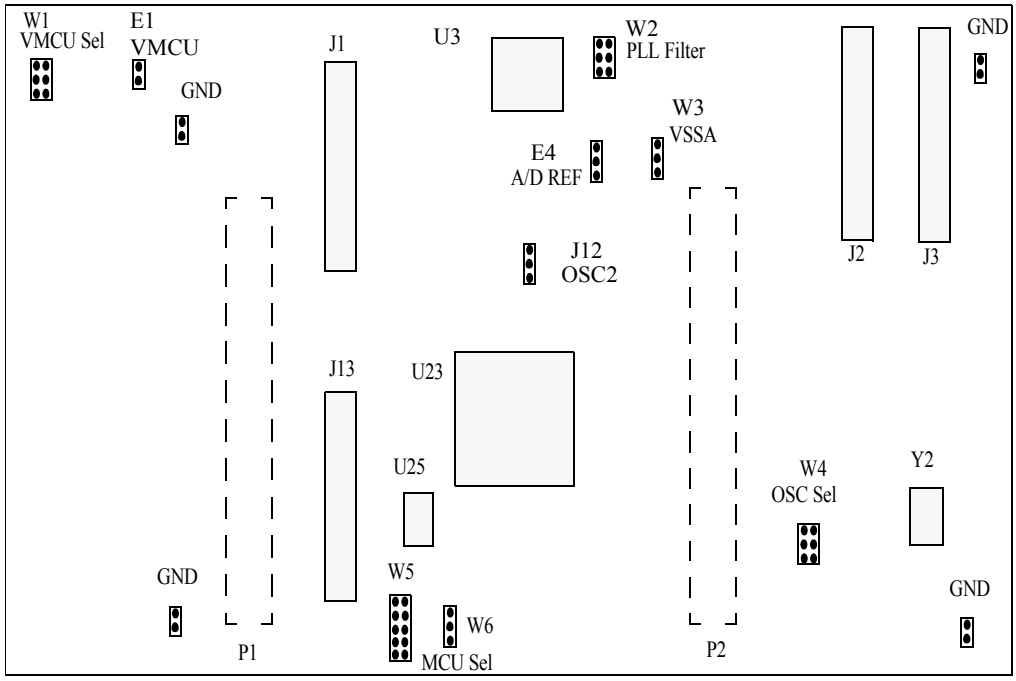


Figure 1-1 M68EML08GZ Emulator Module

1.5 Specifications

Table 1-1 lists EML08GZ specifications

Table 1-1 Specifications

Characteristic	Specifications
Maximum Clock speed	32.8-MHz (8.2-MHz Bus) at 5V 16.4-MHz (4.1-MHz Bus) at 3V
Target Voltage	Target Tracking 1.8V to 5.5V, 3V Forced or 5V Forced (+/-10%)
Temperature operating storage	 -10° to +50° C -40° to +85° C
MCU Extension I/O	HCMOS Compatible at Vmcu (5V or 3V)
Relative humidity	0 to 90% (noncondensing)
Power requirements	5VDC supplied from the MMDS or MMEVS
Dimensions	5.5 X 8.0 X 0.75 inches (139.7 x 203.2 x 19.1 mm)

1.6 Target Cable Assemblies

To connect your EML08GZ to a target system, you need the included target cable and adapters. See Figure 1-2.

The cable assembly for a 64-pin QFP package consists of: a flex cable, a target head adapter, a socket-saver and a 64-pin QFP surface mount adapter. The cable assembly for a 48-pin QFP package consists of: a flex cable, a target head adapter, a socket-saver and a 48-pin QFP surface mount adapter. The cable assembly for a 32-pin QFP package consists of: a flex cable, a target head adapter, a socket-saver and a 32-pin QFP surface mount adapter. The cable assembly for a 28-pin DIP or SOIC package consists of: a flex cable, a target head adapter, and a 28-pin SOIC surface mount adapter. One end of the target cable plugs onto EML08GZ connectors J2 and J3. The other end of the flex cable plugs onto the target head adapter, which plugs onto the QFP surface mount adapter. You should solder the QFP surface mount adapter directly onto the target-system board in place of the MCU. The socket-saver goes between the target head adapter and surface mount adapter. If you use it, it will reduce wear on the target head adapter. After many insertions, you can replace the socket-saver without replacing the entire target head adapter.

Table 1-2 lists target cable and head part numbers appropriate for the EML08GZ.

Table 1-2 M68EML08GZ Target Cable and Head Assemblies

MCU Package	Flex Cable Part Number	Target Head Adapter Part Number	Surface Mount Adapter Part Number	Socket-Saver Part Number
28-pin DIP/SOIC	M68CBL05C	M68TC08GZP28	M68DIP28SOIC	N/A
32-pin QFP	M68CBL05C	M68TC08GZFJ32	M68TQP032SA1	M68TQS032SAG1
48-pin QFP	M68CBL05C	M68TC08GZFA48	M68TQP048SD1	M68TQS048SDG1
64-pin QFP	M68CBL05C	M68TC08GZFB64	M68TQP064SA1	M68TQS064SAG1

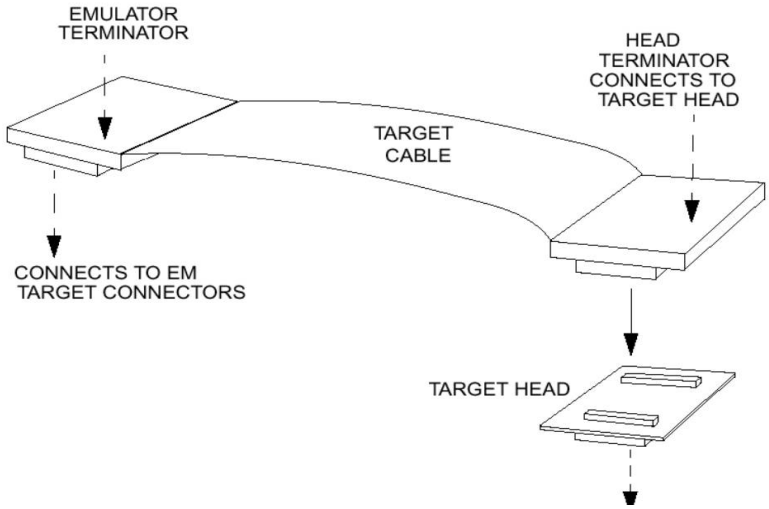


Figure 1-2 Target Cable Assembly

Section 2. Preparation and Operation

2.1 Introduction

This section explains EML08GZ preparation: how to set board jumpers and how to make system connections.

Note that you can reconfigure an EML08GZ already installed in an MMDS0508 station module enclosure. To do so, switch off station-module power and target power, remove the panel, then follow the guidance of this section. Similarly, you can reconfigure an EML08GZ already installed on the MMEVS platform board, provided that you disconnect platform-board power and target power.

CAUTION: ESD Protection

Motorola development systems include open-construction printed circuit boards that contain static-sensitive components. These boards are subject to damage from electrostatic discharge (ESD). To prevent such damage, you must use static-safe work surfaces and grounding straps, as defined in ANSI/EOS/ESD S6.1 and ANSI/EOS/ESD S4.1. All handling of these boards must be in accordance with ANSI/EAI 625.

2.2 Configuring Board Components

Table 2-1 is a summary of configuration settings.

Table 2-1 Configuration Components

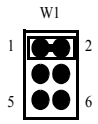
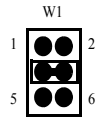
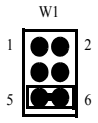
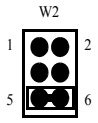
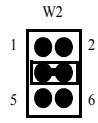
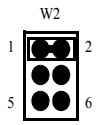
Component	Position	Effect
Target Voltage Select Header, W1 (Not populated) You must populate this header and remove component R3 to use this function.		**5V:** Forces 5.0-volt system operating voltage.
You must populate this header and remove component R3 to use this function.		**3V:** Forces 3.0-volt system operating voltage.
This is the factory configuration. Component R3 forces this option. (Use only one jumper in this header.)		**TRCK:** Specifies that the system operating voltage track the target voltage (1.8V to 5.5V). If no target is connected or if the target voltage decreases below 500mV, then the system operating voltage will switch to 5V. **Factory setting**
PLL Filter Select Header, W2 (Use only one jumper in this header.)		**5M:** Specifies a PLL filter circuit designed for 5MHz reference frequency. **Factory setting**
		**32K:** Specifies a PLL filter circuit designed for 32kHz reference frequency.
		**CUS:** Specifies a custom PLL filter circuit. You must populate thru-hole components C2, C3, and R2 with appropriate values for your desired reference frequency.

Table 2-1 Configuration Components (Continued)

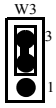
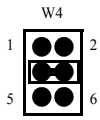
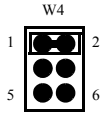
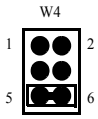
Component	Position	Effect
Analog Ground (VSSA) Unify Header, W3		**DISCONNECT:** Separates analog ground references of the processor and the board. **Factory setting**
		**CONNECT:** Unifies analog ground references of the processor and the target board: VSSA = VREF_LOW = AGND. (This configuration increases sensitivity to noise)
Oscillator Select Header, W4 (Use only one jumper in this header.)		**PFB:** Specifies the oscillator clock signal from the platform board (PFB). **Factory setting**
		**EM:** Specifies the clock signal from the 4.915-megahertz oscillator on the EM board at Y2 (EM).
		**XTAL:** Specifies the clock signal from a crystal installed at Y1 (XTAL).

Table 2-1 Configuration Components (Continued)

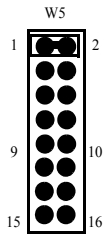
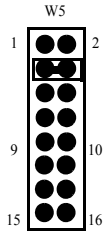
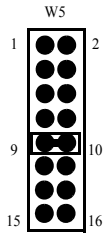
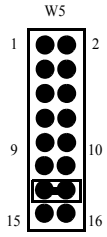
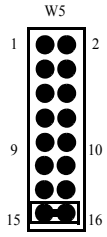
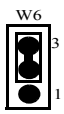
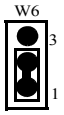
Component	Position	Effect
MCU Flash Size Select Header, W5 Settings other than those described here are not currently supported. (Use only one jumper in this header.)		**60K:** Specifies an MCU flash size of 60K. Use this setting to emulate an HC08GZ60 MCU. **Factory setting**
		**48K:** Specifies an MCU flash size of 48K. Use this setting to emulate an HC08GZ48 MCU.
		**16K:** Specifies an MCU flash size of 16K. Use this setting to emulate an HC08GZ16 or HC08GR16 MCU.
		**8K:** Specifies an MCU flash size of 8K. Use this setting to emulate an HC08GR8 or HC08GZ8 MCU.
		**4K:** Specifies an MCU flash size of 8K. Use this setting to emulate an HC08GR4 MCU.

Table 2-1 Configuration Components (Continued)

Component	Position	Effect
MCU Family Select Header, W6		**GZ:** Specifies emulation of an HC08GZ family MCU. **Factory setting**
		**GR:** Specifies emulation of an HC08GR family MCU.

2.3 Limitations

Limitations listed here apply to using your EML08GZ versus using the actual MCU in your target system:

Limitation 1 - Crystals: You can install a crystal at location Y1 and associated components (refer to the schematic) to be a clock signal source. But each crystal has slightly different characteristics, and a crystal's behavior can differ substantially in different circuits. Satisfactory performance as part of the EML08GZ Y1 timing circuit does not guarantee that the same crystal will perform satisfactorily on a target board.

Limitation 2 - OSC2: The OSC2 pin function will not be available on the target cable. If you wish to use this signal on your target, you must make a connection between J12 and your target system.

Limitation 3 - MCLK: The MCLK (T12CLK) pin function will not be available on the target cable. If you wish to use this signal on your target, you must make a connection between J1 pin 3 and your target system.

Limitation 4 - GR8 and GR4 Registers: The emulator uses a GZ60 to emulate all supported MCUs. Several of the GR8 and GR4 registers may be different than emulator registers, such as in the A/D module.

Limitation 5 - LVI Resets: The emulator will not reset if the target voltage falls below the LVI thresholds.

Limitation 6 STOP Mode: The emulator will not correctly recover from STOP mode in certain circumstances. When using the IRQ in conjunction with the STOP function, you must make sure the IRQ is not asserted as you enter STOP. Otherwise the debugger will stop and cite a write protect error.

2.4 Remaining System Installation

When you have configured jumper headers, you are ready to complete EML08GZ installation:

- To install the EML08GZ in an MMDS0508 station module, remove the panel from the station module top. Fit together EM connectors P1 and P2 (on the bottom of the board) and platform-board connectors P11 and P12, respectively. Snap the corners of the EM onto the plastic standoffs. Connect the target cable, if appropriate, then replace the panel.
- If your EML08GZ already is installed in the station module, reconnect the target cable (if necessary). Replace the panel.
- To install the EML08GZ on an MMEVS platform board, fit together EM connectors P1 and P2 (on the bottom of the board) and platform-board connectors P11 and P12 (P6 and P7 on some MMEVS boards), respectively. Snap the corners of the EM onto the plastic standoffs.
- *If you will use the P&E development system*, copy personality files 00C35Vxx.mem, 00C36Vxx.mem, 00C38Vxx.mem, 00C3CVxx.mem, 00C3DVxx.mem, 00C77Vxx.mem, and 00C78Vxx.mem from the documentation CD-ROM to the installation directory that contains file `MMDS08.EXE or MMEVS08.EXE`. Then rename these files to 00435Vxx.mem, 00436Vxx.mem, 00438Vxx.mem, 0043DVxx.mem, 00477Vxx.mem, and 00478Vxx.mem.
- *If you will use the CodeWarrior IDE development software*, copy personality files 00C35Vxx.mem, 00C36Vxx.mem, 00C38Vxx.mem, 00C3CVxx.mem, 00C3DVxx.mem, 00C77Vxx.mem, and 00C78Vxx.mem from the documentation CD-ROM to the `...\prog\mem` subdirectory of the CodeWarrior IDE installation directory.

  Additionally, if you must use CodeWarrior IDE development software, you will need to copy the EML08GZ register files `MCU0C35.reg, MCU0C36.reg, MCU0C38.reg, MCU0C3C.reg, MCU0C3D.reg, MCU0C77.reg, and MCU0C78.reg` from the documentation CD-ROM to the `...\prog\reg` subdirectory of the CodeWarrior IDE installation directory. The CodeWarrior IDE uses these files to implement optional functionality such as letting you view

or modify register contents by name rather than by address. A register file is an ASCII text file, which you may customize. (The CodeWarrior IDE user's manual explains how to create and use such files.)

At this point, you are ready to make any remaining cable connections and apply power. For instructions, consult the MMDS or MMEVS operations manual.

2.5 Running the Automated Board Test

This section explains how to test the EML08GZ emulation module using test software located on the included documentation CD-ROM. This test allow you to verify the proper operation of your board.

2.5.1 Set up the hardware

Follow the setup steps outlined in the Quickstart section of this user's manual. You must have the CodeWarrior IDE for HC08V3.0 or later installed on your computer to run this test. Do not connect the emulator board to your target system during this test.

2.5.2 Install the test software

The factory ships the EML08GZ with the test software. Double-click the file EML08GZ_Test.exe on the included documentation CD-ROM to run the setup program and follow the installation instructions. You must install this softare in the default location.

2.5.3 Run the test

Run the test by choosing Programs -> EML08GZ60 -> EML08GZ in the Windows Start Menu. Then follow the steps below:

- Click on the *Setup* button and verify that your hardware is connected as shown in the diagram. Click *Hide* to close the diagram.

- Click on the *Initial/Final Jumper Configuration* button and verify that the jumper setting on your board match the diagram. Verify that you have the factory installed 32.768kHz oscillator in location Y2. Click *Hide* to close the diagram.
- Apply power to the emulator.
- Click on the *Test* button.
- Click *OK* when you are ready to run the test.
- Move the jumpers as directed during the test.
- When the test is complete, you can verify that each item tested passed by checking that its box is green. The message window also displays the results of each test.
- You may now either run the test again or exit this program by clicking on the *Exit* button.

Section 3. Support Information

3.1 Introduction

This section consists of connector pin assignments, connector signal descriptions, and other information that may be useful in your development activities.

3.2 Target Connectors J2 and J3

Connectors J2 and J3 are the EML08GZ target connectors. Figure 3-1 and Table 3-1 give the pin assignments and signal descriptions for connector J2. Figure 3-2 and Table 3-2 give the pin assignments and signal descriptions for connector J3.

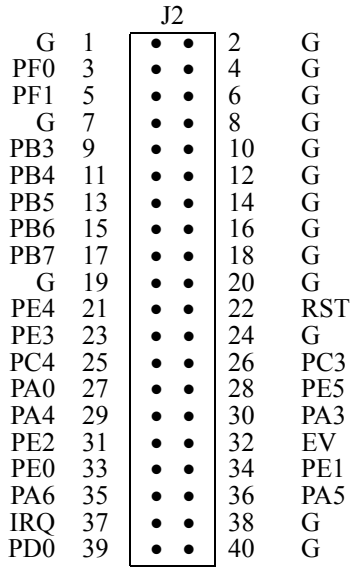


Figure 3-1 Target Connector J2 Pin Assignments

Table 3-1 Target Connector J2 Signal Descriptions

Pin	Label	Signal
1 — 2, 4, 6 — 8, 10, 12, 14, 16, 18 — 21, 23, 24, 28, 31, 38, 40	G	GROUND
9, 11, 13, 15, 17	PB3 — PB7	PORT B (lines 3—7) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port B lines are available on connector J3.)
22	RST	RESET — Active-low signal. If an output, starts a target reset. If an input, confirms reset of the target MCU.
25, 26	PC4, PC3	PORT C (lines 4, 3) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port C lines are available on connector J3.)
27, 29, 30, 35, 36	PA0, PA3 — PA6	PORT A (lines 0, 3—6) — General-purpose I/O lines controlled by software via data direction and data registers. (Port A lines 1, 2, and 7 are available on connector J3.)
32	EV	EXTERNAL VOLTAGE DETECT — Input signal that detects target-system power-up.
33, 34, 31, 23, 21, 28	PE0 — PE5	PORT E (lines 0 — 5) — General-purpose I/O lines controlled by software via data direction and data registers.
37	IRQ	TARGET INTERRUPT — Active-low input line for requesting a target interrupt.
39	PD0	PORT D (line 0) — General-purpose I/O lines controlled by software via data direction and data registers. (Port D line 1—7 is available on connector J3.)
3, 5	PF0, PF1	PORT F (lines 0—1) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port F lines are available on connector J3.)

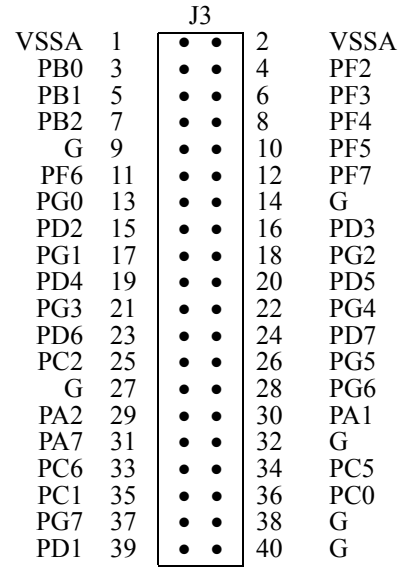


Figure 3-2 Target Connector J3 Pin Assignments

Table 3-2 Target Connector J3 Signal Descriptions

Pin	Label	Signal
1, 2	VSSA	TARGET ANALOG GROUND — Analog-ground reference signal from the target.
3, 5, 7	PB0 — PB2	PORT B (lines 0—2) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port B lines are available on connector J2.)
4, 6, 8 — 24, 26 — 28, 31 — 34, 37, 38, 40	G	GROUND
36, 35, 25, 34, 33	PC0 — PC2, PC5, PC6	PORT C (lines 0—2, 5, 6) — General-purpose I/O lines controlled by software via data direction and data registers. (Port C lines 3 and 4 are available on connector J2.)
29, 30, 31	PA2, PA1, PA7	PORT A (lines 2, 1) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port A lines are available on connector J2.)
39, 15, 16, 19, 20, 23, 24	PD1 — PD7	PORT D (lines 1—7) —General-purpose I/O lines controlled by software via data direction and data registers. (Port D line 0 is available on connector J2.)
4, 6, 8, 10—12	PF2—PF7	PORT F (lines 2—7) — General-purpose I/O lines controlled by software via data direction and data registers. (Other port F lines are available on connector J2.)
13, 17, 18, 21 22, 26, 28, 37	PG0—PG7	PORT G (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.

3.3 Logic Analyzer Connectors J1 and J13

Connectors J1 and J13 are the EML08GZ logic analyzer connectors. Figure 3-3 and Table 3-3 give pin assignments and signal descriptions for connector J1, which has pod 1 signals. Figure 3-4 and Table 3-4 give pin assignments and signal descriptions for connector J13, which has pod 2 signals.

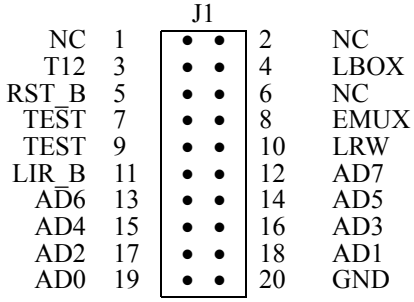


Figure 3-3 Logic Analyzer Connector J1 Pin Assignments

Table 3-3 Logic Analyzer Connector J1 Signal Descriptions

Pin	Label	Signal
1, 2, 6	NC	No connection
3	T12	SYSTEM BUS CLOCK — Clock that matches the internal emulation MCU bus clock
4	LBOX	LAST BUS CYCLE — Output signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction.
5	RST_B	COP RESET — Active-low output signal indicating (1) the target driving its reset pin, or (2) the platform board driving a reset to the emulator module.
7, 9	TEST	Test pins are used only during system development and factory test.
8	EMUX	MUXED CONTROL — Output from the emulation MCU that, during different phases of the clock, drives R/W, LIR_B, and LAST signals.
10	LRW	LATCHED READ/WRITE — Output signal from the target MCU. If high, the target MCU is reading. If low, the target MCU is writing.
11	LIR_B	LOAD INSTRUCTION REGISTER — Active-low output signal indicating that the target MCU is fetching an instruction.
12 — 19	AD7 — AD0	PFB DATA BUS (lines 7—0) — Outputs the data lines going to the platform board.
20	GND	GROUND

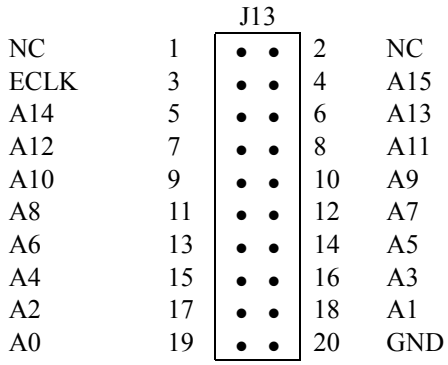


Figure 3-4 Logic Analyzer Connector J13 Pin Assignments

Table 3-4 Logic Analyzer Connector J13 Signal Descriptions

Pin	Label	Signal
1, 2	NC	No connection
3	ECLK	EM CLOCK — Output clock signal for the emulator module.
4 — 19	A15 — A0	LATCHED ADDRESS BUS (lines 15—0) — Output showing the address of the current bus cycle.
20	GND	GROUND

3.4 Inverted Clock Connector J12

Connector J12 is the source for inverted clock signal OSC2. Figure 3-5 and Table 3-5 give the pin assignments and signal descriptions for this connector. Because the OSC2 signal is not present on the target cable, you should connect this signal to your target system if you will use the OSC2 signal.

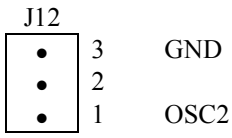


Figure 3-5 Connector J12 Pin Assignments

Table 3-5 Connector J12 Signal Descriptions

Pin	Label	Signal
3	GND	Ground
2		No connection
1	OSC2	INVERTED CLOCK OUTPUT — Inversion of the clock signal that jumper header W4 specifies if you select the external clock. Inversion of the PLL clock if you select the PLL clock (default).

3.5 Analog-to-Digital Converter Reference Voltage Connector E4

Connector E4 is the source for the filtered A/D reference voltages. Figure 3-6 and Table 3-6 give the pin assignments and signal descriptions for this connector. The factory test uses this connection.

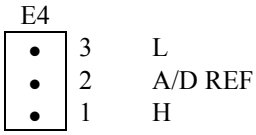


Figure 3-6 Connector E4 Pin Assignments

Table 3-6 Connector E4 Signal Descriptions

Pin	Label	Signal
3	L	LOW REFERENCE VOLTAGE
2	A/D REF	No connection (label only)
1	H	HIGH REFERENCE VOLTAGE

3.6 Board Factory Test Connector J14

Factory tests use this connector. It may not be populated.

3.7 Optional crystal circuit using Y1

When you select the XTAL option on jumper W4 (jumper on pins 5-6), the clock signal generated by Y1 is supplied to the external inputs of the MCU. This circuit does not necessarily represent a crystal attached to the MCU.

3.8 Clock oscillator Y2

When you select the EM option on jumper W4 (jumper on pins 1-2), the clock signal generated by Y2 is supplied to the external inputs of the MCU. You can replace Y2 with another compatible clock oscillator to provide a different clock frequency (see schematic page 6).

3.9 EM Board Socket Connectors P1 and P2

Connectors P1 and P2 connect the EML08GZ to the platform board. Figure 3-7 and Table 3-7 give pin assignments and signal descriptions for connector P1. Figure 3-8 and Table 3-8 give pin assignments and signal descriptions for connector P2.

P1

A			B			C		
•	A1	LA[14]	•	B1	PFB_AD[7]	•	C1	GND
•	A2	LA[13]	•	B2	PFB_AD[6]	•	C2	GND
•	A3	LA[12]	•	B3	PFB_AD[5]	•	C3	GND
•	A4	LA[11]	•	B4	PFB_AD[4]	•	C4	GND
•	A5	LA[10]	•	B5	PFB_AD[3]	•	C5	GND
•	A6	LA[9]	•	B6	PFB_AD[2]	•	C6	GND
•	A7	LA[8]	•	B7	PFB_AD[1]	•	C7	GND
•	A8	LA[7]	•	B8	PFB_AD[0]	•	C8	GND
•	A9	LA[6]	•	B9	LIR_B	•	C9	GND
•	A10	LA[5]	•	B10	LRW	•	C10	GND
•	A11	LA[4]	•	B11	SCLK	•	C11	GND
•	A12	LA[3]	•	B12	T12CLK	•	C12	GND
•	A13	LA[2]	•	B13	NC	•	C13	GND
•	A14	LA[1]	•	B14	NC	•	C14	GND
•	A15	LA[0]	•	B15	NC	•	C15	GND
•	A16	LA[15]	•	B16	NC	•	C16	GND
•	A17	NC	•	B17	INTERNAL_B	•	C17	GND
•	A18	NC	•	B18	NC	•	C18	GND
•	A19	PFB_IRQ_B	•	B19	SWITCH_B	•	C19	GND
•	A20	CHRGPMP	•	B20	NC	•	C20	GND
•	A21	NC	•	B21	NC	•	C21	GND
•	A22	NC	•	B22	NC	•	C22	GND
•	A23	PFB_OSC	•	B23	NC	•	C23	GND
•	A24	NC	•	B24	LBOX	•	C24	GND
•	A25	NC	•	B25	BREAK_B	•	C25	GND
•	A26	NC	•	B26	NC	•	C26	GND
•	A27	NC	•	B27	NC	•	C27	GND
•	A28	NC	•	B28	NC	•	C28	GND
•	A29	NC	•	B29	NC	•	C29	GND
•	A30	NC	•	B30	NC	•	C30	GND
•	A31	PFB_VCC	•	B31	PFB_VCC	•	C31	GND
•	A32	GND	•	B32	GND	•	C32	GND

Figure 3-7 EM Connector P1 Pin Assignments

Table 3-7 EM Connector P1 Signal Descriptions

Pin	Mnemonic	Signal
A1 — A16	LA[15] — LA[0] (not in exact order)	LATCHED ADDRESS BUS (lines 15—0) — Output lines for addressing external devices.
A17, A18, A21, A22, A24 — A30	NC	No connection
A19	PFB_IRQ_B	PFB INTERRUPT — Active-low signal that requests an interrupt of the platform board.
A20	CHRGPMP	CHARGE PUMP — 12-volt signal (from the platform board).
A23	PFB_OSC	PFB OSCILLATOR — Oscillator clock signal from the platform board.
A31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
A32	GND	GROUND
B1 — B8	PFB_AD[7] — PFB_AD[0]	PFB ADDRESS (lines 7—0) — Address of the current bus cycle.
B9	LIR_B	LOAD INSTRUCTION REGISTER — Active-low signal that the target MCU is fetching an instruction.
B10	LRW	LATCHED READ/WRITE — Input signal from the target MCU. If high, the target MCU is reading. If low, the target MCU is writing.
B11	SCLK	SERIAL CLOCK — Output clock signal to the platform board.
B12	T12CLK	T12 CLOCK — Matches the internal bus clock of the emulation MCU.
B13 — B16, B18, B20 — B23, B26 — B30	NC	No connection
B17	INTERNAL_B	INTERNAL RESOURCE — Active-low input signal indicating (1) that the current address is a target-MCU internal resource, or (2) that the EM board recreated the current address.
B19	SWITCH_B	SWITCH CONTROL — Active-low input signal that controls switches into the foreground map.
B24	LBOX	LAST BUS CYCLE — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction.
B25	BREAK_B	BREAK REQUEST — Active-low output signal that requests a switch to background logic.
B31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
B32	GND	GROUND
C1 — C32	GND	GROUND

P2

A			B			C		
•	A1	GND	•	B1	GND	•	C1	GND
•	A2	GND	•	B2	VCC	•	C2	VCC
•	A3	GND	•	B3	PTC[0]	•	C3	PTA[0]
•	A4	GND	•	B4	PTC[1]	•	C4	PTA[1]
•	A5	GND	•	B5	PTC[2]	•	C5	PTA[2]
•	A6	GND	•	B6	PTC[3]	•	C6	PTA[3]
•	A7	GND	•	B7	PTC[4]	•	C7	PTA[4]
•	A8	GND	•	B8	NC	•	C8	PTA[5]
•	A9	GND	•	B9	NC	•	C9	PTA[6]
•	A10	GND	•	B10	NC	•	C10	NC
•	A11	GND	•	B11	LOCKOUT_B	•	C11	PTB[7]
•	A12	GND	•	B12	T_RESET_5V_B	•	C12	PTB[6]
•	A13	GND	•	B13	NC	•	C13	PTB[5]
•	A14	GND	•	B14	PORTS_B	•	C14	PTB[4]
•	A15	GND	•	B15	NC	•	C15	PTB[3]
•	A16	GND	•	B16	PFB_RST_B	•	C16	PTB[2]
•	A17	GND	•	B17	COP_RST_B	•	C17	PTB[1]
•	A18	GND	•	B18	NC	•	C18	PTB[0]
•	A19	GND	•	B19	NC	•	C19	ID9
•	A20	GND	•	B20	NC	•	C20	ID8
•	A21	GND	•	B21	NC	•	C21	ID7
•	A22	GND	•	B22	NC	•	C22	ID6
•	A23	GND	•	B23	NC	•	C23	NC
•	A24	GND	•	B24	NC	•	C24	NC
•	A25	GND	•	B25	NC	•	C25	ID3
•	A26	GND	•	B26	NC	•	C26	ID2
•	A27	GND	•	B27	NC	•	C27	MCU_ID1
•	A28	GND	•	B28	VPRU	•	C28	MCU_ID0
•	A29	GND	•	B29	NC	•	C29	NC
•	A30	GND	•	B30	EVDD	•	C30	DAVINCI
•	A31	GND	•	B31	PFB_VCC	•	C31	PFB_VCC
•	A32	GND	•	B32	GND	•	C32	GND

Figure 3-8 EM Connector P2 Pin Assignments

Table 3-8 EM Connector P2 Signal Descriptions

Pin	Mnemonic	Signal
A1 — A32	GND	GROUND
B1, B32	GND	GROUND
B2	VCC	POWER — Operating voltage.
B3 — B7	PTC[0] — PTC[4]	PORT C (lines 0—4) — General-purpose I/O lines controlled by software via data direction and data registers.
B8 — B10, B13, B15, B18 — B27, 29	NC	No connection
B11	LOCKOUT_B	Used by the platform board to block the IRQ_B signal during reset recovery.
B12	T_RESET_5V_B	Target reset used to sense and drive resets to and from the target.
B14	PORTS_B	Indicates a port-related register access, which is routed to the PRU on the platform board.
B16	PFB_RST_B	PFB RESET — Active-low signal that requests a reset of the platform board.
B17	COP_RST_B	COP RESET — Active-low signal that resets the EM board.
B28	VPRU	Emulation MCU voltage used by the port replacement unit on the platform board.
B31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.
C1, C32	GND	GROUND
C2	VCC	POWER — Operating voltage.
C3 — C9	PTA[0] — PTA[7]	PORT A (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
C10, C23, C24, C29	NC	No connection
C11 — C18	PTB[7] — PTB[0]	PORT B (lines 0—7) — General-purpose I/O lines controlled by software via data direction and data registers.
C19 — C22, C25 — C28	ID9 — ID6, ID3, ID2, MCU_ID1, MCU_ID0	MCU identification signals used by the platform board to detect which EM board is inserted.
C30	DAVINCI	Used to indicate HC05 or HC08 EM boards.
C31	PFB_VCC	PFB POWER — Operating voltage signal from the platform board.

Support Information

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