RailClamp™
Low Capacitance TVS Diode Array

SR2.8

January 05, 2000

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SR series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **EFT** (electrical fast transients), and tertiary **lightning.**

The unique design of the SR series devices incorporates four surge rated, low capacitance steering diodes and a TVS diode in a single package. The TVS diode is constructed using Semtech's proprietary low voltage EPD technology for superior electrical characteristics at 2.8 volts.

During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The low capacitance array configuration allows the user to protect two high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges.

FEATURES

- ESD protection to **IEC 1000-4-2, Level 4**
- Array of surge rated diodes with internal EPD TVS diode
- Protects two I/O lines
- Low capacitance (<10pF) for high-speed interfaces
- Low leakage current (< 1µA)
- Low operating voltage: 2.8V
- Solid-state technology

MECHANICAL CHARACTERISTICS

- JEDEC SOT-143 package
- Molding compound flammability rating: UL 94V-0
- Marking : R2.8
- Packaging : Tape and Reel per EIA 481

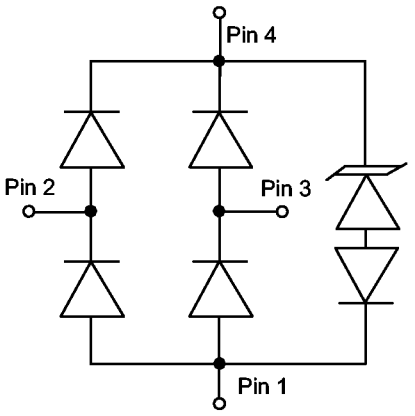
APPLICATIONS

- 10/100 Ethernet
- Firewire
- Sensitive Analog Inputs
- Video Line Protection
- Portable Electronics
- Microcontroller Input Protection
- WAN/LAN Equipment

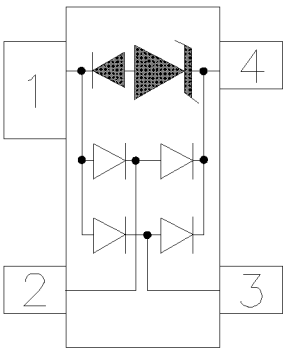
ORDERING INFORMATION

Part Number	Working Voltage	Qty per Reel	Reel Size
SR2.8.TC	2.8V	3,000	7"
SR2.8.TG	2.8V	10,000	13"

CIRCUIT DIAGRAM



SCHEMATIC & PIN CONFIGURATION



SOT-143 (Top View)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20μs)	P_{pk}	200	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	14	A
Peak Forward Voltage (IF=1A, tp=8/20μs)	V_{FP}	1.5	V
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS

SR2.8

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				2.8	V
Punch-Through Voltage	V_{PT}	I_{PT} = 2μA	3.0			V
Snap-Back Voltage	V_{SB}	I_{SB} = 50mA	2.8			V
Reverse Leakage Current	I_R	V_{RWM} = 2.8V, T=25°C			1	μA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs			5.0	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20μs			8.5	V
Maximum Peak Pulse Current	I_{PP}	tp = 8/20μs			14	A
Junction Capacitance	C_j	Between I/O pins and Gnd V_R = 0V, f = 1MHz		6	10	pF
		Between I/O pins V_R = 0V, f = 1MHz		3		pF

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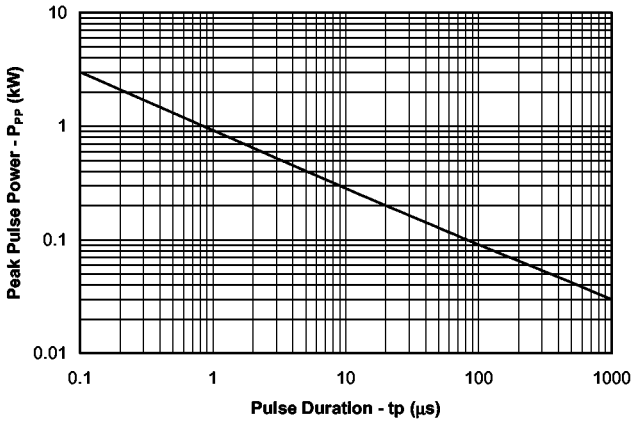
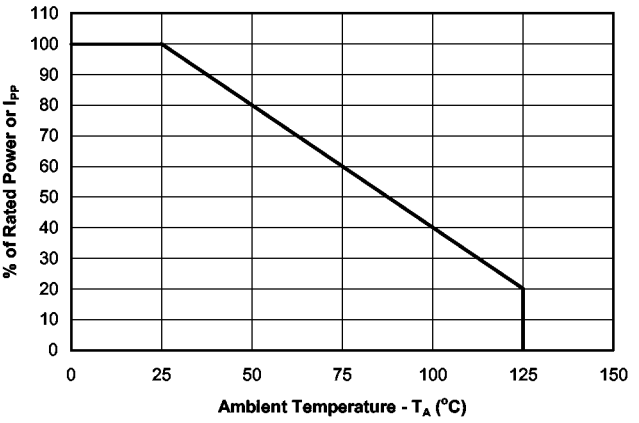
TYPICAL CHARACTERISTICS

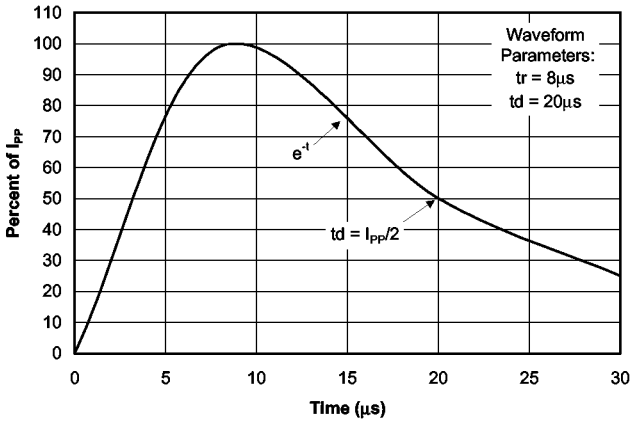
Non-Repetitive Peak Pulse Power vs. Pulse Time



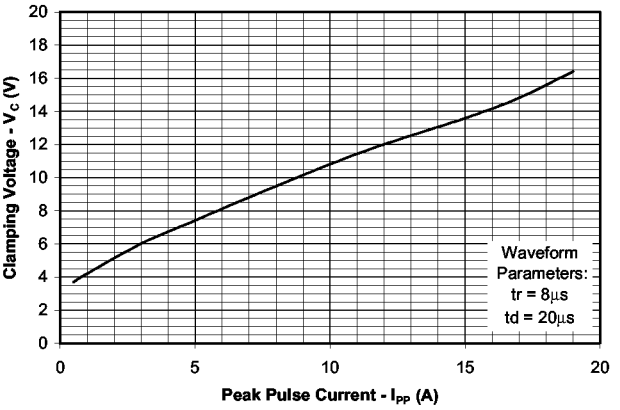
Power Derating Curve



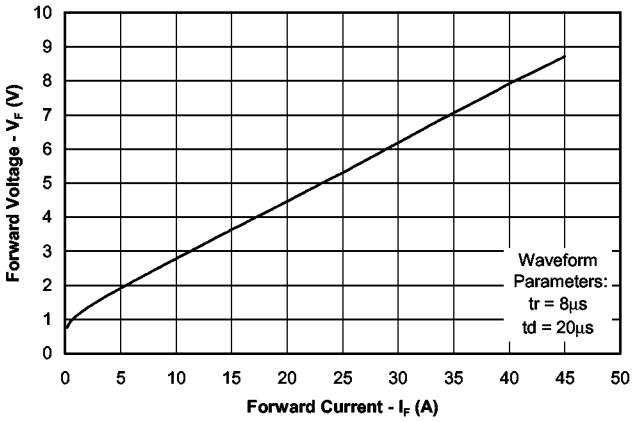
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Forward Voltage vs. Forward Current

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APPLICATIONS INFORMATION

Device Connection Options for Protection of Two High-Speed Data Lines

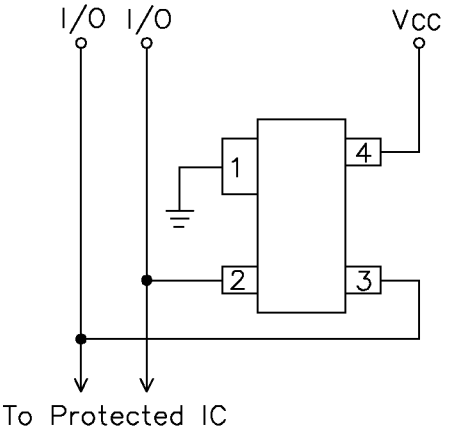
The SR2.8 TVS is designed to protect two data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 2 and 3. The negative reference (REF1) is connected at pin 1. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (REF2) is connected at pin 4. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 4 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. The SR2.8 can be isolated from the power supply by adding a series resistor between pin 4 and V_{CC}. A value of 10kΩ is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

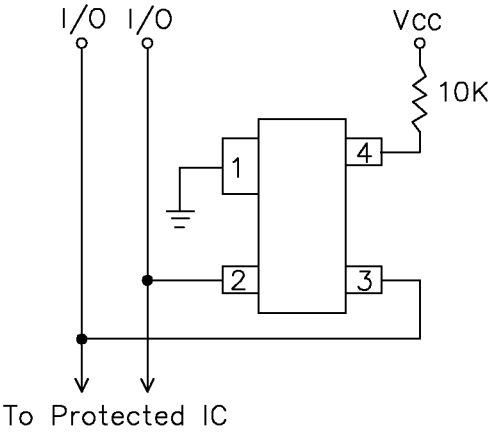
Board Layout Considerations for ESD Protection

Board layout plays an important role in the suppression of extremely fast rise-time ESD transients. Recall that the voltage developed across an inductive load is proportional to the time rate of change of current through the load (V = Ldi/dt). The total clamping voltage seen by the protected load will be the sum of the TVS clamping voltage and the voltage due to the parasitic inductance ($V_{C(TOT)} = V_C + L\ di/dt$) . ***Parasitic inductance in the protection path can result in significant voltage overshoot, reducing the effectiveness of the suppression circuit.*** An ESD induced transient for example reaches a peak in approximately 1ns. For a 30A pulse (per IEC 1000-4-2

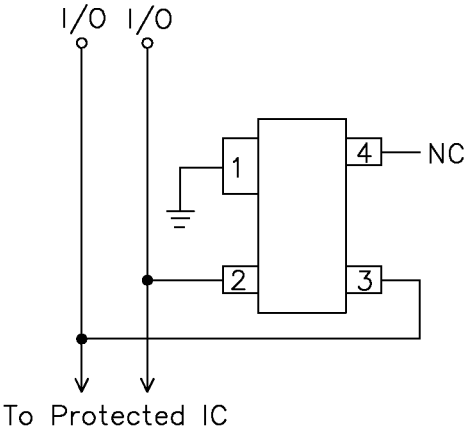
Data Line and Power Supply Protection Using Vcc as reference



Data Line Protection with Bias and Power Supply Isolation Resistor



Data Line Protection Using Internal TVS Diode as Reference



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APPLICATIONS INFORMATION

Level 4), 1nH of series inductance will increase the effective clamping voltage by 30V ($V = 1x10^{-9}$ ($30/1x10^{-9}$)). For maximum effectiveness, the following board layout guidelines are recommended:

- Minimize the path length between the SR2.8 and the protected line.
- Place the SR2.8 near the RJ45 connector to restrict transient coupling in nearby traces.
- Minimize the path length (inductance) between the RJ45 connector and the SR2.8.

EPD TVS Characteristics

The internal TVS of the SR2.8 is constructed using Semtech's proprietary EPD technology. The structure of the EPD TVS is vastly different from the traditional pn-junction devices. At voltages below 5V, high leakage current and junction capacitance render conventional avalanche technology impractical for most applications. However, by utilizing the EPD technology, the SR2.8 can effectively operate at 2.8V while maintaining excellent electrical characteristics.

The EPD TVS employs a complex nppn structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. The EPD mechanism is achieved by engineering the center region of the device such that the reverse biased junction does not avalanche, but will "punch-through" to a conducting state. This structure results in a device with superior dc electrical parameters at low voltages while maintaining the capability to absorb high transient currents.

The IV characteristic curve of the EPD device is shown in Figure 1. The device represents a high impedance to the circuit up to the working voltage (V_{RWM}). During a transient event, the device will begin to conduct as it is biased in the reverse direction. When the punch-through voltage (V_{PT}) is exceeded, the device enters a low impedance state, diverting the transient current away from the protected circuit. When the device is conducting current, it will exhibit a slight "snap-back" or negative resistance characteristic due to its structure. This must be considered when connecting the device to a power supply rail. To return to a non-conducting state, the current through the device must fall below the snap-back current (approximately < 50mA).

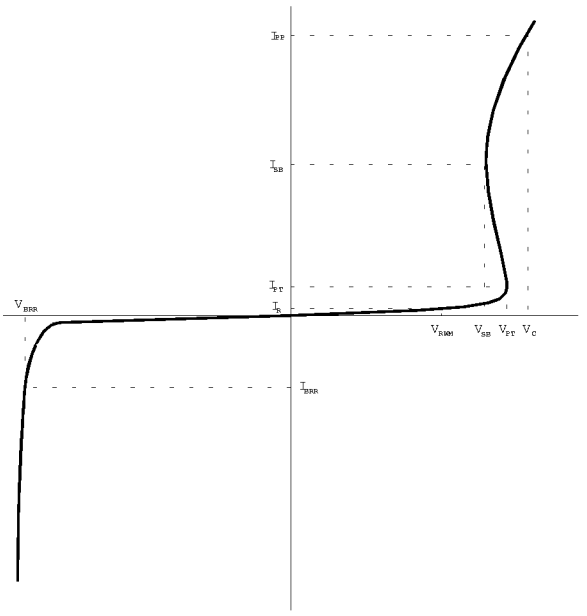

Figure 1 - EPD TVS IV Characteristic Curve

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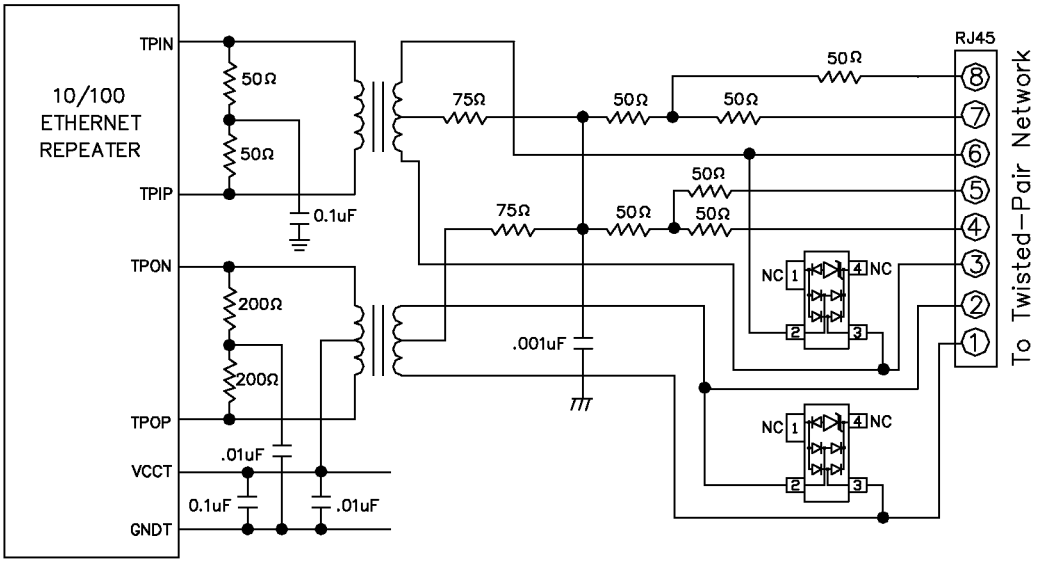
TYPICAL APPLICATIONS



10/100 Ethernet ESD Protection

10/100 Ethernet ICs are vulnerable to damage from electrostatic discharge (ESD). The fatal discharge may originate from a charged cable (cable discharge event or CDE) or the body of a user. Charges can exceed several thousand volts under the right conditions. If the circuit is left unprotected, the voltage will be capacitively coupled thru the transformer, potentially damaging or latching-up the Ethernet Phy chip. The figure above illustrates how to use the SR2.8 to protect one 10/100 Ethernet line pair. The devices are connected differentially between transmit and receive line pairs. When the voltage on the data lines exceeds the TVS punch-through (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected chip. The design takes advantage of the isolation provided by the line transformer to suppress common mode surges.

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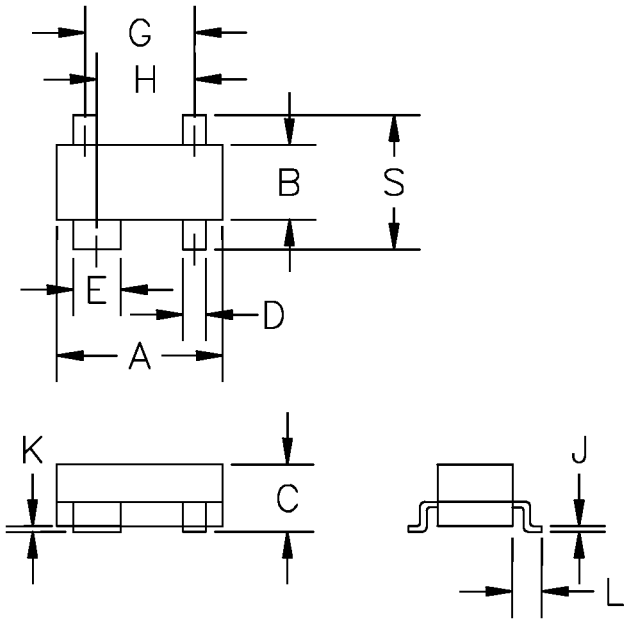
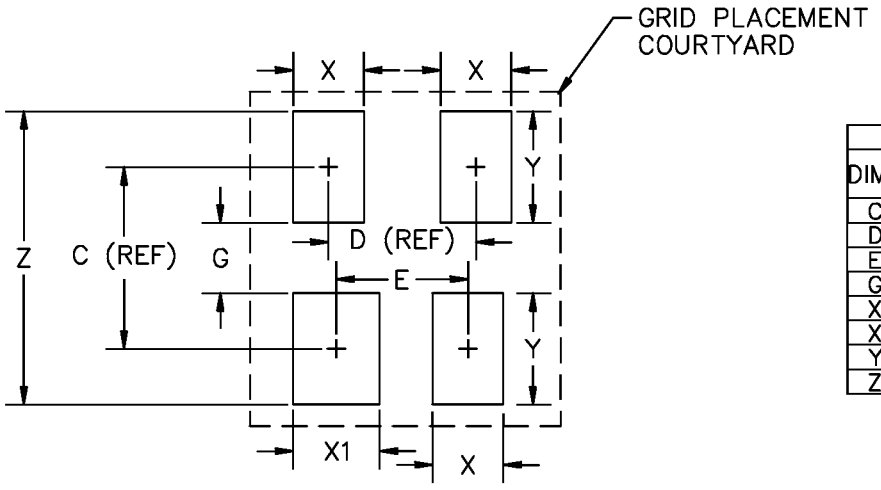
OUTLINE DRAWING - SOT-143



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.120	2.80	3.04	–
B	.047	.055	1.20	1.40	–
C	.031	.047	.80	1.20	–
D	.014	.018	.37	.510	–
E	.030	.035	.76	.940	–
G	.076 BSC		1.92 BSC		–
H	.068 BSC		1.72 BSC		–
J	.003	.005	.085	.180	–
K	.002	.005	.013	0.10	–
L	.010	.022	–	.55	REF
S	.082	.104	2.10	2.64	–

Notes:
(1) Controlling dimension: Inch (unless otherwise specified).
(2) Dimension A and B do not include mold protrusions. Mold protrusions are .006" max.

LAND PATTERN - SOT-143



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.087	–	2.20	–
D	.075 BSC		1.90 BSC		–
E	.067 BSC		1.70 BSC		–
G	.032	.040	.80	1.00	–
X	.032	.040	.80	1.00	–
X1	.040	.048	1.00	1.20	–
Y	–	.057	–	1.44	–
Z	.134	.140	3.40	3.60	–

Notes:
(1) Controlling dimension is millimeters.
(2) Grid placement courtyard is 8 x 8 elements (4mm x 4mm) in accordance with the international grid detailed in IEC publication 97.