

IRF2807S

IRF2807L

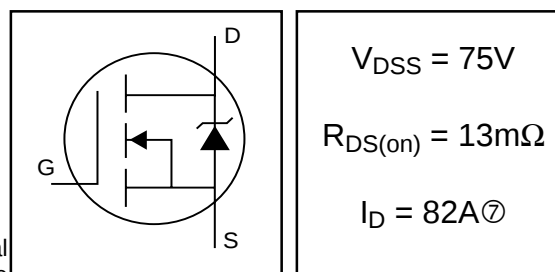
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications. The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

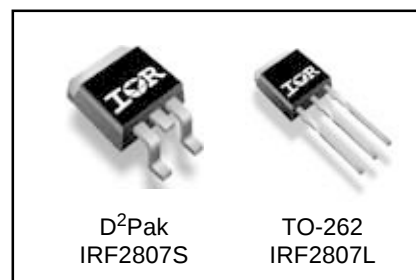
The through-hole version (IRF2807L) is available for low-profile applications.



$$V_{DS} = 75V$$

$$R_{DS(on)} = 13m\Omega$$

$$I_D = 82A \textcircled{7}$$



D²Pak
IRF2807S

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Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	82 $\textcircled{7}$	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	58	
I_{DM}	Pulsed Drain Current $\textcircled{1}$	280	
$P_D @ T_C = 25^\circ C$	Power Dissipation	230	W
	Linear Derating Factor	1.5	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current $\textcircled{1}$	43	A
E_{AR}	Repetitive Avalanche Energy $\textcircled{1}$	23	mJ
dv/dt	Peak Diode Recovery dv/dt $\textcircled{3}$	5.9	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	75	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.074	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	13	mΩ	V _{GS} = 10V, I _D = 43A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	38	—	—	S	V _{DS} = 50V, I _D = 43A④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 75V, V _{GS} = 0V
		—	—	250	μA	V _{DS} = 60V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V _{GS} = -20V
Q _g	Total Gate Charge	—	—	160	nC	I _D = 43A
Q _{gs}	Gate-to-Source Charge	—	—	29	nC	V _{DS} = 60V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	55	nC	V _{GS} = 10V, See Fig. 6 and 13
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = 38V
t _r	Rise Time	—	64	—	ns	I _D = 43A
t _{d(off)}	Turn-Off Delay Time	—	49	—	ns	R _G = 2.5Ω
t _f	Fall Time	—	48	—	ns	V _{GS} = 10V, See Fig. 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—	nH	
C _{iss}	Input Capacitance	—	3820	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	610	—	pF	V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	130	—	pF	f = 1.0MHz, See Fig. 5
E _{AS}	Single Pulse Avalanche Energy②	—	1280⑤	340⑥	mJ	I _{AS} = 50A, L = 370μH

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	82⑦	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode)①	—	—	280	A	
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 43A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	100	150	ns	T _J = 25°C, I _F = 43A
Q _{rr}	Reverse Recovery Charge	—	410	610	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

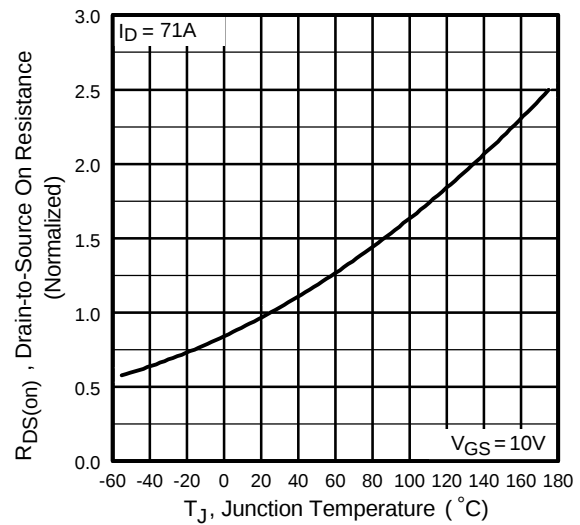
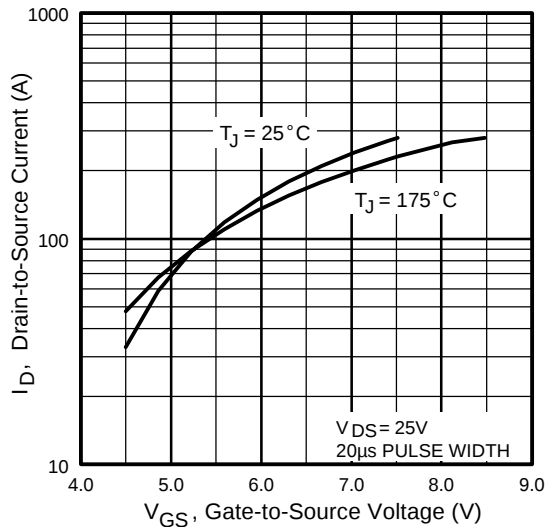
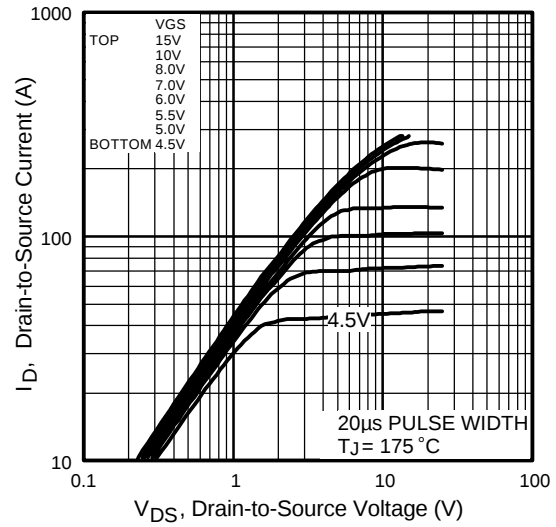
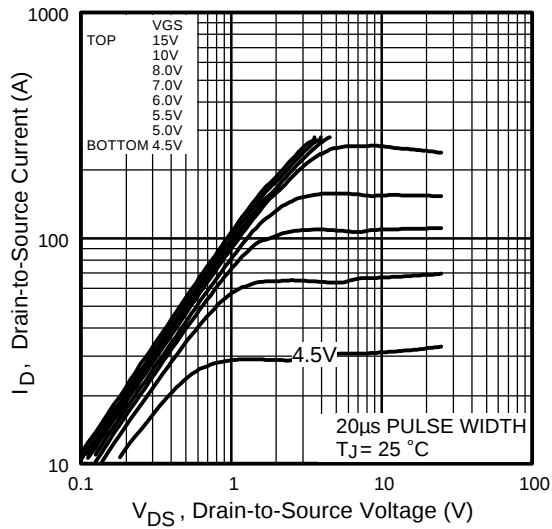
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 370μH
R_G = 25Ω, I_{AS} = 43A, V_{GS} = 10V (See Figure 12)
- ③ I_{SD} ≤ 43A, di/dt ≤ 300A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C.

⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

**When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994



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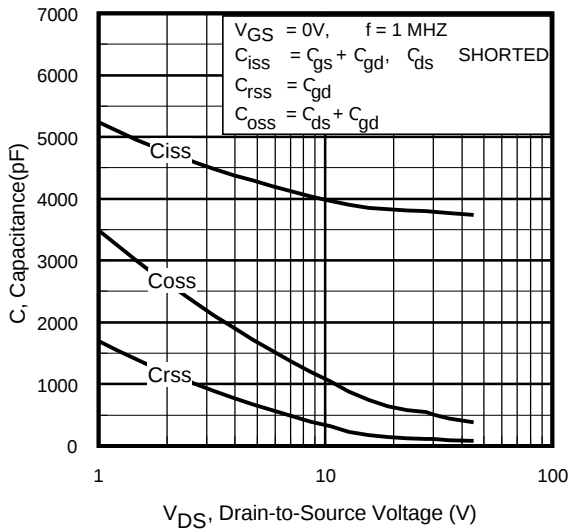


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

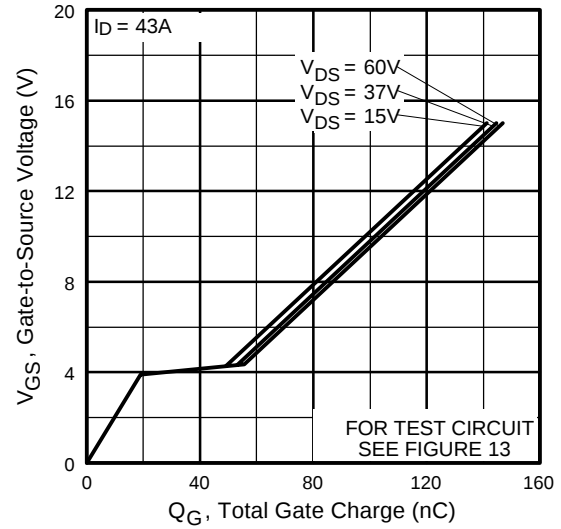


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

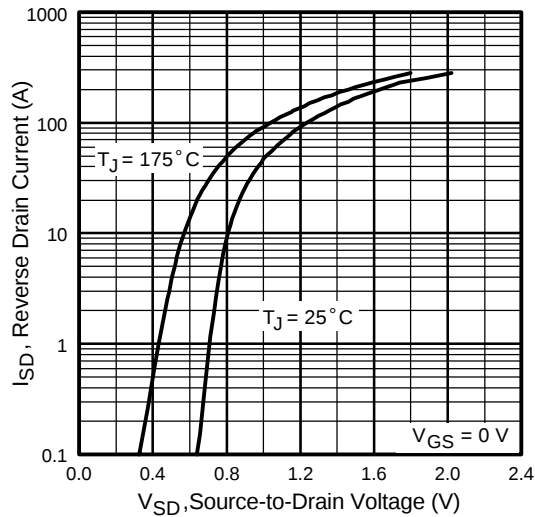


Fig 7. Typical Source-Drain Diode Forward Voltage

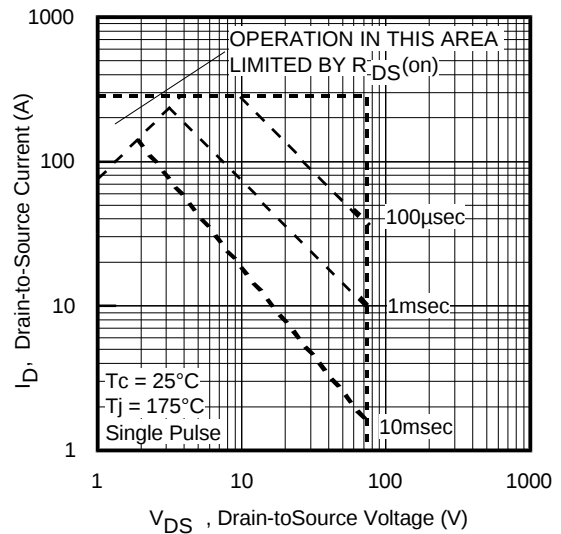


Fig 8. Maximum Safe Operating Area

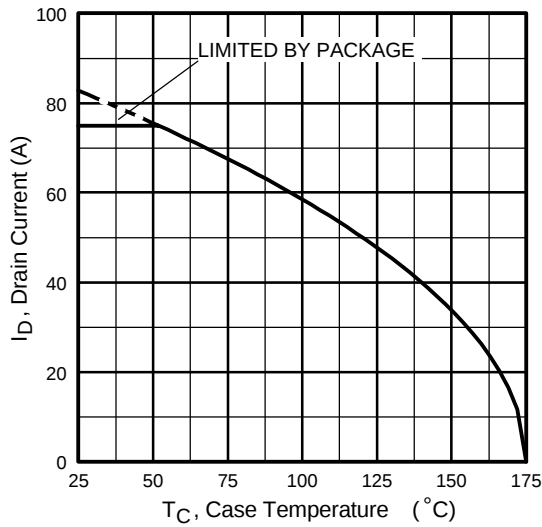


Fig 9. Maximum Drain Current Vs. Case Temperature

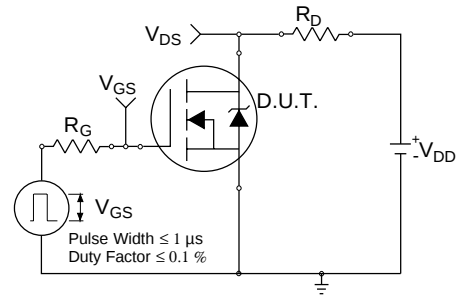


Fig 10a. Switching Time Test Circuit

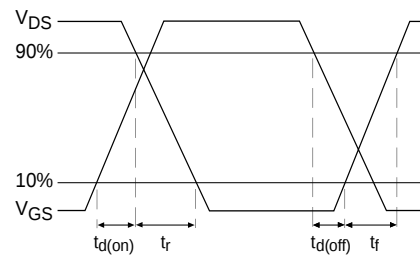


Fig 10b. Switching Time Waveforms

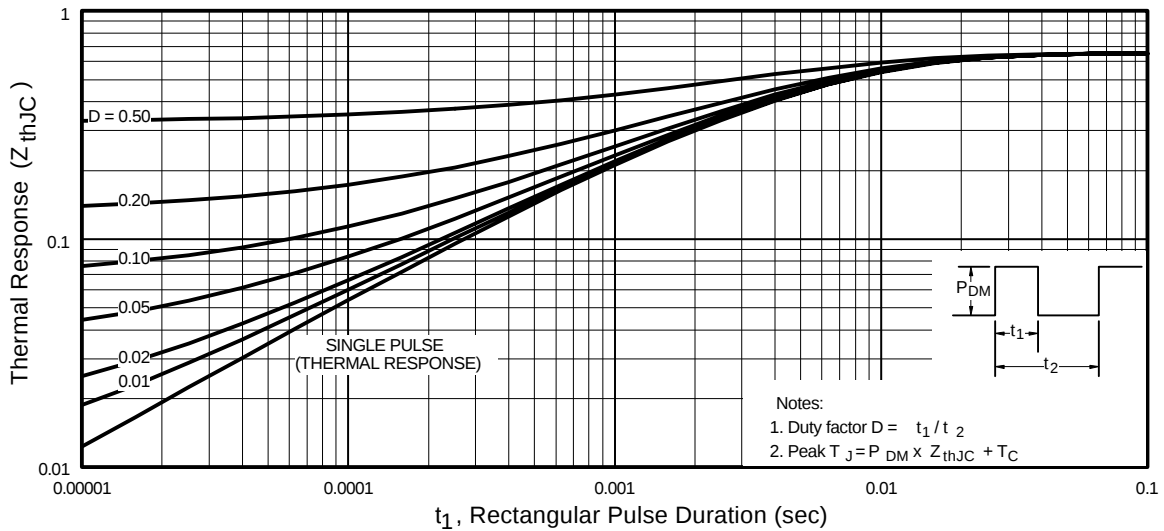


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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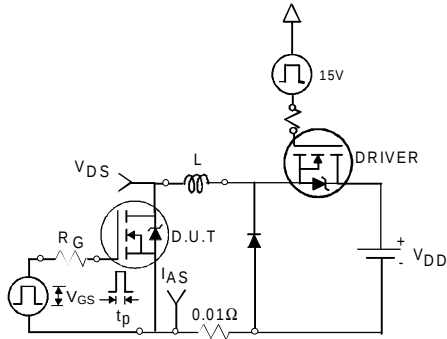


Fig 12a. Unclamped Inductive Test Circuit

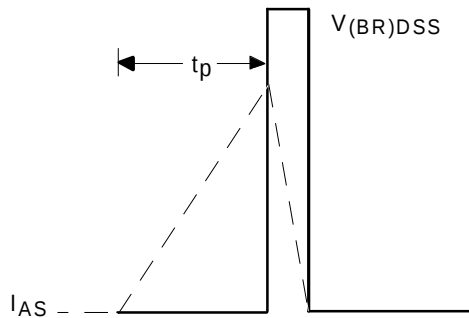


Fig 12b. Unclamped Inductive Waveforms

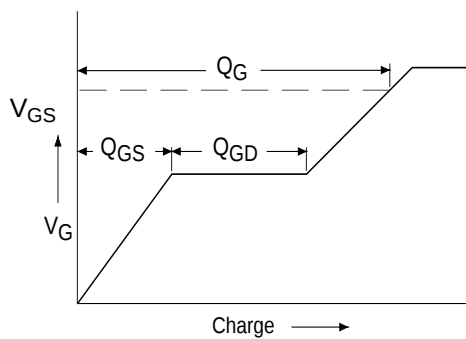


Fig 13a. Basic Gate Charge Waveform

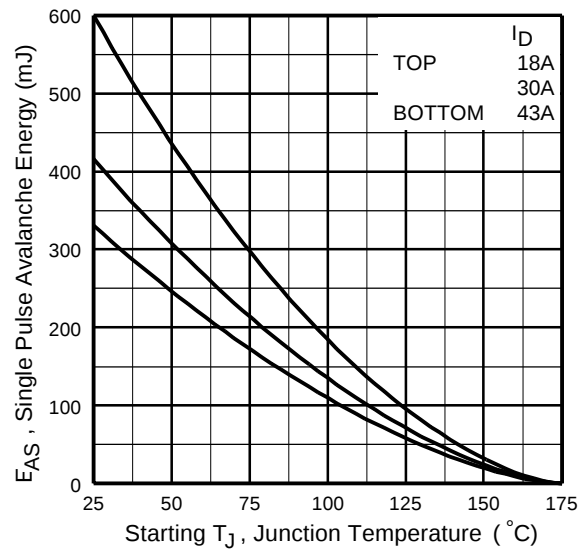


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

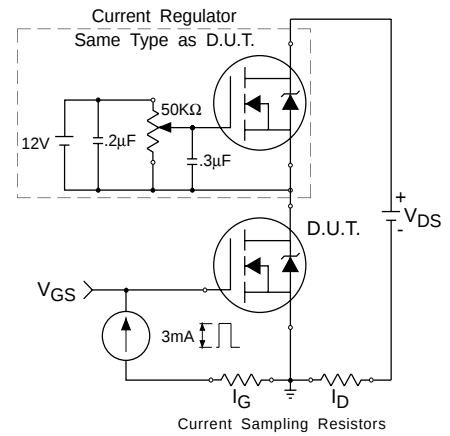
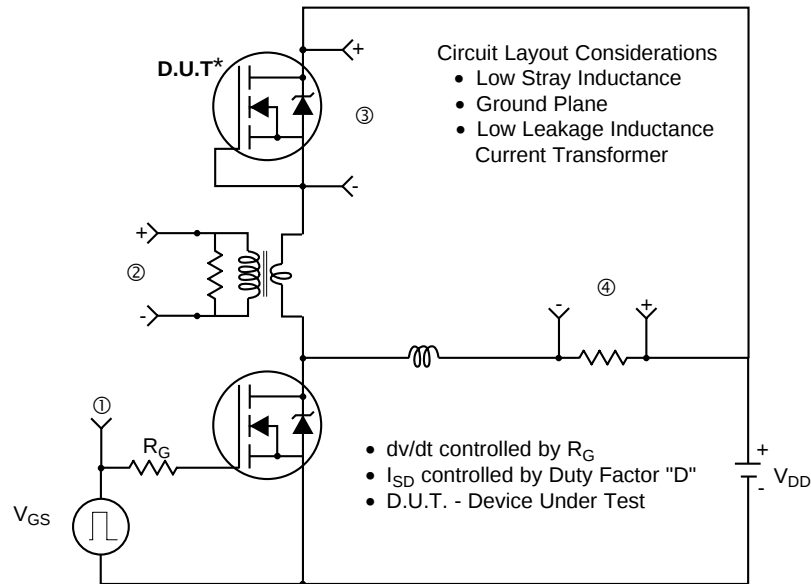
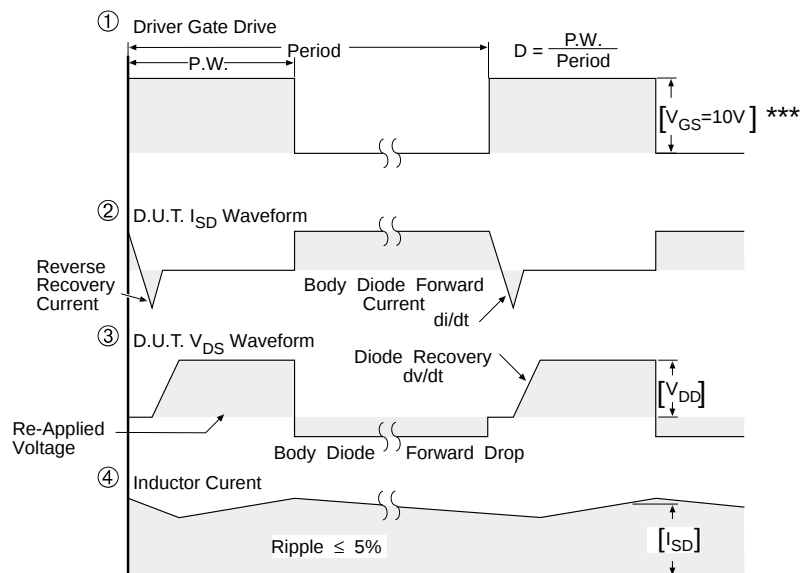


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



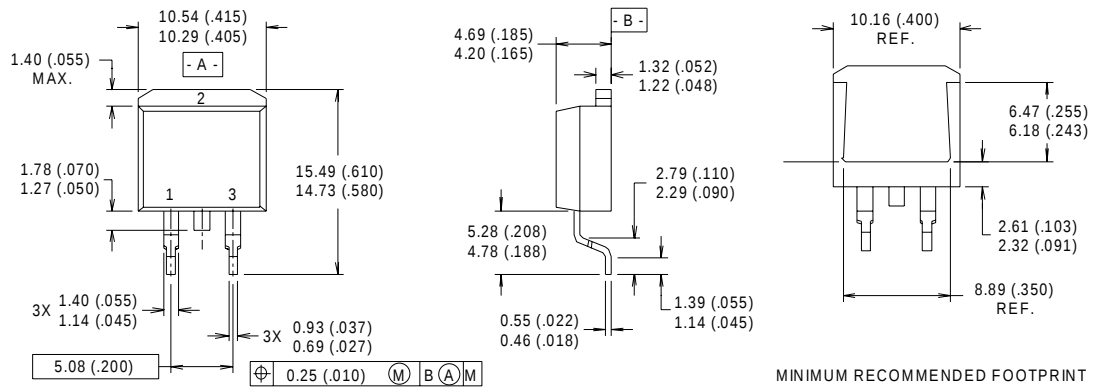
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline



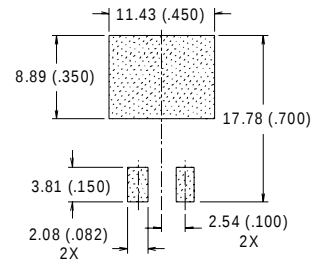
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

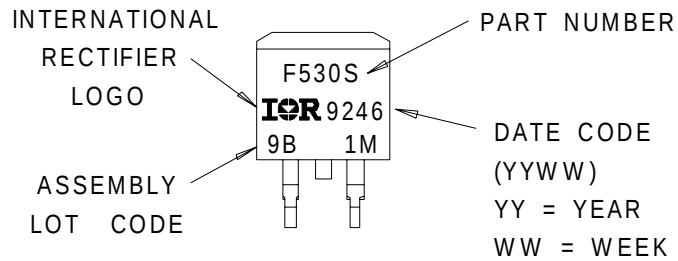
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

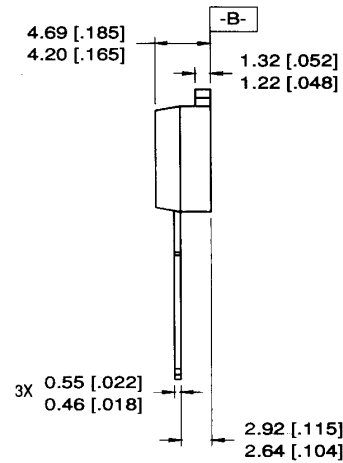
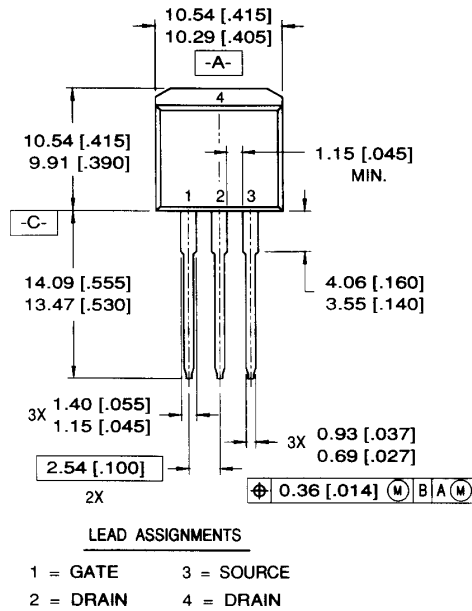
MINIMUM RECOMMENDED FOOTPRINT



D²Pak Part Marking Information



TO-262 Package Outline

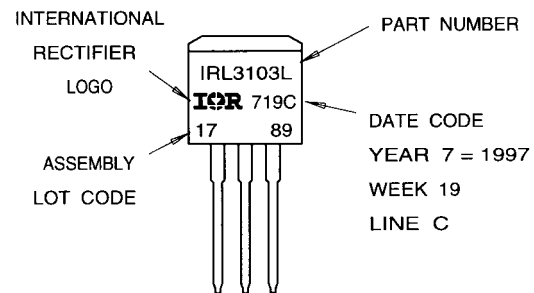


NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



International
IOR Rectifier

TRR

FEED DIRECTION →

TRL

FEED DIRECTION →

1.60 (.063)
1.50 (.059)
4.10 (.161)
3.90 (.153)
1.85 (.073)
1.65 (.065)
11.60 (.457)
11.40 (.449)
1.60 (.063)
1.50 (.059)
11.60 (.457)
11.40 (.449)
1.75 (.069)
1.25 (.049)
16.10 (.634)
15.90 (.626)
0.368 (.0145)
0.342 (.0135)
15.42 (.609)
15.22 (.601)
24.30 (.957)
23.90 (.941)
4.72 (.136)
4.52 (.178)
13.50 (.532)
Ø 12.80 (.504)
Ø 330.00 (14.173) MAX.
27.40 (1.079)
23.90 (.941)
Ø 60.00 (2.362) MIN.
30.40 (1.197) MAX.
26.40 (1.039)
24.40 (.961)

NOTES :

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>