

## 2-Mbit (128K x 16) Static RAM

### Features

- **Temperature Ranges**
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive: -40°C to 125°C
- **High Speed: 55 ns and 70 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Ultra-low active, standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package Available in a standard 44-pin TSOP Type II (forward pinout) package**

### Functional Description<sup>[1]</sup>

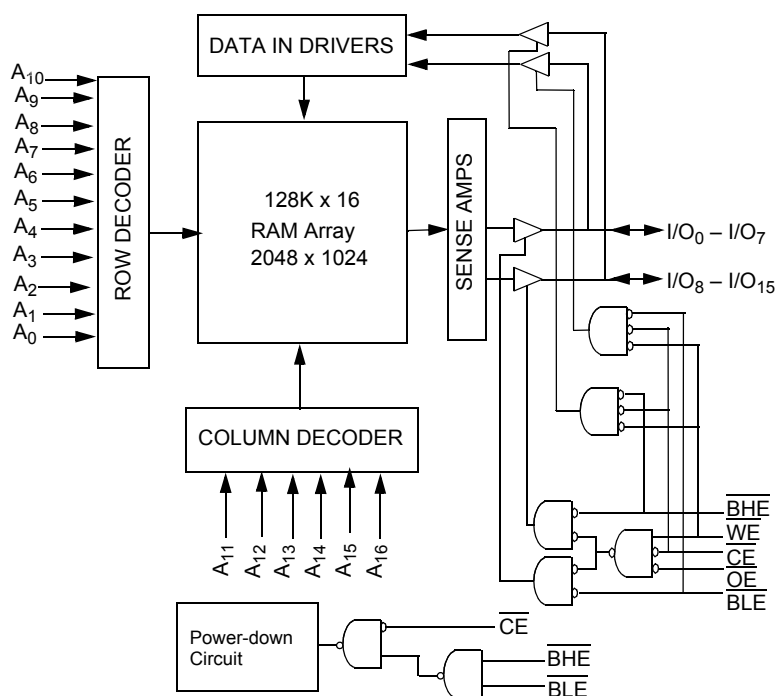
The CY62137V is a high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life® (MoBL®) in portable applications such as cellular telephones. The device

also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}$  HIGH) or when  $\overline{CE}$  is LOW and both BLE and BHE are HIGH. The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}$  HIGH), outputs are disabled ( $\overline{OE}$  HIGH), BHE and BLE are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.

### Logic Block Diagram



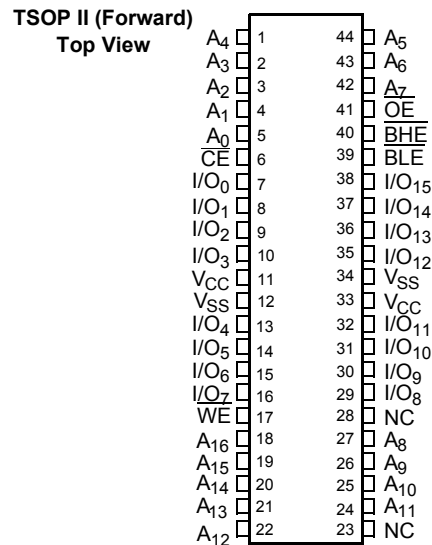
#### Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

## Product Portfolio

Product		V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation			
						Operating, I <sub>CC</sub> (mA)		Standby, I <sub>SB2</sub> (μA)	
		Min.	Typ. <sup>[3]</sup>	Max.		Typ. <sup>[3]</sup>	Max.	Typ. <sup>[3]</sup>	Max.
CY62137VLL	Industrial	2.7	3.0	3.6	55	7	20	1	15
CY62137VSL					55	7	20	1	5
CY62137VLL					70	7	15	1	15
CY62137VSL					70	7	15	1	5
CY62137VLL	Automotive				70	7	15	1	20

## Pin Configurations



## Pin Definitions

Pin Number	Type	Description
1-5, 18-22, 24-27, 42-45	Input	<b>A<sub>0</sub>-A<sub>16</sub></b> . Address Inputs
7-10, 13-16, 29-32, 35-38	Input/Output	<b>I/O<sub>0</sub>-I/O<sub>15</sub></b> . Data lines. Used as input or output lines depending on operation
23	No Connect	<b>NC</b> . This pin is not connected to the die
17	Input/Control	<b>WE</b> . When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
6	Input/Control	<b>CE</b> . When LOW, selects the chip. When HIGH, deselects the chip
39, 40	Input/Control	<b>BHE, BLE</b> . BHE = LOW selects higher order byte WRITES or READs on the SRAM. BLE = LOW selects lower order byte WRITES or READs on the SRAM
41	Input/Control	<b>OE</b> . Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins
12, 34	Ground	<b>V<sub>ss</sub></b> . Ground for the device
11, 33	Power Supply	<b>V<sub>cc</sub></b> . Power supply for the device

### Notes:

- NC pins are not connected on the die.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(TYP)</sub>, T<sub>A</sub> = 25°C.

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +4.6V

DC Voltage Applied to Outputs  
in High-Z State<sup>[4]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[4]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Industrial	-40°C to +85°C	2.7V to 3.6V
Automotive	-40°C to +125°C	2.7V to 3.6V

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62137V-55			CY62137V-70			Unit
			Min.	Typ. <sup>[3]</sup>	Max.	Min.	Typ. <sup>[3]</sup>	Max.	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -1.0 \text{ mA}$ , $V_{CC} = 2.7V$	2.4			2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 2.1 \text{ mA}$ , $V_{CC} = 2.7V$			0.4			0.4	V
$V_{IH}$	Input HIGH Voltage		2.2		$V_{CC} + 0.5V$	2.2		$V_{CC} + 0.5V$	V
$V_{IL}$	Input LOW Voltage		-0.5		0.8	-0.5		0.8	V
$I_{IX}$	Input Load Current	$GND \leq V_I \leq V_{CC}$	-1		+1	-1		+1	$\mu A$
$I_{OZ}$	Output Leakage Current	$GND \leq V_O \leq V_{CC}$ , Output Disabled	-1		+1	-1		+1	$\mu A$
$I_{CC}$	$V_{CC}$ Operating Supply Current	$I_{OUT} = 0 \text{ mA}$ , $f = f_{MAX} = 1/t_{RC}$ , CMOS Levels		7	20		7	15	mA
		$I_{OUT} = 0 \text{ mA}$ , $f = 1 \text{ MHz}$ , CMOS Levels		1	2		1	2	
$I_{SB1}$	Automatic CE Power-down Current— CMOS Inputs	$CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = f_{MAX}$			100			100	$\mu A$
$I_{SB2}$	Automatic CE Power-down Current— CMOS Inputs	$CE \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ , $f = 0$	$V_{CC} = 3.6V$	LL	1	15		1	15
				Automotive				1	20
				SL	1	5		1	5

## Capacitance<sup>[5]</sup>

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ C$ , $f = 1 \text{ MHz}$ , $V_{CC} = V_{CC}(\text{typ})$	6	pF
$C_{OUT}$	Output Capacitance		8	pF

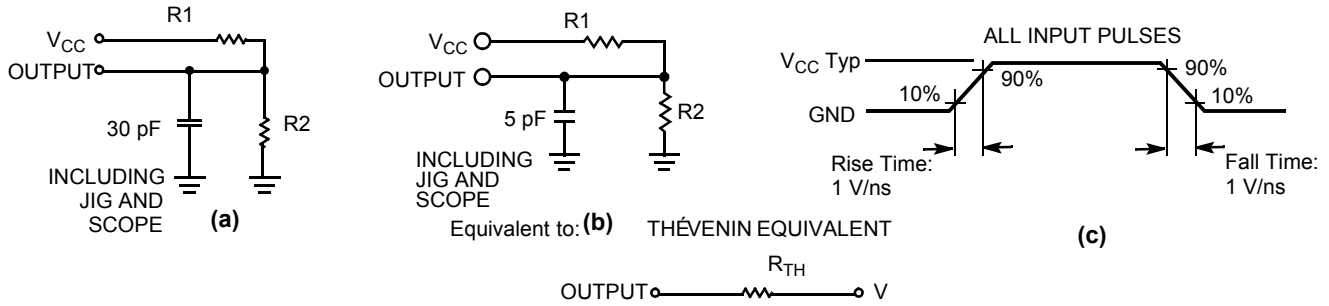
## Thermal Resistance

Description	Test Conditions	Symbol	TSOPII	Unit
Thermal Resistance (Junction to Ambient) <sup>[5]</sup>	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	$\Theta_{JA}$	60	$^\circ C/W$
Thermal Resistance (Junction to Case) <sup>[5]</sup>		$\Theta_{JC}$	22	$^\circ C/W$

### Notes:

- $V_{IL}(\text{min.}) = -2.0V$  for pulse durations less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

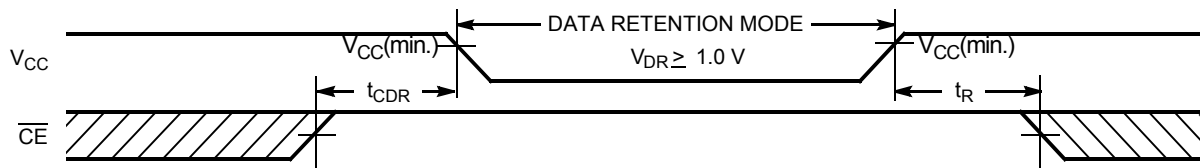


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
$R_{TH}$	645	Ohms
$V_{TH}$	1.75	Volts

## Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. <sup>[3]</sup>	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		1.0			V
$I_{CCDR}$	Data Retention Current	$V_{CC} = 1.0V, \overline{CE} \geq V_{CC} - 0.3V, V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ ; No input may exceed; $V_{CC} + 0.3V$		0.5	7.5	$\mu A$
		LL				
		Automotive			10	
		SL		0.5	5	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R$	Operation Recovery Time		70			ns

## Data Retention Waveform



**Switching Characteristics** Over the Operating Range <sup>[6]</sup>

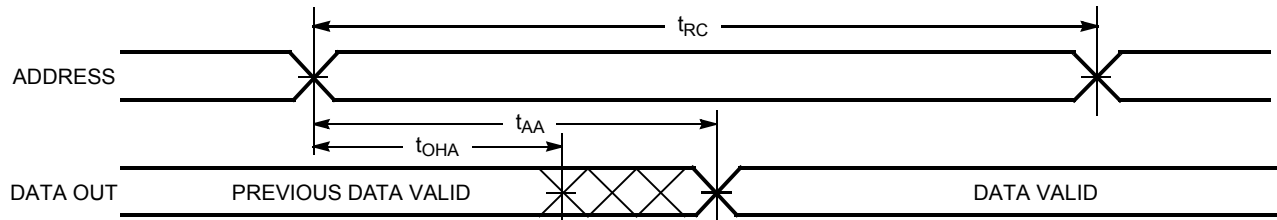
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	10		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low-Z <sup>[7]</sup>	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low-Z <sup>[7]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High-Z <sup>[7, 8]</sup>		25		25	ns
t <sub>PU</sub>	$\overline{CE}$ LOW to Power-up	0		0		ns
t <sub>PD</sub>	$\overline{CE}$ HIGH to Power-down		55		70	ns
t <sub>DBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub> <sup>(9)</sup>	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low-Z	5		5		ns
t <sub>HZBE</sub>	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High-Z		25		25	ns
Write Cycle <sup>[10, 11]</sup>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		50		ns
t <sub>SD</sub>	Data Set-up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High-Z <sup>[7, 8]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low-Z <sup>[7]</sup>	5		10		ns
t <sub>BW</sub>	$\overline{BHE}$ / $\overline{BLE}$ LOW to End of Write	50		60		ns

**Notes:**

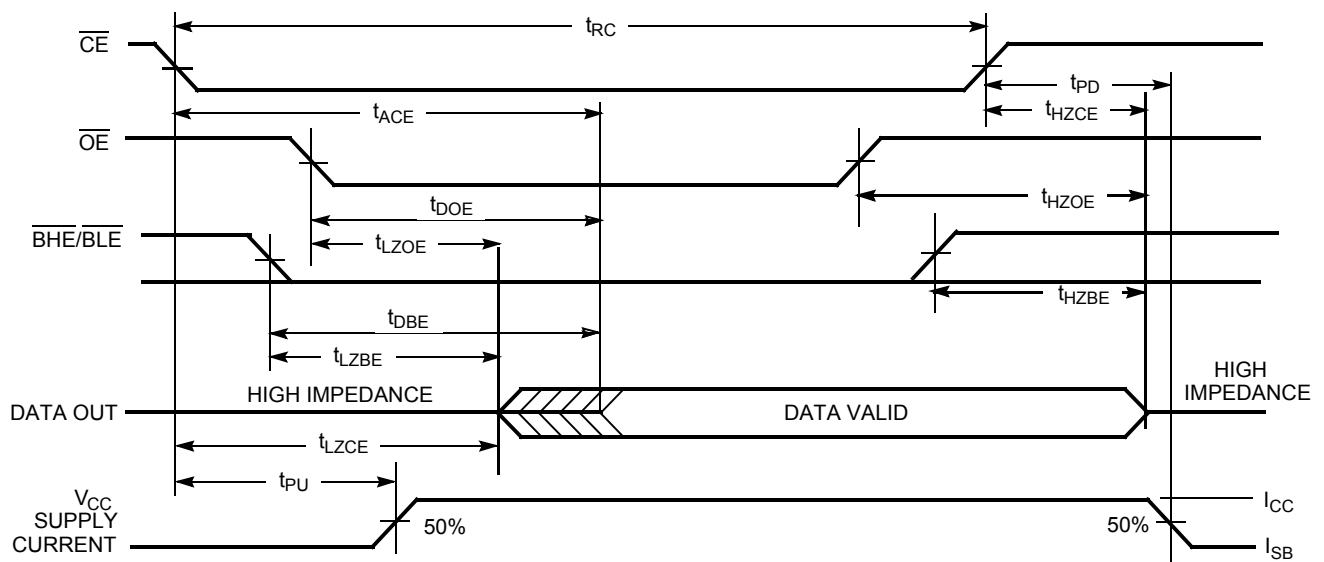
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to  $V_{CC}$  typ., and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- If both byte enables are toggled together this value is 10 ns.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

### Read Cycle No. 1<sup>[12, 13]</sup>

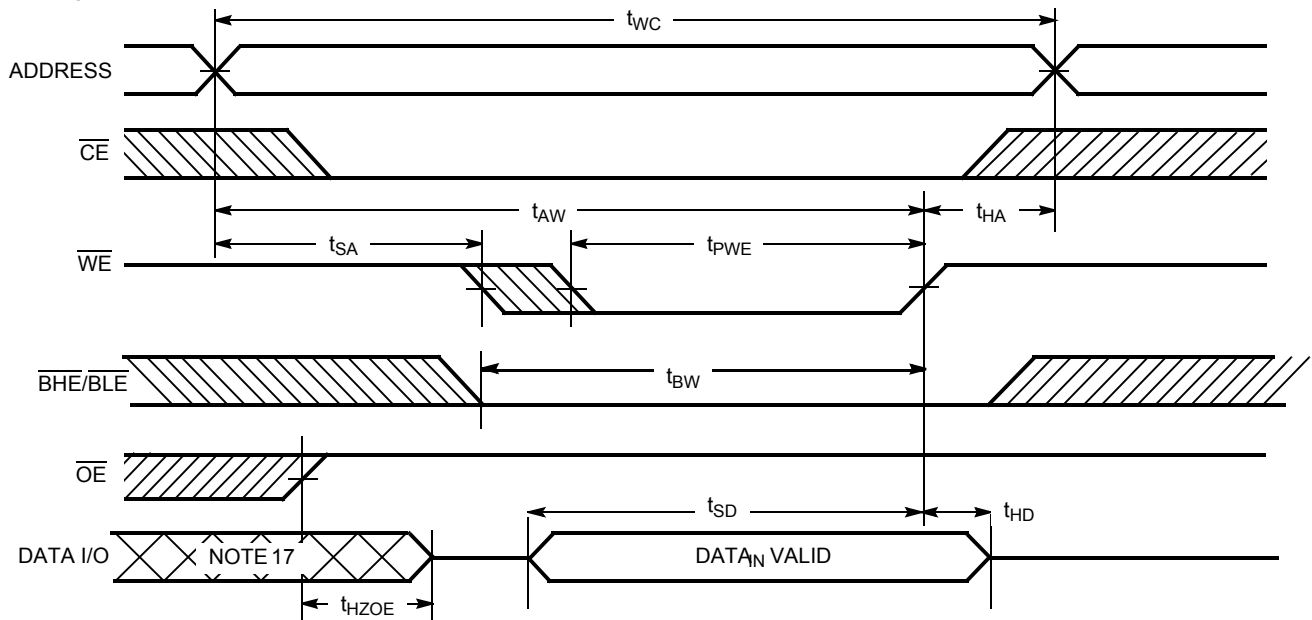
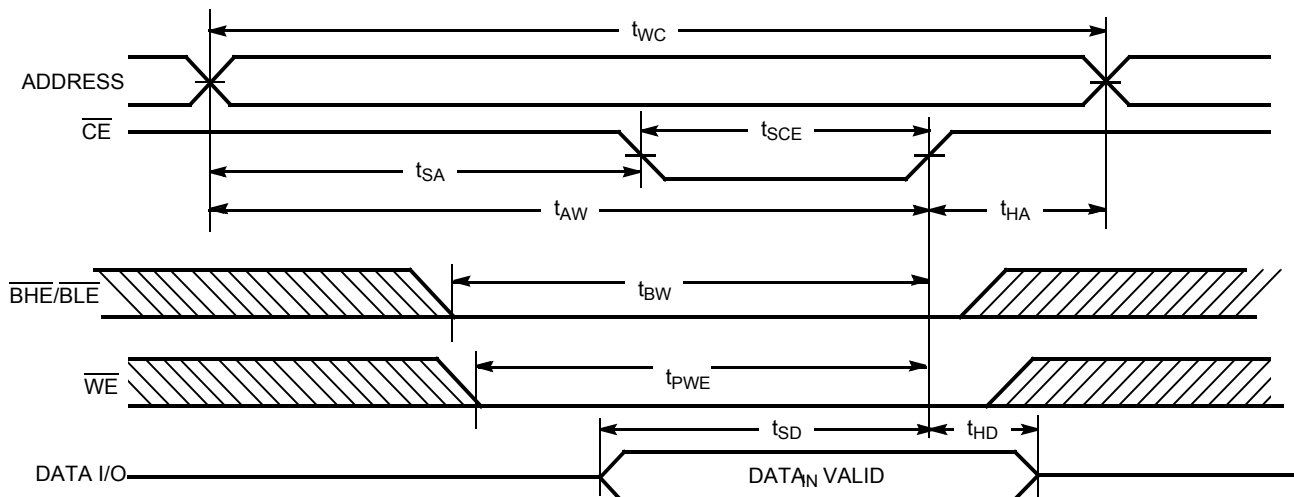


### Read Cycle No. 2<sup>[13, 14]</sup>

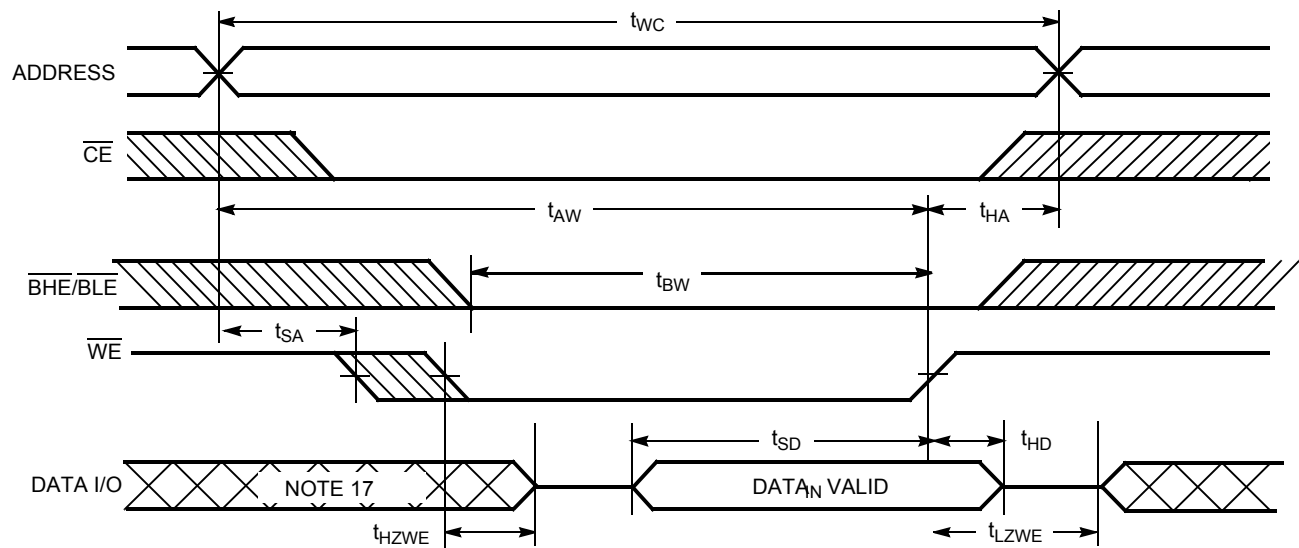
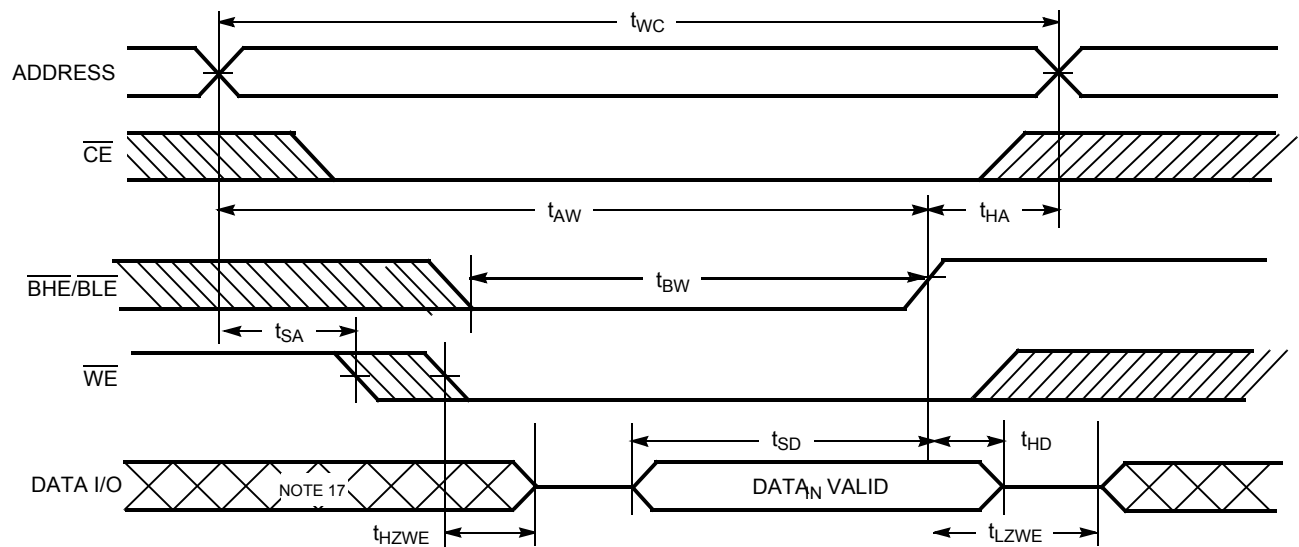


#### Notes:

12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
13.  $\overline{WE}$  is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

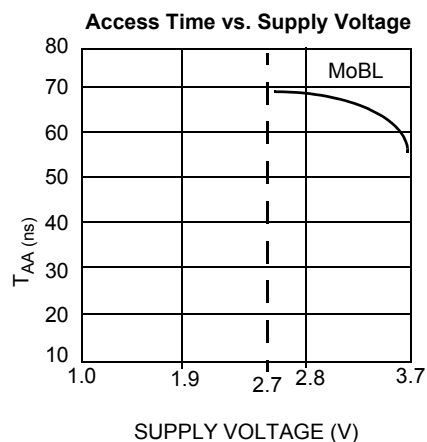
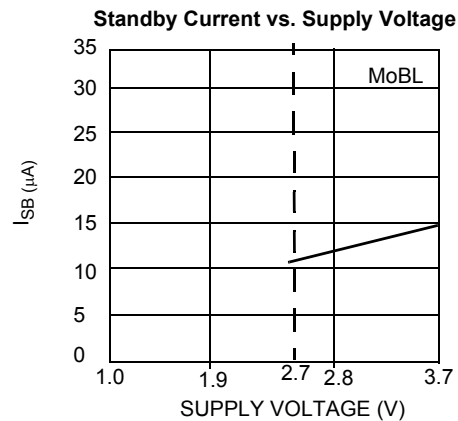
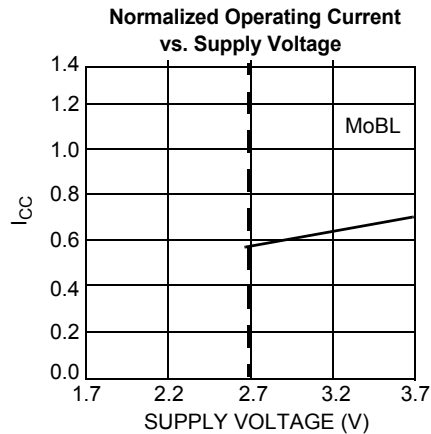
**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** <sup>[10, 15, 16]</sup>

**Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** <sup>[10, 15, 16]</sup>

**Notes:**

15. Data I/O is high-impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
16. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

**Switching Waveforms (continued)**
**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[11, 16]</sup>**

**Write Cycle No. 4 ( $\overline{\text{BHE/BL}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[17]</sup>**




## Typical DC and AC Characteristics



## Truth Table

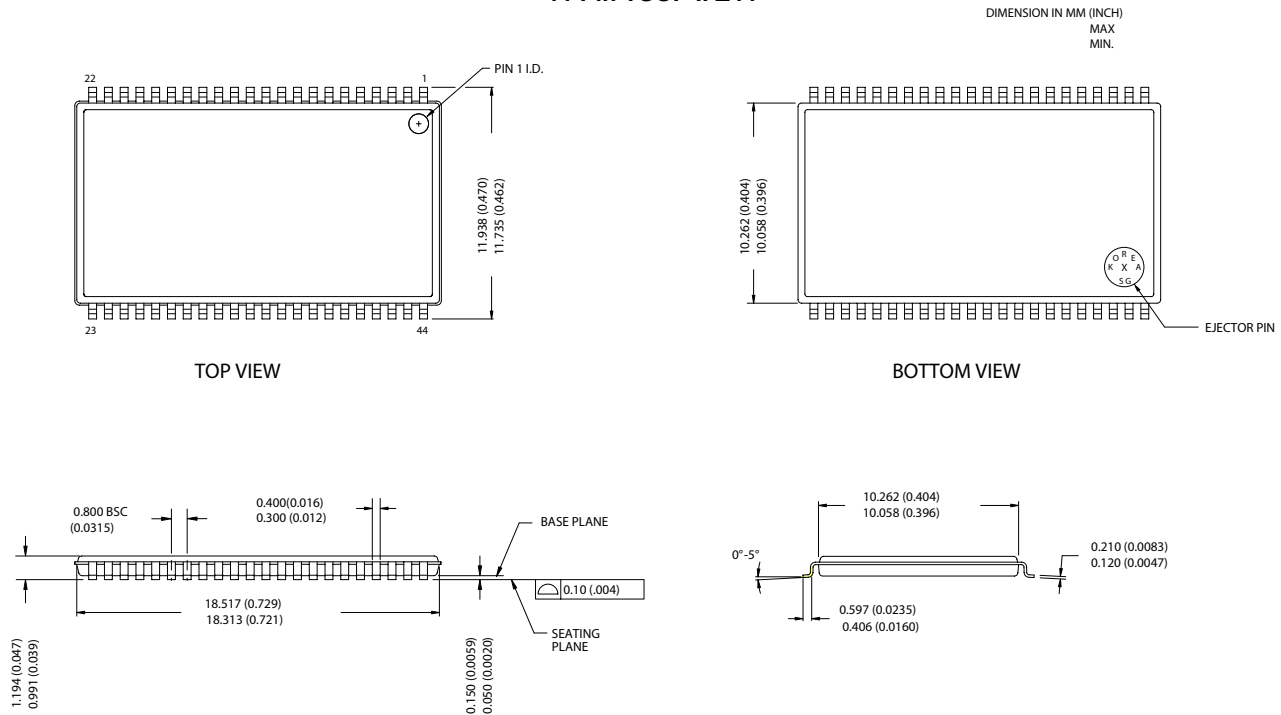
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	X	X	H	H	High-Z	Deselect/Power-down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	L	L	H	Data Out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High-Z	Read	Active ( $I_{CC}$ )
L	H	H	L	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	H	High-Z	Deselect/Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High-Z	Write	Active ( $I_{CC}$ )
L	L	X	L	H	Data In ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High-Z	Write	Active ( $I_{CC}$ )

## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62137VLL-55ZI	Z44	44-pin TSOP II	Industrial
	CY62137VSL-55ZI			
70	CY62137VLL-70ZI			
	CY62137VSL-70ZI			
	CY62137VLL-70ZE			Automotive

## Package Diagrams

### 44-Pin TSOP II Z44



51-85087-\*A

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**Document Title: CY62137V MoBL<sup>®</sup> 2M (128K x 16) Static RAM**  
**Document Number: 38-05051**

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109960	10/03/01	SZV	Changed from Spec number: 38-00738 to 38-05051
*A	116788	09/04/02	GBI	Added footnote number one. Added SL power bin. Deleted fBGA package; replacement fBGA package is available in CY62137CV30.
*B	237428	See ECN	AJU	Added Automotive product information