±14,000°/sec Digital Gyroscope Sensor

Data Sheet

ADIS16266

FEATURES

- Yaw rate gyroscope with range scaling
  - ±3500°/sec, ±7000°/sec, and ±14,000°/sec settings
- 2429 SPS sample rate
- Wide sensor bandwidth: 360 Hz
- No external configuration required to start data collection
  - Start-up time: 170 ms
  - Sleep mode recovery time: 2.5 ms
- Factory-calibrated sensitivity and bias
  - Calibration temperature range: −40°C to +70°C
- SPI-compatible serial interface
- Embedded temperature sensor
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Bartlett window FIR filter length, number of taps
  - Digital input/output: data ready, alarm indicator, general-purpose
  - Alarms for condition monitoring
  - Sleep mode for power management
  - DAC output voltage
  - Single-command self-test
- Single-supply operation: 4.75 V to 5.25 V
  - 3.3 V compatible digital lines
- 2000 *g* shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Platform control and stabilization
- Navigation
- Medical instrumentation
- Robotics

GENERAL DESCRIPTION

The ADIS16266 is a programmable digital gyroscope that combines industry-leading MEMS and signal processing technology in a single compact package. It provides accuracy performance that would otherwise require full motion calibration with any other MEMS gyroscope in this performance class. When power is applied, the ADIS16266 automatically starts up and begins sampling sensor data, without requiring configuration commands from a system processor. An addressable register structure and a common serial peripheral interface (SPI) provide simple access to sensor data and configuration settings. Many digital processor platforms support the SPI with simple firmware level instructions.

The ADIS16266 provides several programmable features for in-system optimization. The Bartlett window FIR filter length and sample rate settings provide users with controls that enable noise vs. bandwidth optimization. The digital input/output lines offer options for a data ready signal that helps the master processor efficiently manage data coherency, an alarm indicator signal for triggering master processor interrupts, and a general-purpose function for setting and monitoring system level digital controls/conditions.

The ADIS16266 is pin-compatible with the ADIS16265 and comes in an LGA package (11.2 mm × 11.2 mm × 5.5 mm) that meets Pb-free solder reflow profile requirements, per JEDEC J-STD-020. It offers an extended operating temperature range of −40°C to +105°C.

FUNCTIONAL BLOCK DIAGRAM

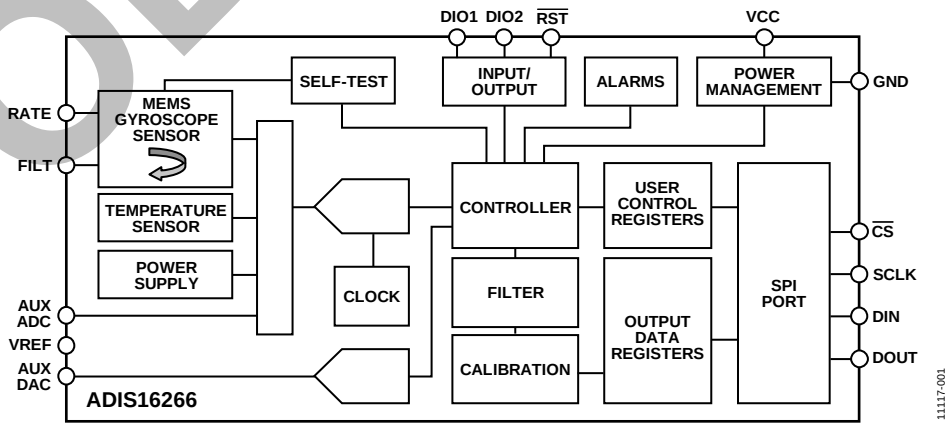

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

7/15—Rev. A to Rev. B

Change to Features Section ... 1

1/14—Rev. 0 to Rev. A

Changes to General Description Section ... 1

10/12—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +105°C, VCC = 5.0 V, angular rate = 0°/sec, ±1 *g*, ±14,000°/sec range setting, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSITIVITY[1]	Clockwise rotation is positive output				
	25°C, dynamic range = ±14,000°/sec[2]		4.17		°/sec/LSB
	25°C, dynamic range = ±7000°/sec		2.08		°/sec/LSB
	25°C, dynamic range = ±3500°/sec		1.04		°/sec/LSB
Initial Tolerance	25°C, dynamic range = ±14000°/sec, VDD = 5 V		±0.5	±2	%
Temperature Coefficient	4.75 V < VDD < 5.25 V		200		ppm/°C
Nonlinearity	Best fit straight line		0.1		% of FS
BIAS					
Initial Error			±15		°/sec
In-Run Bias Stability	25°C, 1 σ		470		°/hour
Angular Random Walk	25°C, 1 σ		21.5		°/√hour
Linear Acceleration Effect	25°C, 1 σ		0.1		°/sec/*g*
Temperature Coefficient			0.35		°/sec/°C
Voltage Sensitivity	VCC = 4.75 V to 5.25 V, μ ± 1 σ		7.5		°/sec/V
NOISE PERFORMANCE					
Output Noise	25°C, ±14,000°/sec range, no filtering		11.2		°/sec rms
	25°C, ±7000°/sec range, 4-tap filter setting		7.2		°/sec rms
	25°C, ±3500°/sec range, 16-tap filter setting		3.4		°/sec rms
Rate Noise Density	25°C, f = 25 Hz, ±14,000°/sec range, no filtering		0.44		°/sec/√Hz rms
FREQUENCY RESPONSE					
3 dB Bandwidth			360		Hz
Sensor Resonant Frequency		16	18	20	kHz
SELF-TEST STATE					
Change for Positive Stimulus	±14,000°/sec dynamic range setting	150		500	LSB
Change for Negative Stimulus	±14,000°/sec dynamic range setting	−500		−150	LSB
Internal Self-Test Cycle Time			30		ms
ADC INPUT					
Resolution			12		Bits
Integral Nonlinearity			±2		LSB
Differential Nonlinearity			±1		LSB
Offset Error			±4		LSB
Gain Error			±2		LSB
Input Range		0		2.5	V
Input Capacitance	During acquisition		20		pF
ON-CHIP VOLTAGE REFERENCE			2.5		V
Accuracy	25°C	−10		+10	mV
Temperature Coefficient			±40		ppm/°C
Output Impedance			70		Ω
DAC OUTPUT	5 kΩ/100 pF to GND				
Resolution			12		Bits
Relative Accuracy	For Code 101 to Code 4095		4		LSB
Differential Nonlinearity			1		LSB
Offset Error			±5		mV
Gain Error			±0.5		%
Output Range		0		2.5	V
Output Impedance			2		Ω
Output Settling Time			10		μs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS	Internal 3.3 V interface				
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±10	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V				
All Except $\overline{RST}$			−40	−60	µA
$\overline{RST}$	The $\overline{RST}$ pin has an internal pull-up.		−1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS	Internal 3.3 V interface				
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
SLEEP TIMER					
Timeout Period[3]		0.5		128	sec
START-UP TIME					
Initial Start-Up Time			170		ms
Sleep Mode Recovery			2.5		ms
Reset Recovery			78		ms
Flash Memory Update Time			40		ms
Flash Memory Test Time			18		ms
Self-Test Time			30		ms
FLASH MEMORY					
Endurance[4]		20,000			Cycles
Data Retention[5]	T_J = 55°C	10			Years
CONVERSION RATE					
Sample Rate			2429		SPS
Sample Rate Tolerance				±3	%
POWER SUPPLY					
Operating Voltage Range, V_{CC}		4.75	5.0	5.25	V
Power Supply Current			41		mA
	Sleep mode		400		µA

[1] Characterization data represents ±4σ to fall within the ±1% limit.
[2] The maximum guaranteed measurement range is ±14,000°/sec. The sensor outputs measure beyond this range, but performance is guaranteed.
[3] Guaranteed by design.
[4] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[5] Retention lifetime equivalent at a junction temperature (T_J) of 55°C, as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature.

TIMING SPECIFICATIONS

T_A = −40°C to +85°C, VCC = 5.0 V, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Serial clock (not shown in figures)	0.01		2.5	MHz
$t_{DATARATE}$	Data rate period	32			µs
t_{STALL}	Stall period between data	9			µs
$t_{\overline{CS}}$	Chip select to clock edge	48.8			ns
t_{DAV}	Data output valid after SCLK falling edge[2]			100	ns
t_{DSU}	Data input setup time before SCLK rising edge	24.4			ns
t_{DHD}	Data input hold time after SCLK rising edge	48.8			ns
t_{DF}	Data output fall time (not shown in figures)		5	12.5	ns
t_{DR}	Data output rise time (not shown in figures)		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge[3]	5			ns

[1] Guaranteed by design; not production tested.
[2] The MSB presents an exception to this parameter. The MSB clocks out on the falling edge of $\overline{CS}$. The remaining DOUT bits are clocked after the falling edge of SCLK and are governed by this specification.
[3] This parameter may need to be expanded to allow for proper capture of the LSB. After $\overline{CS}$ goes high, the DOUT line enters a high impedance state.

Timing Diagrams

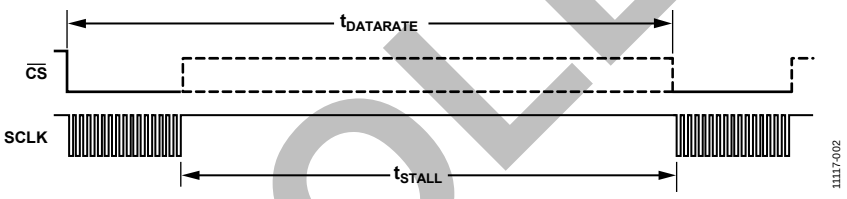

Figure 2. SPI Chip Select Timing

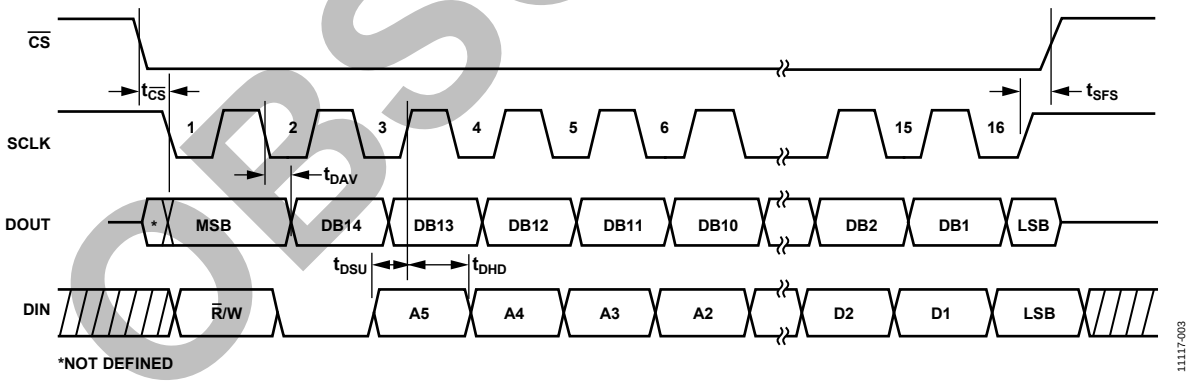

Figure 3. SPI Timing (Using SPI Settings Typically Identified as CPOL = 1, CPHA = 1)

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered, 0.5 ms	2000 *g*
Any Axis, Powered, 0.5 ms	2000 *g*
VCC to GND	−0.3 V to +6.0 V
Digital Input/Output Voltage to GND	−0.3 V to +5.3 V
Analog Inputs to GND	−0.3 V to +3.5 V
Operating Temperature Range[1]	−40°C to +105°C
Storage Temperature Range[1]	−65°C to +150°C

[1] Extended exposure to temperatures outside the temperature range of −40°C to +85°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the part within the temperature range of −40°C to +85°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

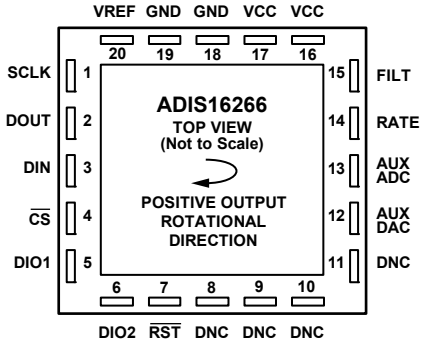

Figure 4. Pin Configuration

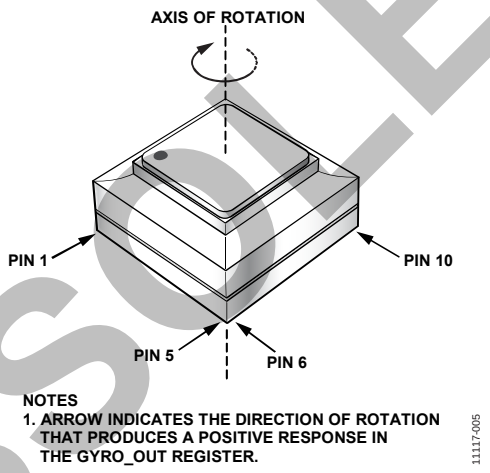

Figure 5. Axial Orientation

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	SCLK	I	SPI Serial Clock.
2	DOUT	O	SPI Data Output. DOUT clocks the output on the falling edge of SCLK.
3	DIN	I	SPI Data Input. DIN clocks the input on the rising edge of SCLK.
4	$\overline{CS}$	I	SPI Chip Select. Active low.
5, 6	DIO1, DIO2	I/O	Configurable Digital Input/Output.
7	$\overline{RST}$	I	Reset. Active low.
8, 9, 10, 11	DNC		Do Not Connect.
12	AUX DAC	O	Auxiliary DAC Output.
13	AUX ADC	I	Auxiliary ADC Input.
14	RATE	O	Rate Output. For bandwidth reduction only, the output is not specified.
15	FILT	I	Filter Terminal.
16, 17	VCC	S	5.0 V Power Supply.
18, 19	GND	S	Ground.
20	VREF	O	Precision Reference Output.

[1] I = input, I/O = input/output, O = output, and S = supply.

TYPICAL PERFORMANCE CHARACTERISTICS

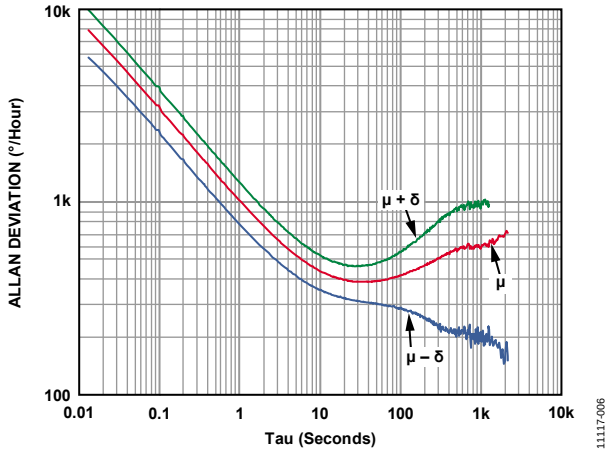

Figure 6. Allan Variance Plot

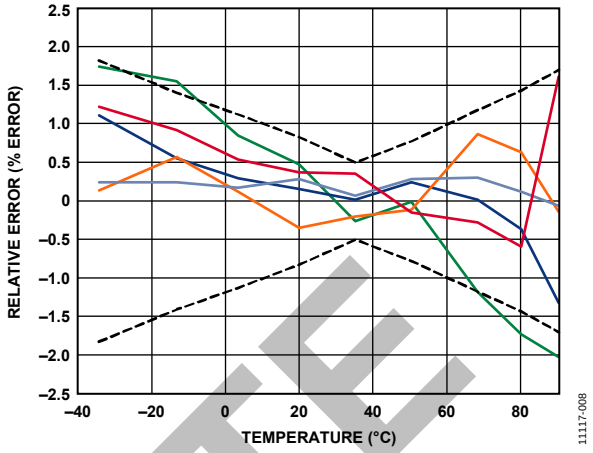

Figure 8. Sensitivity vs. Temperature

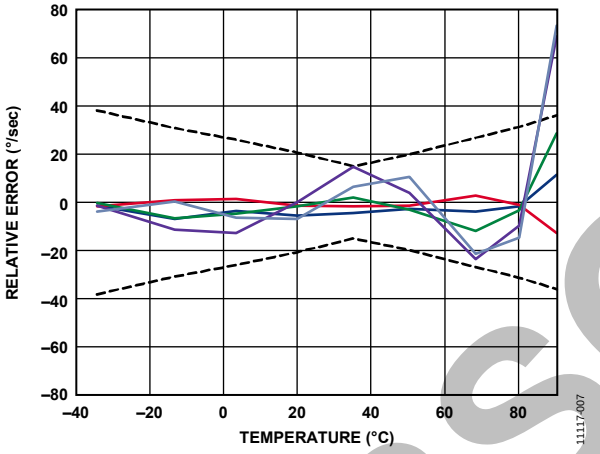

Figure 7. Bias vs. Temperature

THEORY OF OPERATION

The ADIS16266 integrates a MEMS gyroscope with data sampling, signal processing, and calibration functions, along with a simple user interface. This sensing system collects data autonomously and makes it available to any processor system that supports a 4-wire serial peripheral interface (SPI).

SENSING ELEMENT

The sensing element operates on the principle of a resonator gyro. Two polysilicon sensing structures each contain a dither frame that is electrostatically driven to resonance, producing the necessary velocity element to generate a Coriolis force during angular rate. At two of the outer extremes of each frame, orthogonal to the dither motion, movable fingers are placed between fixed pickoff fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed into a series of gain and demodulation stages that produce the electrical rate signal output. The differential structure minimizes the response to linear acceleration (gravity, vibration, and so on) and EMI.

DATA SAMPLING AND PROCESSING

The ADIS16266 runs autonomously, based on the configuration in the user control registers. The analog gyroscope signal feeds into an analog-to-digital converter (ADC) stage, which passes digitized data into the controller for data processing and register loading. Data processing in the embedded controller includes correction formulas, filtering, and checking for preset alarm conditions. The correction formulas are unique for each individual ADIS16266 and come from the factory characterization of each device over a temperature range of −40°C to +70°C.

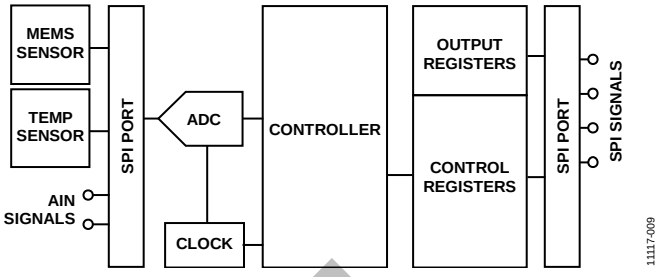

Figure 9. Simplified Sensor Signal Processing Diagram

USER INTERFACE

SPI Interface

Data collection and configuration commands both use the SPI, which consists of four wires. The chip select ($\overline{CS}$) signal activates the SPI interface, and the serial clock (SCLK) signal synchronizes the serial data lines. The serial input data clocks into DIN on the SCLK rising edge, and the serial output data clocks out of DOUT on the SCLK falling edge. Many digital processor platforms support this interface with dedicated serial ports and simple instruction sets.

User Registers

The user registers provide addressing for all input/output operations on the SPI interface. Each 16-bit register has its own unique bit assignment and has two 7-bit addresses: one for its upper byte and one for its lower byte. Table 7 provides a memory map of the user registers, along with the function of each register.

BASIC OPERATION

The ADIS16266 is an autonomous system that requires no user initialization. As soon as it has a valid power supply, it initializes and starts sampling, processing, and loading sensor data into the output registers. After each sample cycle concludes, DIO1 pulses high. The SPI interface enables simple integration with many embedded processor platforms, as shown in Figure 10 (electrical connection) and Table 5 (processor pin names and functions).

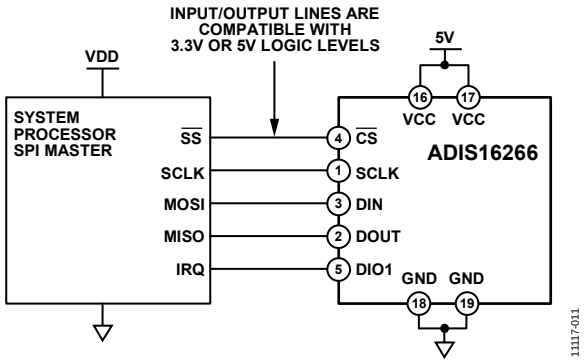

Figure 10. Electrical Connection Diagram

Table 5. Generic Master Processor Pin Names and Functions

Pin Name	Function
$\overline{SS}$	Slave select
IRQ	Interrupt request
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

The SPI interface of the ADIS16266 supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 13. Table 6 provides a list of the most common settings that require attention to initialize a processor serial port for the SPI interface of the ADIS16266.

Table 6. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16266 operates as a slave
SCLK Rate ≤ 2.5 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence
16-Bit Mode	Shift register/data length

READING SENSOR DATA

A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 13. Then, the register contents follow on DOUT during the second sequence. Figure 11 includes three single register reads in succession. In this example, the process starts with Pin 3, DIN = 0x0400, to request the contents of the GYRO_OUT register and follows with 0x0600 to request the contents of the GYRO_OUT2 register and with 0x0C00 to request the contents of the TEMP_OUT register. Full duplex operation enables processors to use the same 16-bit SPI cycle to read data from DOUT while requesting the next set of data on the DIN pin. Figure 12 provides an example of the four SPI signals when reading GYRO_OUT in a repeating pattern.

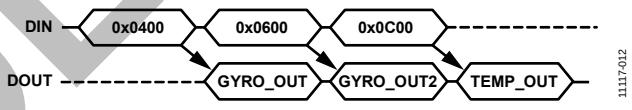

Figure 11. SPI Read Example

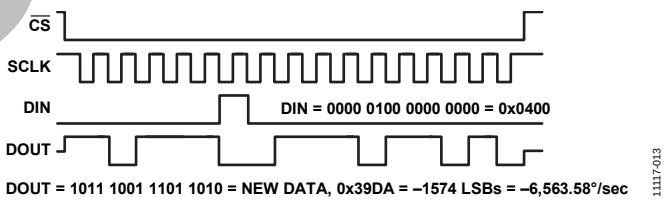

Figure 12. SPI Read Example, Second 16-Bit Sequence

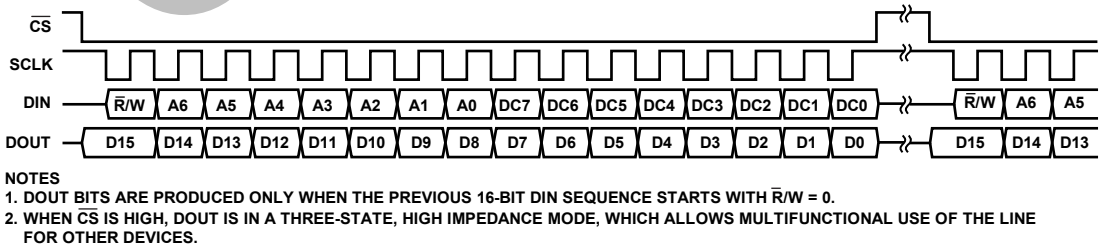

Figure 13. SPI Communication Bit Sequence

USER REGISTERS

Table 7. User Register Memory Map

Name	R/W	Flash Backup	Address[1]	Default	Register Description	Bit Descriptions
FLASH_CNT	R	Yes	0x00	N/A[2]	Flash memory write count	See Table 27
SUPPLY_OUT	R	No	0x02	N/A[2]	Output, power supply	See Table 13
GYRO_OUT	R	No	0x04	N/A[2]	Output, gyroscope	See Table 8
GYRO_OUT2	R	No	0x06	N/A[2]	Output, gyroscope, bit growth from decimation	See Table 10
Reserved	N/A[2]	N/A[2]	0x08	N/A[2]	Reserved	
AUX_ADC	R	No	0x0A	N/A[2]	Output, auxiliary ADC measurement	See Table 15
TEMP_OUT	R	No	0x0C	N/A[2]	Output, temperature (internal)	See Table 11
Reserved	N/A[2]	N/A[2]	0x0F to 0x13	N/A[2]	Reserved	
GYRO_OFF	R/W	Yes	0x14	0x0000	Gyroscope bias correction	See Table 19
GYRO_SCALE	R/W	Yes	0x16	0x0800	Gyroscope scale correction	See Table 20
Reserved	N/A[2]	N/A[2]	0x18 to 0x1F	N/A[2]	Reserved	
ALM_MAG1	R/W	Yes	0x20	0x0000	Alarm 1 trigger setting	See Table 30
ALM_MAG2	R/W	Yes	0x22	0x0000	Alarm 2 trigger setting	See Table 31
ALM_SMPL1	R/W	Yes	0x24	0x0000	Alarm 1 sample period	See Table 32
ALM_SMPL2	R/W	Yes	0x26	0x0000	Alarm 2 sample period	See Table 33
ALM_CTRL	R/W	Yes	0x28	0x0000	Alarm configuration	See Table 34
Reserved	N/A[2]	N/A[2]	0x2B to 0x2F	N/A[2]	Reserved	
AUX_DAC	R/W	No	0x30	0x0000	Control, DAC output voltage setting	See Table 25
GPIO_CTRL	R/W	No	0x32	0x0000	Control, digital input/output line	See Table 23
MSC_CTRL	R/W	Yes	0x34	0x0006	Control, data ready, self-test settings	See Table 24
SMPL_PRD	R/W	Yes	0x36	0x0000	Control, internal sample rate	See Table 17
SENS_AVG	R/W	Yes	0x38	0x0401	Control, dynamic range, filtering	See Table 18
SLP_CNT	W	Yes	0x3A	N/A[2]	Control, sleep mode initiation	See Table 22
DIAG_STAT	R	No	0x3C	N/A[2]	Diagnostic, error flags	See Table 29
GLOB_CMD	W	No	0x3E	N/A[2]	Control, global commands	See Table 21
			0x40 to 0x51	N/A[2]	Reserved	
LOT_ID1	R	Yes	0x52	N/A	Lot Identification Code 1	See Table 37
LOT_ID2	R	Yes	0x54	N/A[2]	Lot Identification Code 2	See Table 37
PROD_ID	R	Yes	0x56	0x3F8A	Product identifier; 16,266	See Table 37
SERIAL_NUM	R	Yes	0x58	N/A[2]	Serial number	See Table 37

[1] Each register contains two bytes. The address column in this table only offers the address of the lower byte. Add 1 to it to calculate the address of the upper byte.
[2] N/A means not applicable.

OUTPUT DATA REGISTERS

Figure 14 displays the generic pattern for the format of the output registers. The ND bit is equal to 1 when the register contains unread data. The EA bit is high when any error/alarm flag in the DIAG_STAT register is equal to 1.

Figure 14. Output Register Bit Assignments

Rotation Rate (Gyroscope)

GYRO_OUT (see Table 8) is the primary register for gyroscope output data and uses 14-bit twos complement format for its data. Table 9 provides several examples for converting digital data into °/sec.

Table 8. GYRO_OUT Bits (Base Address = 0x04)

Bits	Description
15	New (unread) data indicator; bit = 1 indicates new, unread data in this register
14	Error/alarm; bit = 1 when DIAG_STAT ≠ 0x0000
[13:0]	Gyroscope data; twos complement, 4.17°/sec per LSB, 0°/sec = 0x0000

Table 9. GYRO_OUT, Twos Complement Format

Rotation Rate	Decimal	Hex	Binary
+14000°/sec	+3357	0x0D1D	xx00 1101 0001 1101
+8.34°/sec	+2	0x0002	xx00 0000 0000 0010
+4.17°/sec	+1	0x0001	xx00 0000 0000 0001
0°/sec	0	0x0000	xx00 0000 0000 0000
−4.17°/sec	−1	0x3FFF	xx11 1111 1111 1111
−8.34°/sec	−2	0x3FFE	xx11 1111 1111 1110
−14000°/sec	−3357	0x32E3	xx11 0010 1110 0011

The GYRO_OUT2 register (see Table 10) captures the bit growth associated with the decimation filter (see Figure 19) using an MSB justified format. The bit growth starts with the MSB (GYRO_OUT2[15]), is equal to the decimation rate setting in SMPL_PRD[3:0] (see Table 17), and grows in the LSB direction as the decimation rate increases.

Table 10. GYRO_OUT2 Bits (Base Address = 0x06)

Bits	Description
[15:0]	Rotation rate data; resolution enhancement bits

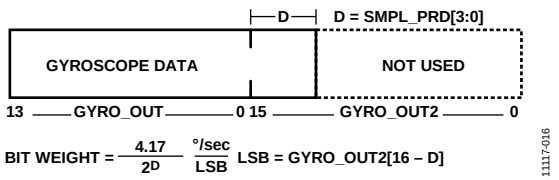

Figure 15. Gyroscope Output Format

Internal Temperature

The TEMP_OUT register (see Table 11) provides access to a sensor that monitors internal temperature, which influences the calibration correction formulas for the gyroscope data. Note that this difference between internal and ambient temperatures is dependent on many factors, which can introduce variation that can approach ±10°C. This temperature measurement is useful for tracking relative changes in temperature.

Table 11. TEMP_OUT Bits (Base Address = 0x0C)

Bits	Description
15	New (unread) data indicator; bit = 1 indicates new, unread data in this register
14	Error/alarm; bit = 1 when DIAG_STAT ≠ 0x0000
[13:12]	Not used
[11:0]	Temperature data; twos complement, 0.1447°C per LSB, 0°C = 0x000

Table 12. Temperature, Twos Complement Format

Temperature	Decimal	Hex	Binary Output
+105°C	+544 LSB	0x220	xxxx 0010 0010 0000
+25.2894°C	+2 LSB	0x002	xxxx 0000 0000 0010
+25.1447°C	+1 LSB	0x001	xxxx 0000 0000 0001
+25°C	0 LSB	0x000	xxxx 0000 0000 0000
+24.8553°C	−1 LSB	0xFFF	xxxx 1111 1111 1111
+24.7106°C	−2 LSB	0xFFE	xxxx 1111 1111 1110
−40°C	−449 LSB	0xE3F	xxxx 1110 0011 1111

Power Supply Voltage

The SUPPLY_OUT (see Table 13) register provides a digital representation of the power supply voltage, across VDD and GND.

Table 13. SUPPLY_OUT Bits (Base Address = 0x02)

Bits	Description
15	New (unread) data indicator; bit = 1 indicates new, unread data in this register
14	Error/alarm; bit = 1 when DIAG_STAT ≠ 0x0000
[13:12]	Not used
[11:0]	Power supply (VDD) data, binary (0 V = 0x000) 1.83 mV/LSB

Table 14. Power Supply Voltage Data Format Examples

Supply Voltage (V)	Decimal	Hex	Binary Output
5.25	2867 LSB	0xB33	xxxx 1011 0011 0011
5.0 + 0.00183	2731 LSB	0xAAB	xxxx 1010 1010 1011
5.0	2730 LSB	0xAAA	xxxx 1010 1010 1010
5.0 – 0.00183	2729 LSB	0xAA9	xxxx 1010 1010 1001
4.75	2594 LSB	0xA22	xxxx 1010 0010 0010

Auxiliary Input Voltage (AUX_ADC)

The AUX_ADC (see Table 15) register provides a digital representation of the voltage on the AUX_ADC pin.

Table 15. AUX_ADC Bits (Base Address = 0x0A)

Bits	Description
15	New (unread) data indicator; bit = 1 indicates new, unread data in this register
14	Error/alarm; bit = 1 when DIAG_STAT ≠ 0x0000
[13:12]	Not used
[11:0]	Auxiliary input voltage, binary (0 V = 0x000) 0.6105 mV/LSB

Table 16. AUX_ADC Voltage Data Format Examples

Input (mV)	Decimal	Hex	Binary Output
2500	4095 LSB	0xFFF	xxxx 1111 1111 1111
1200	1966 LSB	0x7AE	xxxx 0111 1010 1110
0.6105	1 LSB	0x001	xxxx 0000 0000 0001
0	0 LSB	0x000	xxxx 0000 0000 0000

DEVICE CONFIGURATION

The control registers listed in Table 7 provide a variety of user configuration options. The SPI provides access to these registers, one byte at a time, using the bit assignments shown in Figure 13. Each register has 16 bits, wherein Bits[7:0] represent the lower address, and Bits[15:8] represent the upper address. Figure 16 provides an example of writing 0x03 to Address 0x32 (GPIO_CTRL[7:0], see Table 23).

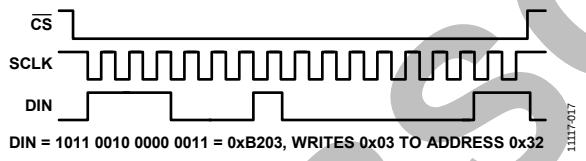

Figure 16. SPI Sequence for Setting the Decimate Rate to 8 (DIN = 0xB203)

Dual Memory Structure

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, set GLOB_CMD[3] = 1 (DIN = 0xBE08) to back up these settings in the nonvolatile flash memory. The flash backup process requires a valid power supply level for the entire 40 ms process time. Table 7 provides a register memory map that includes a column of flash backup information. A yes in this column indicates that a register has a mirror location in flash and, when backed up properly, automatically restores itself during startup or after a reset. Figure 17 provides a diagram of the dual memory structure that is used to manage operation and store critical user settings.

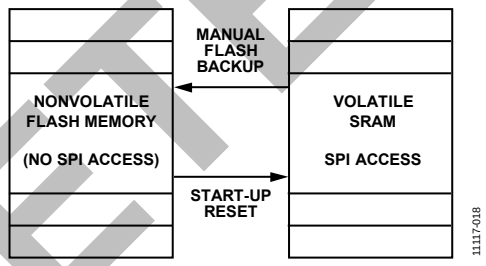

Figure 17. SRAM and Flash Memory Diagram

DIGITAL SIGNAL PROCESSING

Figure 19 provides a signal processing diagram that describes all of the user-configurable options, which influence sample rate and the frequency response. Using the factory default settings for the SMPL_PRD and SENS_AVG registers, the effective sensor bandwidth is 360 Hz.

DECIMATION FILTER (UPDATE RATE)

The internal sampling system produces new data in the output data registers at a rate of 2429 SPS. The SMPL_PRD register (see Table 17) provides the functional control for the decimation filter stage, which provides a user control input for reducing the update rate in the output registers. The decimation filter reduces the update rate, using an averaging filter with a decimated output. These bits provide a binomial control that divides the data rate by a factor of 2 every time this number increases by 1. For example, set SMPL_PRD[3:0] = 00100 (DIN = 0xB604) to set the decimation factor to 16. This reduces the update rate to 151.8 SPS and the bandwidth (−3 dB) to approximately 75 Hz.

Table 17. SMPL_PRD Bits (Base Address = 0x36)

Bits	Description (Default = 0x0000)
[15:4]	Not used
[3:0]	Decimation setting (D), see Figure 19

FREQUENCY RESPONSE

Analog Filter

Prior to the analog-to-digital conversion stage, the ADIS16266 has a two-pole analog filter, with both poles located at approximately 1.6 kHz. The RATE and FILT pins provide access to the amplifier feedback path on one of these filters. This provides an opportunity to reduce the cut-off frequency associated with this filter pole, according to the following relationship.

$$f_C = \frac{1}{2\pi \times 180000 \times (C + 560\ \text{pF})}$$

For example, adding a 1000 pF capacitor reduces this pole to approximately 567 Hz.

Digital Filtering

A programmable low-pass filter provides additional noise reduction on the inertial sensor outputs. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 19). For example, set SENS_AVG[2:0] = 100 (DIN = 0xB804) to set each stage to 16 taps. When used with the default sample rate of 2429 SPS (no decimation), this reduces the bandwidth of the digital filter to approximately 49 Hz. The minimum setting for this filter is two taps per stage (SENS_AVG[2:0] ≥ 001).

Table 18. SENS_AVG Bits (Base Address = 0x38)

Bits	Description (Default = 0x0401)
[15:11]	Not used.
[10:8]	Measurement range (sensitivity) selection. 100 = ±14,000°/sec, filter taps ≥ 2 (Bits[2:0] ≥ 0x01). 010 = ±7000°/sec, filter taps ≥ 4 (Bits[2:0] ≥ 0x02). 001 = ±3500°/sec, filter taps ≥ 16 (Bits[2:0] ≥ 0x04).
[7:3]	Not used.
[2:0]	Number of taps in each stage; value of m in $N = 2^m$.

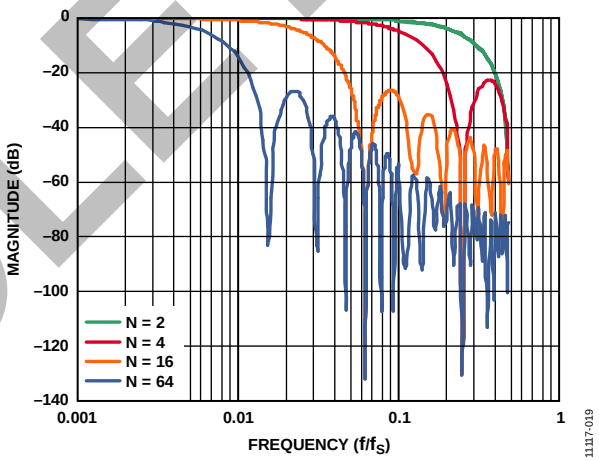

Figure 18. Digital Filter Frequency, Bartlett Window FIR Filter (Phase = N Samples)

DYNAMIC RANGE

The SENS_AVG[10:8] bits provide three dynamic range settings for this gyroscope. The lower dynamic range settings (±3500°/sec and ±7000°/sec) limit the minimum filter tap sizes to maintain resolution. For example, set SENS_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of ±7000°/sec. Because this setting can influence the filter settings, program SENS_AVG[10:8] and then SENS_AVG[2:0] if more filtering is required.

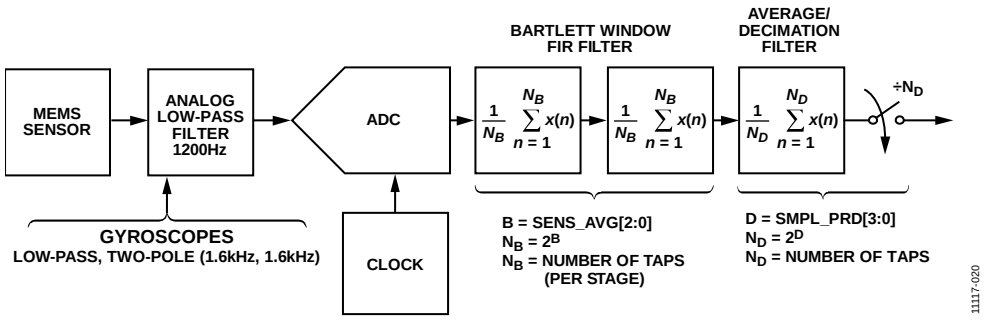

Figure 19. Signal Processing Diagram

CALIBRATION

The GYRO_OFF and GYRO_SCALE registers provide user controls for making in-system adjustments to offset and the scale factor.

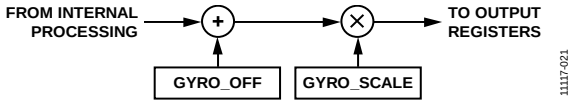

Figure 20. User Calibration Registers

Table 19. GYRO_OFF Bits (Base Address = 0x14)

Bits	Description (Default = 0x0000)
[15:12]	Not used.
[11:0]	Offset adjustment factor, twos complement format, 1.04°/sec per LSB. Examples: 0x000: add 0°/sec to gyroscope data. 0x001: add 1.04°/sec to gyroscope data. 0x0AA: add 176.8°/sec to gyroscope data. 0xF0F: subtract 250.64°/sec from gyroscope data. 0xFFF: subtract 1.04°/sec from gyroscope data.

Table 20. GYRO_SCALE Bits (Base Address = 0x16)

Bits	Description (Default = 0x0800)
[15:12]	Not used.
[11:0]	Scale adjustment factor, offset binary format, 0.00048828/LSB. Examples: 0x000: multiply output by 0. 0x7F0: multiply gyroscope data by 0.99218. 0x800: multiply output by 1. 0x8A0: multiply output by 1.078122. 0xFFF: multiply output by 1.9995.

SYSTEM TOOLS

Global Commands

The GLOB_CMD register provides trigger bits for several functions. Setting the assigned bit to 1 starts each operation, which returns the bit to 0 after completion. For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to execute a software reset, which stops the sensor operation and runs the device through its start-up sequence. This sequence includes loading the control registers with the contents of their respective flash memory locations prior to producing new data.

Table 21. GLOB_CMD Bits (Base Address = 0x3E)

Bits	Description
[15:8]	Not used.
7	Software reset command.
6:4	Not used.
3	Flash update command.
2	Auxiliary DAC data latch.
1	Factory calibration restore command.
0	Autonull command.

Power Management

Use SLP_CNT[7:0] to put the device into sleep mode for a specified period. For example, SLP_CNT[7:0] = 0x64 (DIN = 0xBA64) puts the ADIS16266 to sleep for 50 seconds.

Table 22. SLP_CNT Bits (Base Address = 0x3A)

Bits	Description
[15:8]	Not used.
[7:0]	Programmable sleep time bits, 0.5 sec/LSB.

General-Purpose Input/Output

DIO1 and DIO2 are configurable, general-purpose input/output lines that serve multiple purposes according to the following control register priority: MSC_CTRL, ALM_CTRL, and GPIO_CTRL. For example, set GPIO_CTRL = 0x0202 (DIN = 0xB302, and then 0xB202) to configure DIO1 as an input and DIO2 as an output that is set high.

Table 23. GPIO_CTRL Bits (Base Address = 0x32)

Bits	Description (Default = 0x0000)
[15:10]	Not used.
9	General-Purpose input/output Line 2 (DIO2) data level.
8	General-Purpose input/output Line 1 (DIO1) data level.
[7:2]	Not used.
1	General-Purpose input/output Line 2 (DIO2) direction control. 1 = output, 0 = input.
0	General-Purpose input/output Line 1 (DIO1) direction control. 1 = output, 0 = input.

Data Ready Input/Output Indicator

The MSC_CTRL[2:0] bits configure one of the digital input/output lines as a data ready signal for driving an interrupt. For example, set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to configure DIO1 as a negative-pulse data ready signal. The pulse width is between 100 µs and 200 µs over all conditions.

Table 24. MSC_CTRL Bits (Base Address = 0x34)

Bits	Description (Default = 0x0006)
[15:12]	Not used.
11	Memory test (cleared upon completion). 1 = enabled, 0 = disabled.
10	Internal self-test enable (cleared upon completion). 1 = enabled, 0 = disabled.
9	Manual self-test, negative stimulus. 1 = enabled, 0 = disabled.
8	Manual self-test, positive stimulus. 1 = enabled, 0 = disabled.
7:3	Not used.
2	Data ready enable. 1 = enabled, 0 = disabled.
1	Data ready polarity. 1 = active high, 0 = active low.
0	Data ready line select. 1 = DIO2, 0 = DIO1.

Auxiliary DAC

The 12-bit AUX_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (approximately 100 LSB starting point). As the sink current increases, the nonlinear range increases. The DAC latch command (GLOB_CMD[2]) moves the values of the AUX_DAC register into the internal DAC control register, enabling both bytes to take effect at the same time.

Table 25. AUX_DAC Bits (Base Address = 0x30)

Bits	Description (Default = 0x0000)
[15:12]	Not used.
[11:0]	Data bits, scale factor = 0.6105 mV/code. Offset binary format, 0 V = 0 codes.

Table 26. Setting AUX_DAC = 2 V

DIN	Description
0xB0CC	AUX_DAC[7:0] = 0xCC (204 LSB).
0xB10C	AUX_DAC[15:8] = 0x0C (3072 LSB).
0xBE04	GLOB_CMD[2] = 1. Latch AUX_DAC values into the internal DAC control register which causes the output voltage to settle at a value of 2 V.

Memory Management

The FLASH_CNT register (see Table 27) tracks the number of write cycles for the flash memory to help manage the total cycles against the endurance ratings in Table 1.

Table 27. FLASH_CNT Bits (Base Address = 0x00)

Bits	Description
[15:0]	Flash update counter

DIAGNOSTICS

Self-Test

The self-test function allows the user to verify the mechanical integrity of each MEMS sensor. It applies an electrostatic force to each sensor element, which results in mechanical displacement that simulates a response to actual motion. Table 1 lists the expected response for the sensor, which provides pass/fail criteria.

Set MSC_CTRL[10] = 1 (DIN = 0xB504) to run the internal self-test routine, which exercises the inertial sensor, measures the response, makes a pass/fail decision, reports the decision to the error flags in the DIAG_STAT register, and then restores normal operation. MSC_CTRL[10] resets itself to 0 after completing the routine. The MSC_CTRL[9:8] bits provide manual control of the self-test function for investigation of potential failures. Table 28 outlines an example test flow for using this option to verify the gyroscope function.

Table 28. Manual Self-Test Example Sequence

DIN	Description
0xB601	SMPL_PRD[7:0] = 0x01, sample rate = 2429 SPS.
0xB904	SENS_AVG[15:8] = 0x04, range = ±14000°/sec.
0xB802	SENS_AVG[7:0] = 0x02, four-tap averaging filter.
	Delay = 50 ms.
0x0400	Read GYRO_OUT.
0xB502	MSC_CTRL[9:8] = 10, gyroscope negative self-test.
	Delay = 50 ms.
0x0400	Read GYRO_OUT.
	Determines whether the bias in the gyroscope output changed according to the self-test response specified in Table 1.
0xB501	MSC_CTRL[9:8] = 01, gyroscope positive self-test.
	Delay = 50 ms.
0x0400	Read GYRO_OUT.
	Determines whether the bias in the gyroscope output changed according to the self-test response specified in Table 1.
0xB500	MSC_CTRL[15:8] = 0x00.

Zero motion provides results that are more reliable. The settings in Table 28 are flexible and allow for optimization around speed and noise influence. For example, using fewer filtering taps decreases delay times but increases the potential for noise influence.

Memory Test

Setting MSC_CTRL[11] = 1 (DIN = 0xB508) performs a checksum comparison between the flash memory and SRAM to help verify memory integrity. The pass/fail result is loaded into the DIAG_STAT[6] register.

Status

The error flags provide indicator functions for common system level issues. All of the flags are cleared (set to 0) after each DIAG_STAT register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle. DIAG_STAT[1:0] does not require a read of this register to return to 0. When the power supply voltage goes back into range, these two flags clear automatically.

Table 29. DIAG_STAT Bits (Base Address = 0x3C)

Bits	Description
[15:10]	Not used.
9	Alarm 2 status (1 = active, 0 = inactive).
8	Alarm 1 status (1 = active, 0 = inactive).
7	Not used.
6	Flash test, checksum flag (1 = fail, 0 = pass).
5	Self-test diagnostic error flag (1 = fail, 0 = pass).
4	Sensor overrange (1 = fail, 0 = pass).
3	SPI communication failure (1 = fail, 0 = pass).
2	Flash update failure (1 = fail, 0 = pass).
1	Power supply > 5.25 V. 1 = power supply > 5.25 V, 0 = power supply ≤ 5.25 V.
0	Power supply < 4.75 V. 1 = power supply < 4.75 V, 0 = power supply ≥ 4.75 V.

ALARMS

Alarm Registers

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for data source selection, data filtering (prior to comparison), static comparison, dynamic rate-of-change comparison, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations. Table 35 gives an example of how to configure a static alarm. The ALM_SMPLx registers provide the numbers of samples to use in the dynamic rate-of-change configuration. The period equals the number in the ALM_SMPLx register multiplied by the sample period time. See Table 36 for an example of how to configure the sensor for this type of function.

Table 30. ALM_MAG1 Bits (Base Address = 0x20)

Bits	Description (Default = 0x0000)
15	Comparison polarity (1 = greater than, 0 = less than).
14	Not used.
[13:0]	Data bits that match the format of the trigger source selection.

Table 31. ALM_MAG2 Bits (Base Address = 0x22)

Bits	Description (Default = 0x0000)
15	Comparison polarity (1 = greater than, 0 = less than).
14	Not used.
[13:0]	Data bits that match the format of the trigger source selection.

Table 32. ALM_SMPL1 Bits (Base Address = 0x24)

Bits	Description (Default = 0x0000)
[15:8]	Not used.
[7:0]	Data bits: number of samples (both 0x00 and 0x01 = 1).

Table 33. ALM_SMPL2 Bits (Base Address = 0x26)

Bits	Description (Default = 0x0000)
[15:8]	Not used.
[7:0]	Data bits: number of samples (both 0x00 and 0x01 = 1).

Table 34. ALM_CTRL Bits (Base Address = 0x28)

Bits	Description (Default = 0x0000)
15	Dynamic rate-of-change enable for Alarm 2 (1 = rate of change, 0 = static level).
[14:12]	Alarm 2 source selection. 000 = disable. 001 = power supply output. 010 = gyroscope output. 011 = not used. 100 = not used. 101 = auxiliary ADC input. 110 = temperature output. 111 = not used.
11	Rate-of-change enable for Alarm 1 (1 = dynamic rate of change, 0 = static level).
[10:8]	Alarm 1 source selection (same as for Alarm 2).
[7:5]	Not used.
4	Comparison data filter setting (1 = filtered data, 0 = unfiltered data).
3	Not used.
2	Alarm output enable (1 = enabled, 0 = disabled).
1	Alarm output polarity (1 = active high, 0 = active low).
0	Alarm output line select (1 = DIO2, 0 = DIO1).

Table 35. Alarm Configuration Example 1

DIN	Description
0xA922, 0xA817	ALM_CTRL = 0x2217. Alarm 1 input = GYRO_OUT. Alarm 2 input = GYRO_OUT. Static level comparison, filtered data. DIO2 output indicator, positive polarity.
0xA183, 0xA0E8	ALM_MAG1 = 0x83E8. Alarm 1 is true if GYRO_OUT > +4170°/sec.
0xA338, 0xA230	ALM_MAG2 = 0x3830. Alarm 2 is true if GYRO_OUT < −8340°/sec.

Table 36. Alarm Configuration Example 2

DIN	Description
0xA9AA, 0xA804	ALM_CTRL = 0xAA04. Alarm 1 input = GYRO_OUT. Alarm 2 input = GYRO_OUT. Dynamic rate-of-change comparison, unfiltered data. DIO1 output indicator, negative polarity.
0xB600	SMPL_PRD = 0x0000. Sample rate = 2429 SPS.
0xA4FF	ALM_SMPL1[7:0] = 0x00FF. Alarm 1 dynamic rate-of-change period = 105 ms.
0xA6FF	ALM_SMPL2[7:0] = 0x00FF. Alarm 2 dynamic rate-of-change period = 105 ms.
0xA181, 0xA000	ALM_MAG1 = 0x8100. Alarm 1 is true if GYRO_OUT changes more than 1067.5°/sec over a period of 105 ms.
0xA300, 0xA20A	ALM_MAG2 = 0x000A. Alarm 2 is true if GYRO_OUT changes less than 41.7°/sec over a period of 105 ms.

PRODUCT IDENTIFICATION

Table 37 provides a summary of the registers that identify the product: PROD_ID, which identifies the product type; LOT_ID1 and LOT_ID2, the 32-bit lot identification code; and SERIAL_NUM, which displays the 16-bit serial number. All four registers are two bytes in length.

Table 37. Identification Registers

Register Name	Address	Description
LOT_ID1	0x52	Lot Identification Code 1
LOT_ID2	0x54	Lot Identification Code 2
PROD_ID	0x56	Product identification = 0x3F8A (0x3F8A = 16,266 decimal)
SERIAL_NUM	0x58	Serial number

APPLICATIONS INFORMATION

ASSEMBLY

When developing a process flow for installing ADIS16266 devices on printed circuit boards (PCBs), see the IPC/JEDEC J-STD-020C standard document for reflow temperature profile and processing information. The ADIS16266 can use the Sn-Pb eutectic process or the Pb-free eutectic process from this standard. See IPC/JEDEC J-STD-033 for moisture sensitivity level (MSL) handling requirements. The MSL rating for these devices is marked on the antistatic bags, which protect these devices from electrostatic discharge (ESD) during shipping and handling.

Prior to assembly, review the process flow for information about introducing shock levels that exceed the absolute maximum ratings for the ADIS16266. PCB separation and ultrasonic cleaning processes can introduce high levels of shock and damage the MEMS element. Bowing or flexing the PCB after solder reflow can also place large peeling stress on the pad structure and can damage the device. If this is unavoidable, consider using an underfill material to help distribute these forces across the bottom of the package. Figure 21 provides a PCB pad design example for this package style.

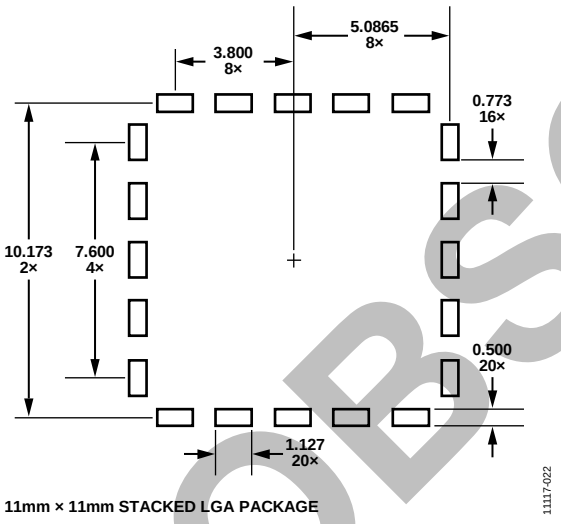

Figure 21. Recommended Pad Layout (Units in Millimeters)

BIAS OPTIMIZATION

Use the following steps to fine tune the bias to an accuracy that approaches the in-run bias stability, 0.129°/sec (1 σ):

1. Apply 5 V and allow enough time to start up.
2. Set SENS_AVG[10:8] = 001 (DIN = 0xB901).
3. Collect GYRO_OUT data for 30 seconds at a sample rate of 2429 SPS.
4. Average data record.
5. Round to the nearest integer.
6. Multiply by −1.
7. Write the resulting number (from Step 6) to GYRO_OFF.
8. Set GLOB_CMD[3] = 1 (DIN = 0xBE08).
9. Wait for >50 ms and resume operation.

Alternatively, setting GLOB_CMD[0] = 1 (DIN = 0xBE01) provides a single sample, bias correction. The Allan variance curve (see Figure 6) provides a trade-off relationship between accuracy and averaging time. For example, an average time of 1 second produces an accuracy of approximately 0.358°/sec (1 σ).

INTERFACE PCB

The ADIS16266/PCBZ includes one ADIS16266BCCZ IC on a 1.2 inch × 1.3 inch PCB. The interface PCB simplifies the IC connection of these devices to an existing processor system. The four mounting holes accommodate either M2 (2 mm) or 2-56 machine screws. These boards are made of IS410 material and are 0.063 inches thick. The second level assembly uses a SAC305-compatible solder composition, which has a presolder reflow thickness of approximately 0.005 inches.

The pad pattern on these PCBs matches that shown in Figure 23. J1 and J2 are dual-row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including the TCSD-08-D-xx.00-01 series from Samtec. The schematic and connector pin assignments for the ADIS16266/PCBZ are shown in Figure 22.

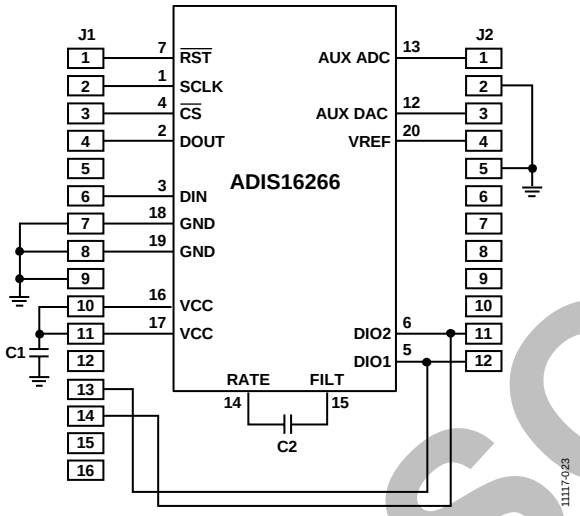

Figure 22. Electrical Schematic

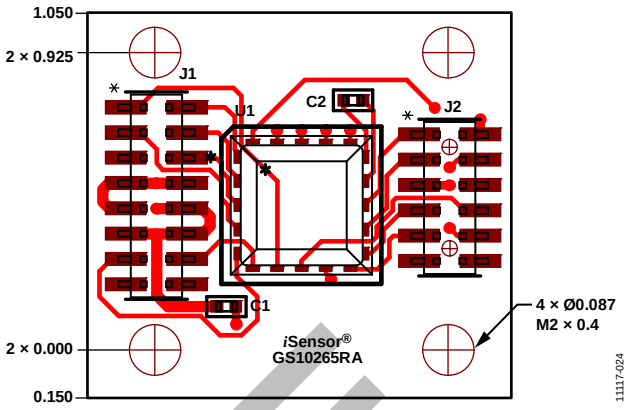

Figure 23. PCB Assembly View and Dimensions

OUTLINE DIMENSIONS

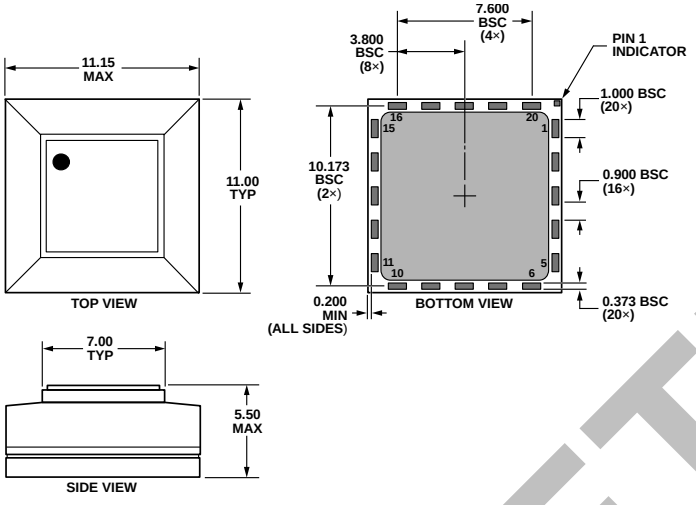

Figure 24. 20-Terminal Stacked Land Grid Array [LGA]
(CC-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16266BCCZ	−40°C to +105°C	20-Terminal Stacked Land Grid Array [LGA]	CC-20-1
ADIS16266/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D11117-0-7/15(B)