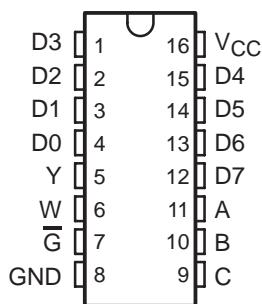


# SN54HC151, SN74HC151 8-LINE TO 1-LINE DATA SELECTORS/MUXES

SCLS110E – DECEMBER 1982 – REVISED SEPTEMBER 2003

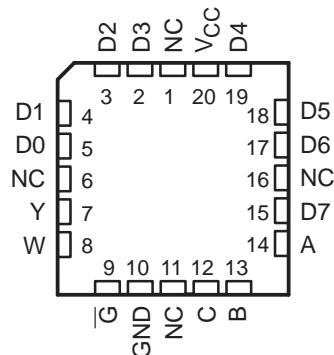
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 13$  ns
- $\pm 6$ -mA Output Drive at 5 V

SN54HC151 . . . J OR W PACKAGE  
SN74HC151 . . . D, N, NS, OR PW PACKAGE  
(TOP VIEW)



- Low Input Current of 1  $\mu$ A Max
- 8-Line to 1-Line Multiplexers Can Perform as:
  - Boolean-Function Generators
  - Parallel-to-Serial Converters
  - Data Source Selectors

SN54HC151 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe ( $\bar{G}$ ) input must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

## ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC151N	SN74HC151N
	SOIC – D	Tube of 40	SN74HC151D	HC151
		Reel of 2500	SN74HC151DR	
		Reel of 250	SN74HC151DT	
	SOP – NS	Reel of 2000	SN74HC151NSR	HC151
	TSSOP – PW	Tube of 90	SN74HC151PW	HC151
		Reel of 2000	SN74HC151PWR	
		Reel of 250	SN74HC151PWT	
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC151J	SNJ54HC151J
	CFP – W	Tube of 150	SNJ54HC151W	SNJ54HC151W
	LCCC – FK	Tube of 55	SNJ54HC151FK	SNJ54HC151FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54HC151, SN74HC151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS110E – DECEMBER 1982 – REVISED SEPTEMBER 2003

FUNCTION TABLE

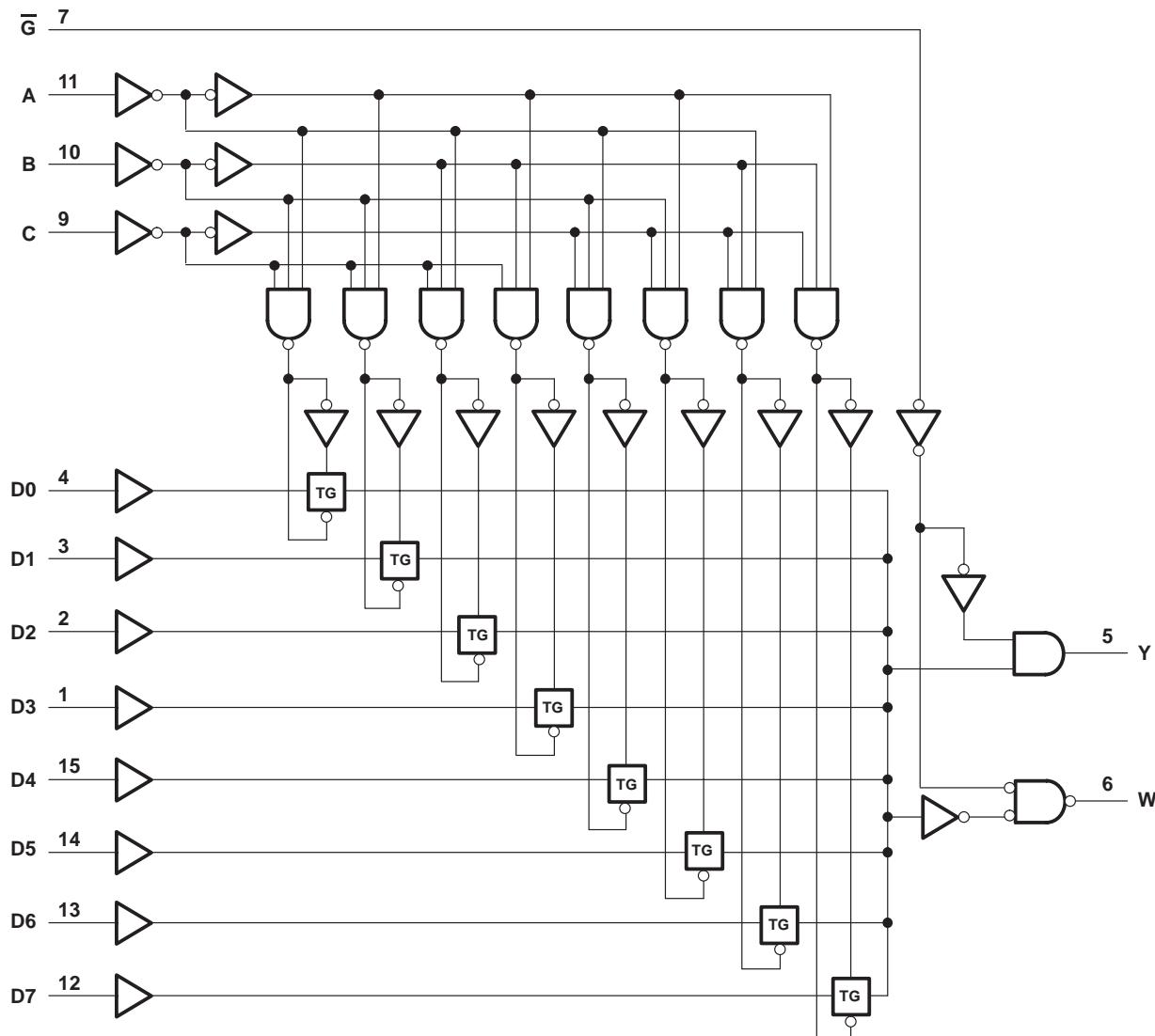
INPUTS			STROBE $\bar{G}$	OUTPUTS	
SELECT		A		Y	W
C	B				
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

D0, D1 . . . D7 = the level of the respective D input



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logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

# **SN54HC151, SN74HC151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HC151			SN74HC151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5			V
		V <sub>CC</sub> = 4.5 V	3.15		3.15			
		V <sub>CC</sub> = 6 V	4.2		4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5		V
		V <sub>CC</sub> = 4.5 V		1.35		1.35		
		V <sub>CC</sub> = 6 V		1.8		1.8		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>		0	V <sub>CC</sub>		V
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 2 V		1000		1000		ns
		V <sub>CC</sub> = 4.5 V		500		500		
		V <sub>CC</sub> = 6 V		400		400		
T <sub>A</sub>	Operating free-air temperature	-55	125		-40	85		°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54HC151, SN74HC151**  
**8-LINE TO 1-LINE DATA SELECTORS/MUX**

SCLS110E – DECEMBER 1982 – REVISED SEPTEMBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC151	SN74HC151	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	2 V	1.9	1.998	1.9	1.9	V
			4.5 V	4.4	4.499	4.4	4.4	
			6 V	5.9	5.999	5.9	5.9	
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3	3.7	3.84	V
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8	5.2	5.34	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V	0.002	0.1	0.1	0.1	V
			4.5 V	0.001	0.1	0.1	0.1	
			6 V	0.001	0.1	0.1	0.1	
		I <sub>OL</sub> = 6 mA	4.5 V	0.17	0.26	0.4	0.33	V
		I <sub>OL</sub> = 7.8 mA	6 V	0.15	0.26	0.4	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1	±100		±1000	±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8	160	80	µA
C <sub>i</sub>		2 V to 6 V	3	10		10	10	pF

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC151	SN74HC151	UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y or W	2 V	94	250		360	312	ns
			4.5 V	30	50		73	63	
			6 V	25	43		62	54	
	Any D	Y or W	2 V	74	195		283	244	
			4.5 V	23	39		57	49	
			6 V	20	33		48	41	
	G̅	Y or W	2 V	49	127		185	159	
			4.5 V	15	25		37	32	
			6 V	13	22		32	28	
t <sub>t</sub>		Y or W	2 V	22	75		110	95	ns
			4.5 V	9	15		22	19	
			6 V	8	13		19	16	

# **SN54HC151, SN74HC151 8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS**

SCLS110E – DECEMBER 1982 – REVISED SEPTEMBER 2003

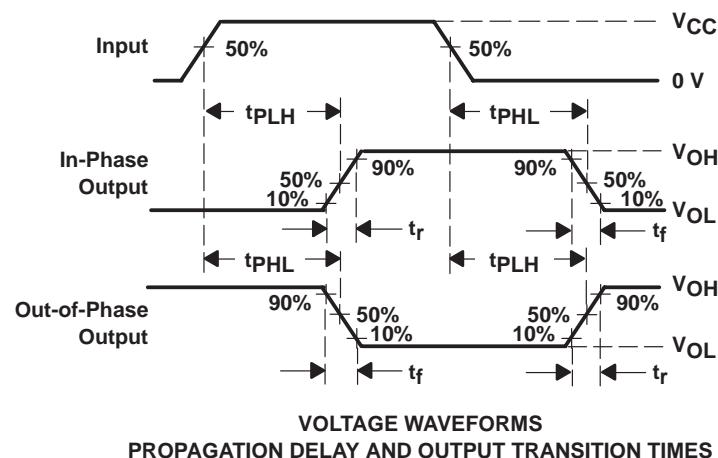
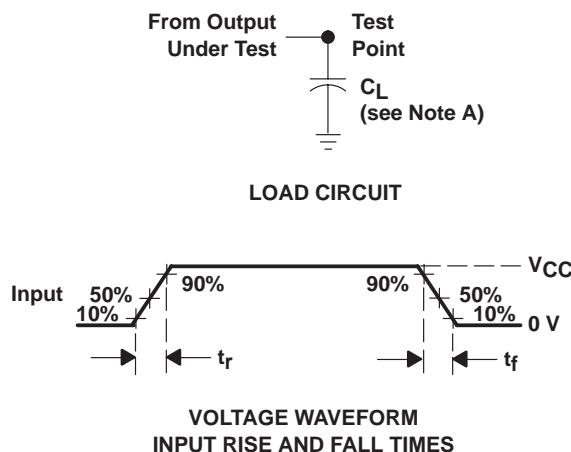
switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC151		SN74HC151		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, or C	Y or W	2 V	107	350	525	425	440	ns		
			4.5 V	33	70	105	88	88			
			6 V	30	59	89	76	76			
	Any D	Y or W	2 V	90	275	415	345	345			
			4.5 V	29	51	83	69	69			
			6 V	25	47	72	59	59			
	G	Y or W	2 V	67	205	310	255	255			
			4.5 V	21	41	62	51	51			
			6 V	18	35	53	43	43			
t <sub>t</sub>		Y or W	2 V	51	210	315	265	265	ns		
			4.5 V	16	42	63	53	53			
			6 V	14	36	53	45	45			

### operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	70	pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and test-fixture capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .

C. The outputs are measured one at a time with one input transition per measurement.

D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84128012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84128012A SNJ54HC 151FK	Samples
8412801EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8412801EA SNJ54HC151J	Samples
SN54HC151J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC151J	Samples
SN74HC151D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC151N	Samples
SN74HC151NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SN74HC151PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC151	Samples
SNJ54HC151FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84128012A SNJ54HC 151FK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54HC151J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8412801EA SNJ54HC151J	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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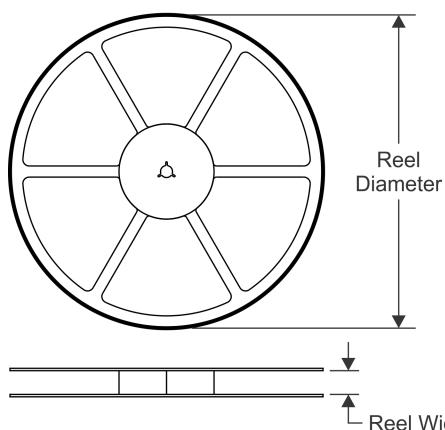
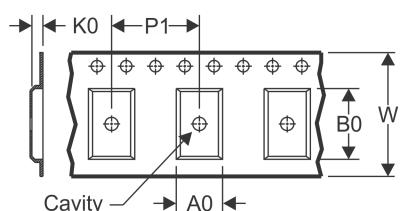
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC151, SN74HC151 :**

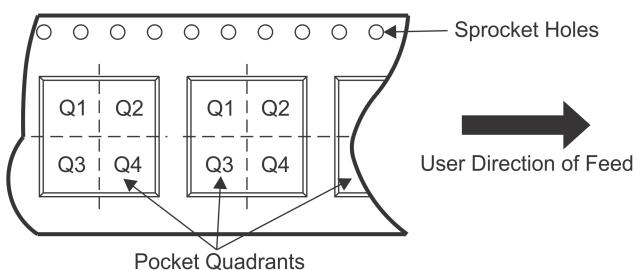
- Catalog: [SN74HC151](#)
- Automotive: [SN74HC151-Q1](#), [SN74HC151-Q1](#)
- Military: [SN54HC151](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC151DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC151PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC151PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC151DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HC151PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74HC151PWT	TSSOP	PW	16	250	367.0	367.0	35.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



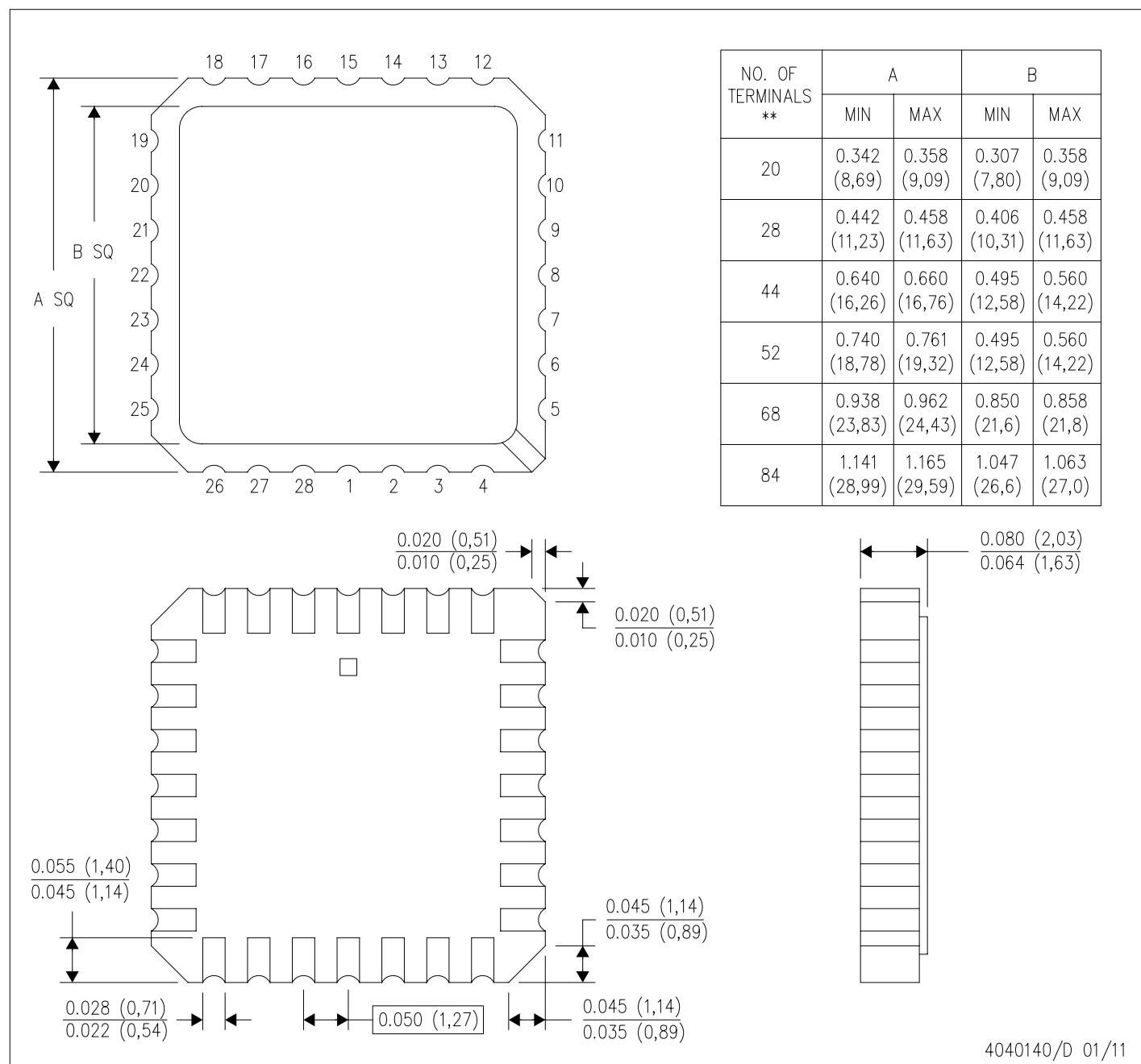
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

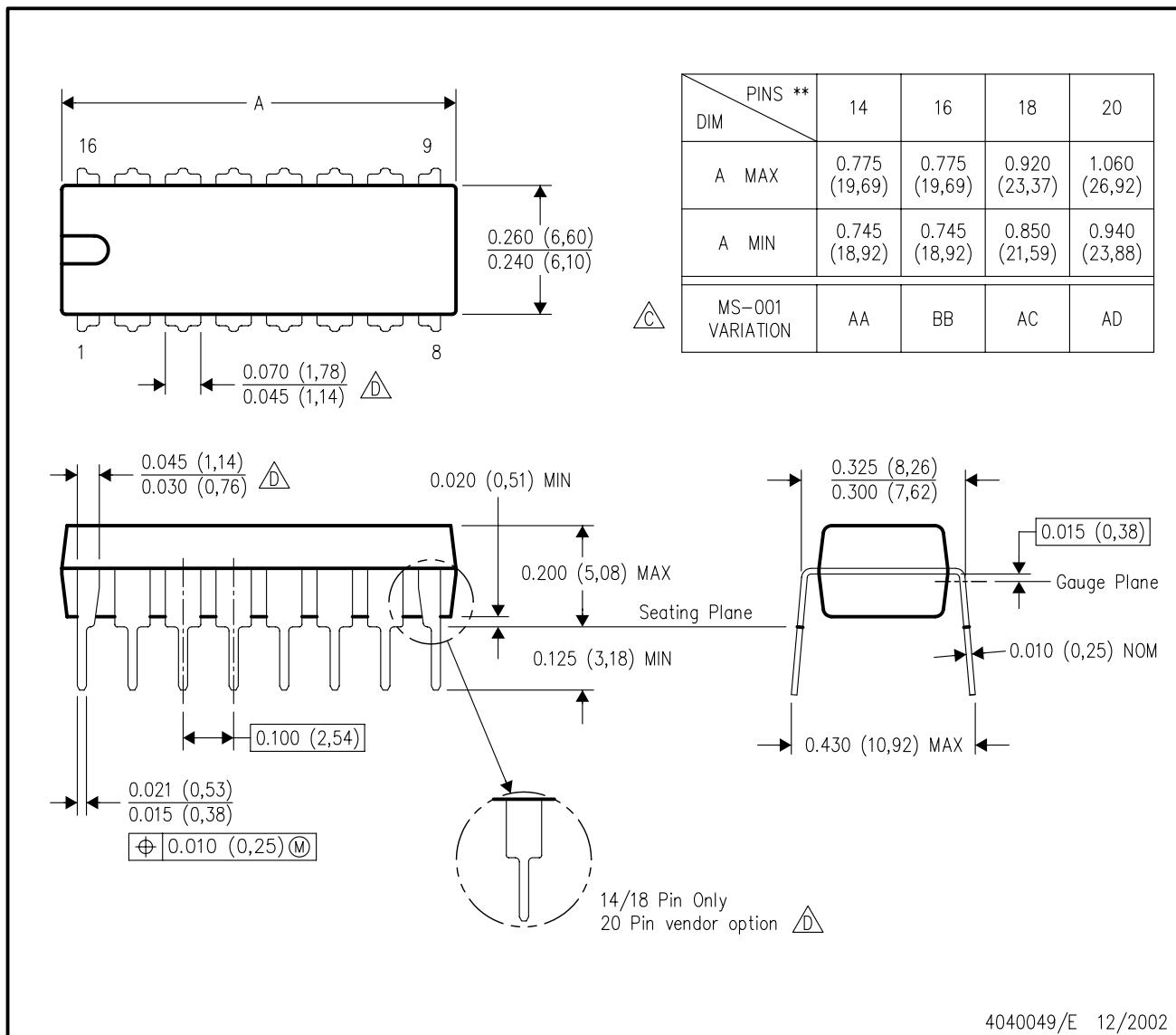
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



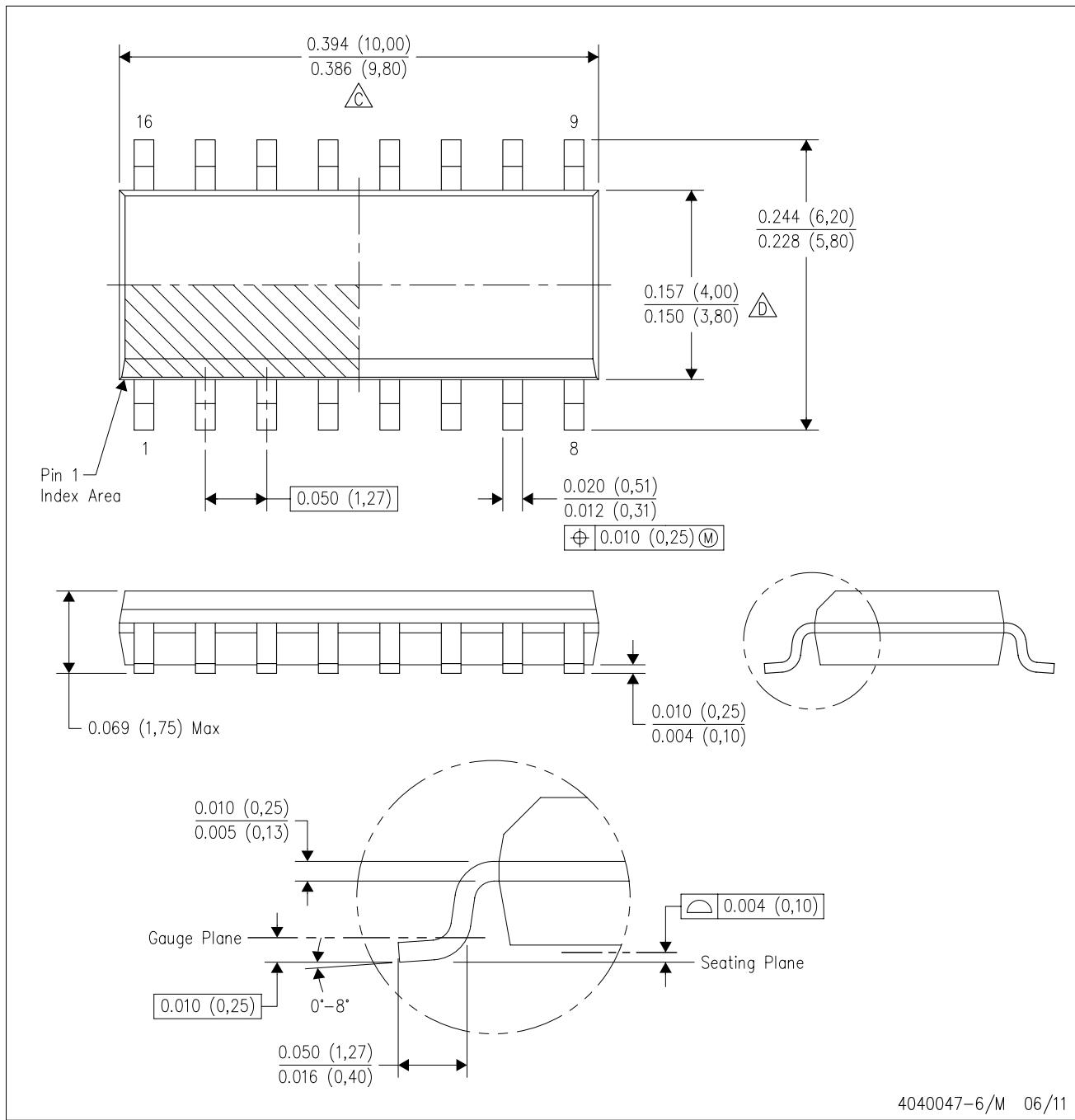
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

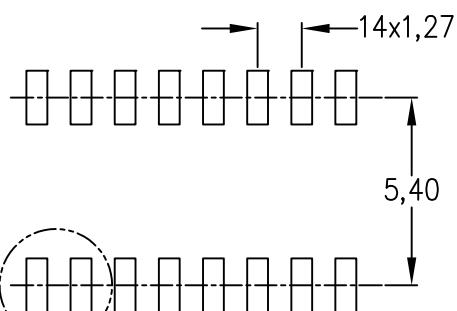
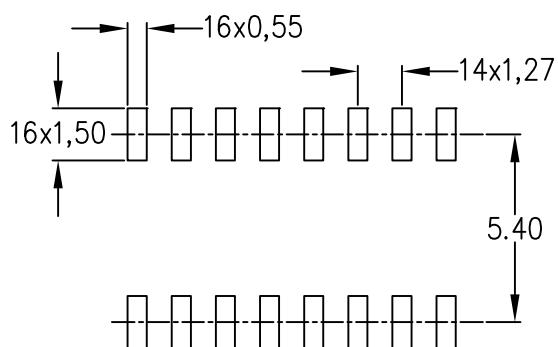
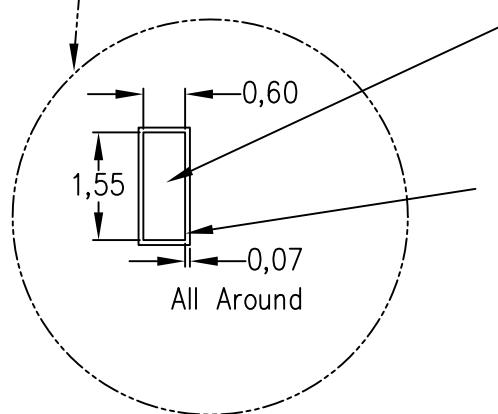
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)Example  
Non Soldermask Defined PadExample  
Pad Geometry  
(See Note C)Example  
Solder Mask Opening  
(See Note E)

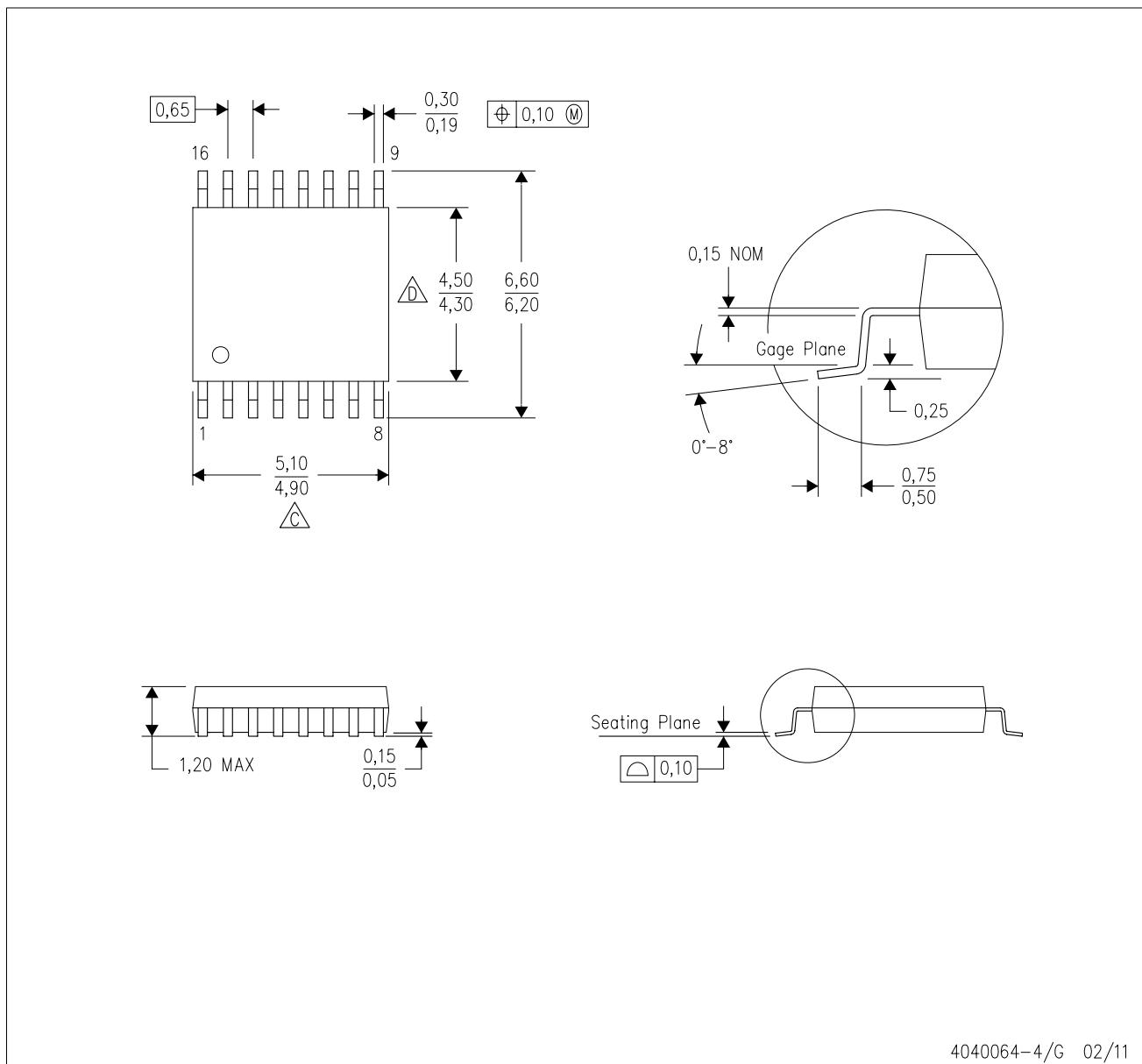
4211283-4/E 08/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

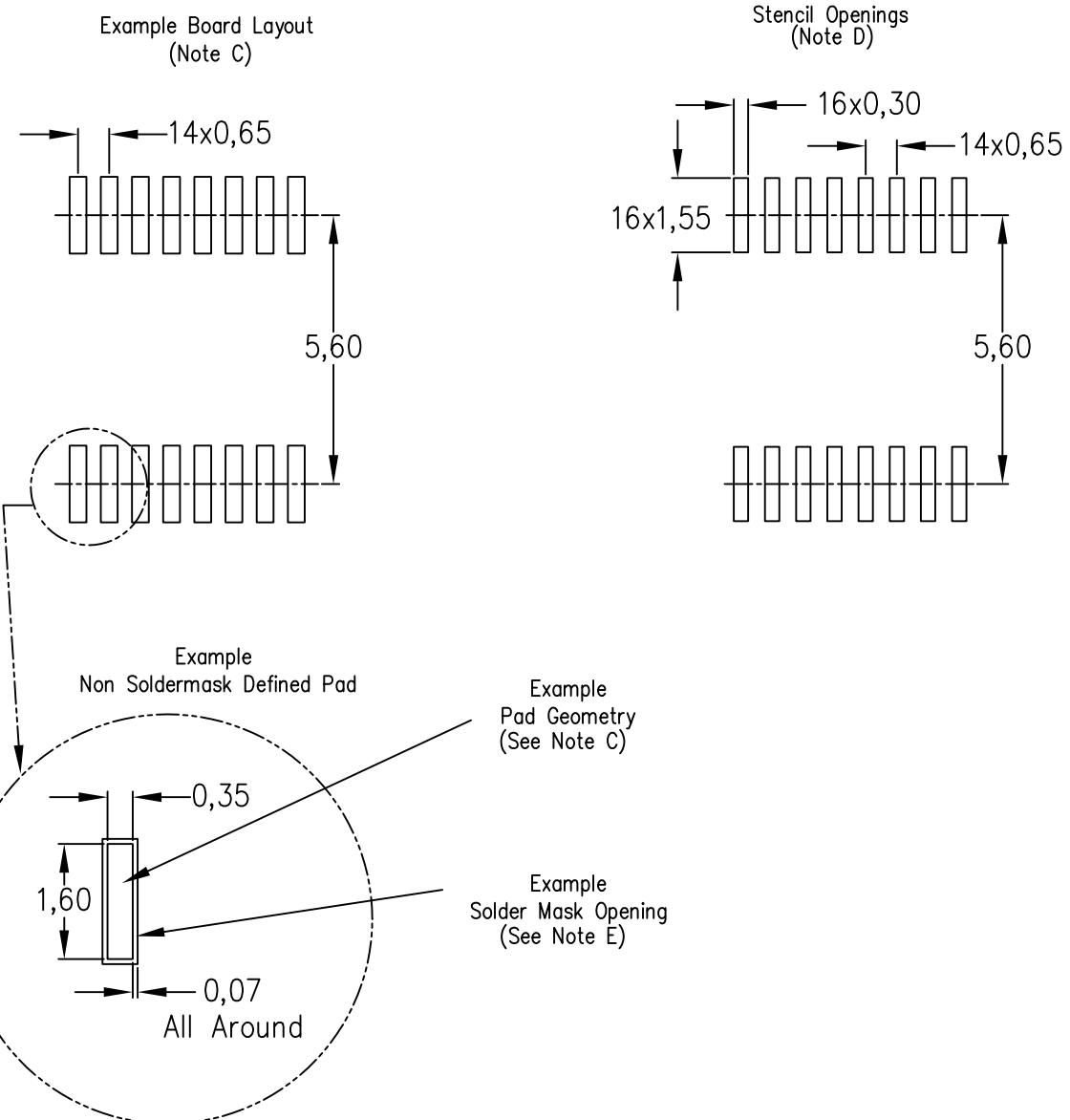
△ C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

△ D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

NOTES:

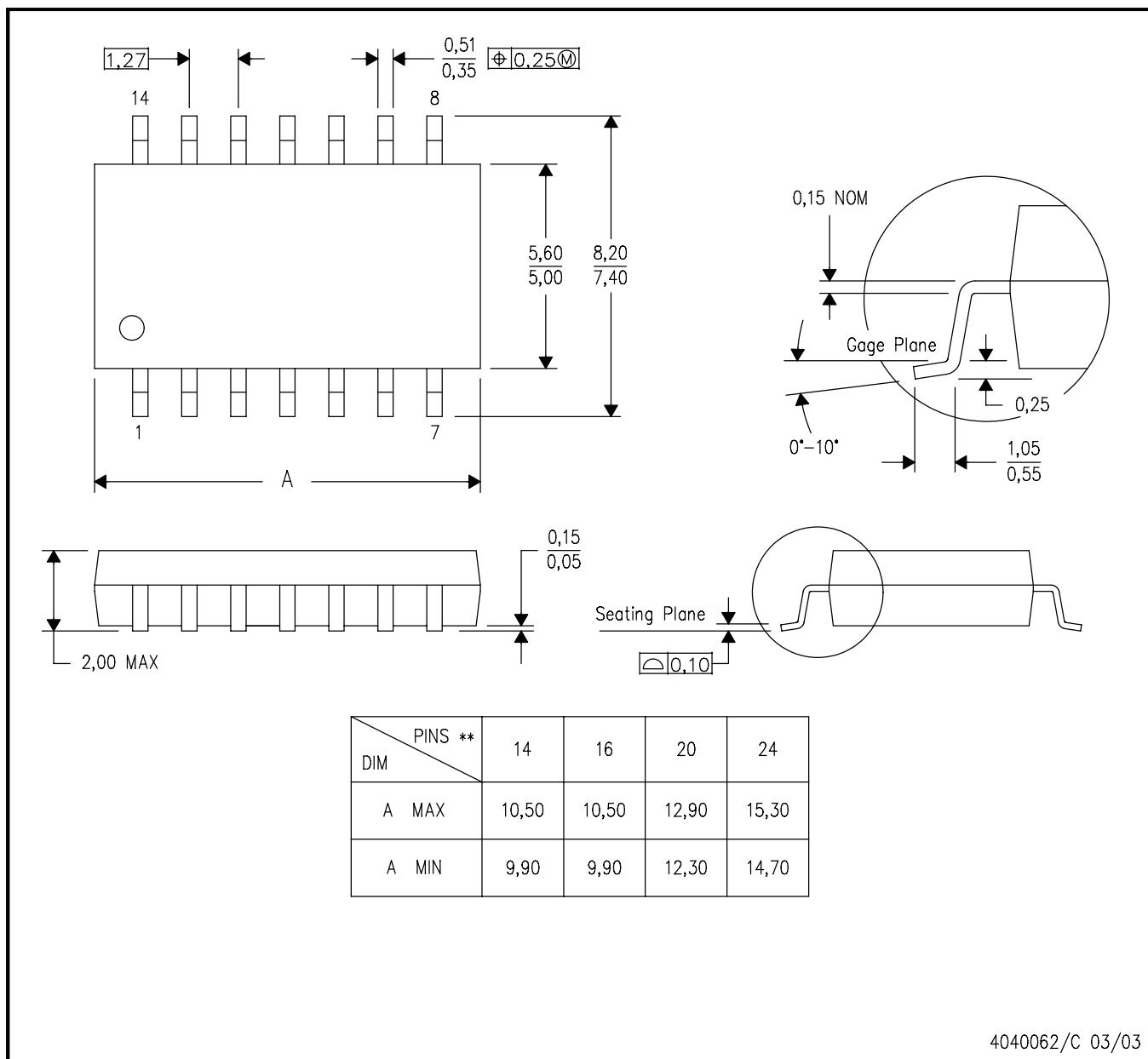
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>
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