

# HEF4011B

## Quad 2-input NAND gate

Rev. 6 — 10 December 2015

Product data sheet

### 1. General description

The HEF4011B is a quad 2-input NAND gate. The outputs are fully buffered for the highest noise immunity and pattern insensitivity to output impedance.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B
- Inputs and outputs are protected against electrostatic effects

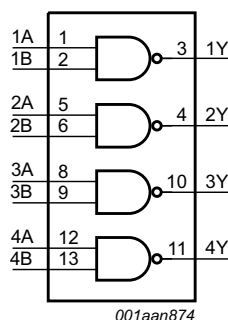
### 3. Ordering information

**Table 1.** Ordering information

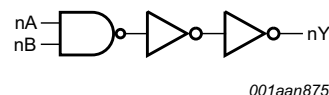
All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

Type number	Package		
	Name	Description	Version
HEF4011BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

### 4. Functional diagram



**Fig 1.** Functional diagram



**Fig 2.** Logic diagram (one gate)

5. Pinning information

5.1 Pinning

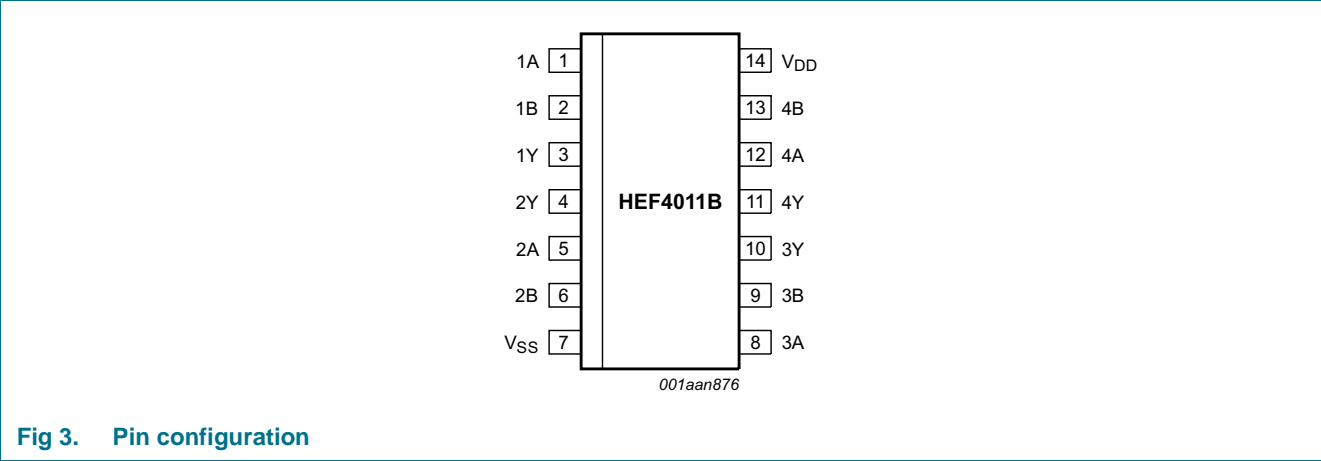


Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
nA	1, 5, 8, 12	input
nB	2, 6, 9, 13	input
nY	3, 4, 10, 11	output
V <sub>SS</sub>	7	ground (0 V)
V <sub>DD</sub>	14	supply voltage

6. Functional description

Table 3. Function table<sup>[1]</sup>

Input		Output
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level.

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V	-	$\pm 10$	mA
$I_{IO}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current		-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to + 125 °C			
		SO14 [1]	-	500	mW
$P$	power dissipation	per output	-	100	mW

[1] For SO14 packages: above  $T_{amb} = 70$  °C,  $P_{tot}$  derates linearly with 8 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5$ V	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10$ V	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15$ V	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		$T_{amb} = +125\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.1$	-	$\pm 0.1$	-	$\pm 1.0$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	all valid input combinations; $I_O = 0\text{ A}$	5 V	-	0.25	-	0.25	-	7.5	-	7.5	$\mu\text{A}$
			10 V	-	0.5	-	0.5	-	15.0	-	15.0	$\mu\text{A}$
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	$\mu\text{A}$
$C_I$	input capacitance			-	-	-	7.5	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; for waveforms see [Figure 4](#); for test circuit see [Figure 5](#); unless otherwise specified.

Symbol	Parameter	Extrapolation formula <sup>[1]</sup>	V <sub>DD</sub>	Min	Typ	Max	Unit
t <sub>pd</sub>	propagation delay	$28 + 0.55 \times C_L$	5 V <sup>[2]</sup>	-	55	110	ns
		$14 + 0.23 \times C_L$	10 V	-	25	45	ns
		$12 + 0.16 \times C_L$	15 V	-	20	35	ns
t <sub>THL</sub>	HIGH to LOW output transition time	$10 + 1.00 \times C_L$	5 V	-	60	120	ns
		$9 + 0.42 \times C_L$	10 V	-	30	60	ns
		$6 + 0.28 \times C_L$	15 V	-	20	40	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	$10 + 1.00 \times C_L$	5 V	-	60	120	ns
		$9 + 0.42 \times C_L$	10 V	-	30	60	ns
		$6 + 0.28 \times C_L$	15 V	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula ( $C_L$  in pF).

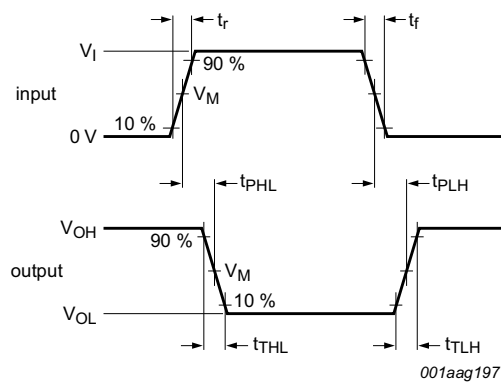
[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

**Table 8. Dynamic power dissipation**

$V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	V <sub>DD</sub>	Typical formula	Where
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	f <sub>i</sub> = input frequency in MHz; f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V <sub>DD</sub> = supply voltage in V.
		10 V	$P_D = 6000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	
		15 V	$P_D = 20100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2\text{ (}\mu\text{W)}$	

11. Waveforms

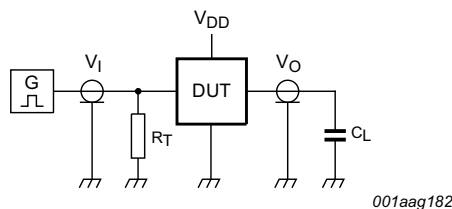


Measurement points are given in [Table 9](#).  
Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 4. Propagation delay, output transition time

Table 9. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).  
Definitions for test circuit:  
DUT = Device Under Test.  
 $C_L$  = load capacitance including jig and probe capacitance.  
 $R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

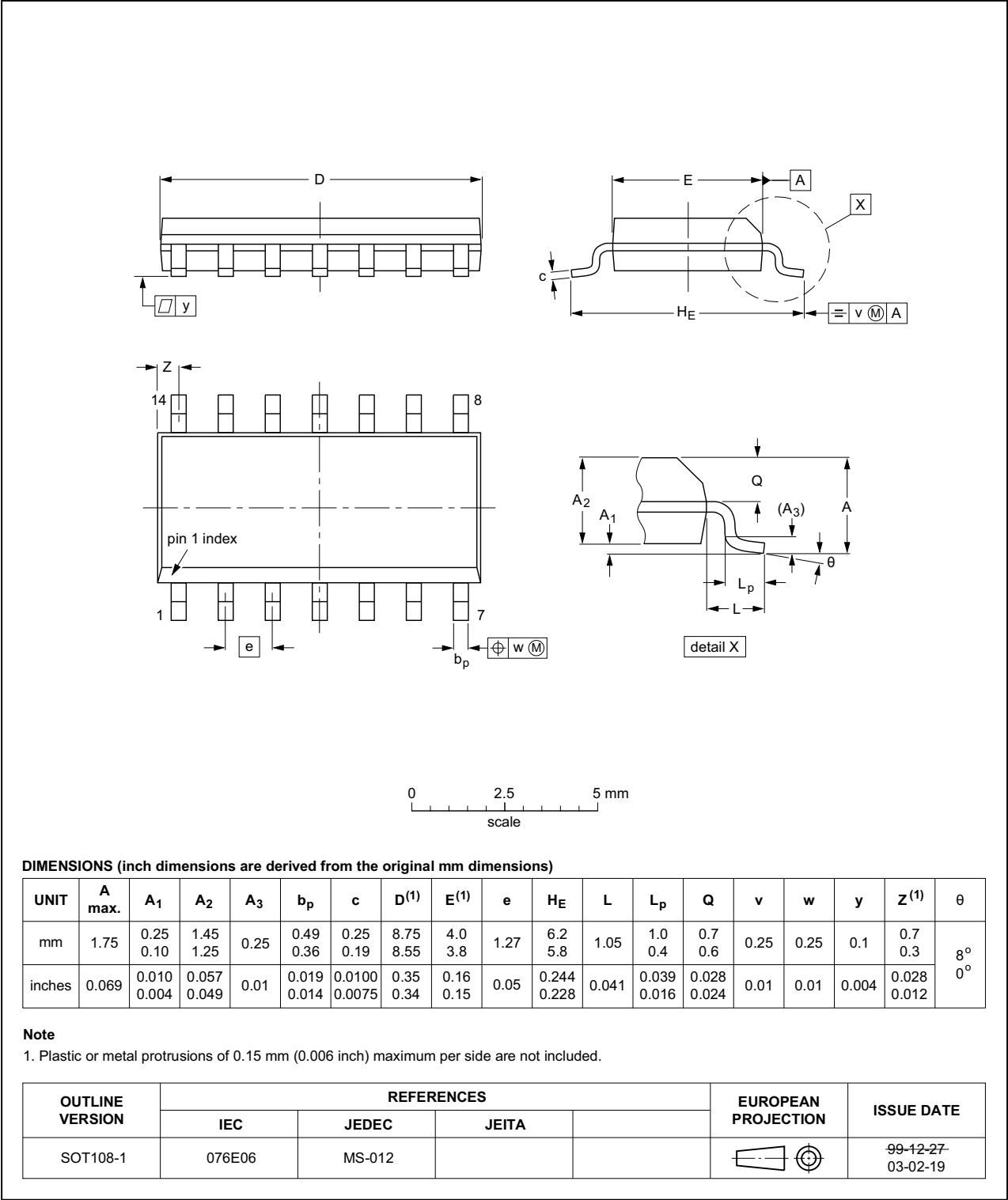


Fig 6. Package outline SOT108-1 (SO14)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4011B v.6	20151210	Product data sheet	-	HEF4011B v.5
Modifications:	<ul style="list-style-type: none"><li>Type number HEF4011BP (SOT27-1) removed.</li></ul>			
HEF4011B v.5	20111121	Product data sheet	-	HEF4011B v.4
Modifications:	<ul style="list-style-type: none"><li>Legal pages updated.</li><li>Changes in “General description” and “Features and benefits”.</li><li>Section “Applications” removed.</li></ul>			
HEF4011B v.4	20110330	Product data sheet	-	HEF4011B_CNV v.3
HEF4011B_CNV v.3	19950101	Product specification	-	HEF4011B_CNV v.2
HEF4011B_CNV v.2	19950101	Product specification	-	-



## 15. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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