Precision RRIO Dual Operational Amplifier

Enhanced Product

OP284-EP

FEATURES

Single-supply operation
Wide bandwidth: 4.25 MHz
Low offset voltage: 100 µV
Unity-gain stable
High slew rate: 4.0 V/µs
Low noise: 3.9 nV/√Hz

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Battery-powered instrumentation
Power supply control and protection
Telecommunications
DAC output amplifier
ADC input buffer

PIN CONNECTION DIAGRAM

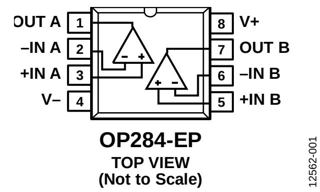

Figure 1.

GENERAL DESCRIPTION

The OP284-EP is a dual, single-supply, 4.25 MHz bandwidth amplifier featuring rail-to-rail inputs and outputs (RRIO).

The OP284-EP is guaranteed to operate from 5 V to 36 V (or ±2.5 V to ±18 V).

This amplifier is superb for single-supply applications requiring both ac and precision dc performance. The combination of wide bandwidth, low noise, and precision makes the OP284-EP useful in a wide variety of applications, including filters and instrumentation.

Other applications for this amplifier include portable telecommunications equipment, power supply control and protection, and use as an amplifier or buffer for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezoelectric, and resistive transducers.

The ability to swing rail to rail at both the input and output enables designers to build multistage filters in single-supply systems and to maintain high signal-to-noise ratios.

The OP284-EP is specified over the extended industrial temperature range of −55°C to +125°C. The OP284-EP is available in a SOIC surface-mount package.

Rev. 0
Document Feedback

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Tel: 781.329.4700

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REVISION HISTORY

5/15—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				125	µV
		−55°C ≤ T_A ≤ +125°C			250	µV
Input Bias Current	I_B			60	450	nA
		−55°C ≤ T_A ≤ +125°C			600	nA
Input Offset Current	I_{OS}					
		−55°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.0 V to 4.0 V, −55°C ≤ T_A ≤ +125°C	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 1 V ≤ V_{OUT} ≤ 4 V	50	240		V/mV
		R_L = 2 kΩ, −55°C ≤ T_A ≤ +125°C	25			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.2	2.00	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	4.80			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			125	mV
Output Current	I_{OUT}		±6.5			mA
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_{OUT} = 2.5 V, −55°C ≤ T_A ≤ +125°C			1.45	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	1.65	2.4		V/µs
Settling Time	t_S	To 0.01%, 1.0 V step		2.5		µs
Gain Bandwidth Product	GBP			3.25		MHz
Phase Margin	Φ_M			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

V_S = ±15.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				100	μV
		−55°C ≤ T_A ≤ +125°C			200	μV
Input Bias Current	I_B			80	450	nA
		−55°C ≤ T_A ≤ +125°C			600	nA
Input Offset Current	I_{OS}	−55°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			−15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −14.0 V to +14.0 V, −55°C ≤ T_A ≤ +125°C	86	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, −10 V ≤ V_{OUT} ≤ 10 V	150	1000		V/mV
		R_L = 2 kΩ, −55°C ≤ TA ≤ +125°C	75			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.2	2.00	μV/°C
Bias Current Drift	$\Delta V_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	14.8			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			−14.875	V
Output Current	I_{OUT}		±10			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.0 V to ±18 V, −55°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 0 V, −55°C ≤ T_A ≤ +125°C			2.0	mA
		V_S = ±18 V, −55°C ≤ T_A ≤ +125°C			2.25	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.0		V/μs
Full Power Bandwidth	BW_p	1% distortion, R_L = 2 kΩ, V_{OUT} = 29 V p-p		35		kHz
Settling Time	t_S	To 0.01%, 10 V step		4		μs
Gain Bandwidth Product	GBP			4.25		MHz
Phase Margin	Φ_M			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	±18 V
Input Voltage	±18 V
Differential Input Voltage[1]	±0.6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] For input voltages greater than 0.6 V, the input current must be limited to less than 5 mA to prevent degradation or destruction of the input devices.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions; that is, θ_{JA} is specified for a device soldered in the circuit board for the SOIC package.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	158	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

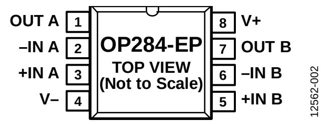

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	−IN A	Inverting Input Channel A.
3	+INA	Noninverting Input Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	−IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

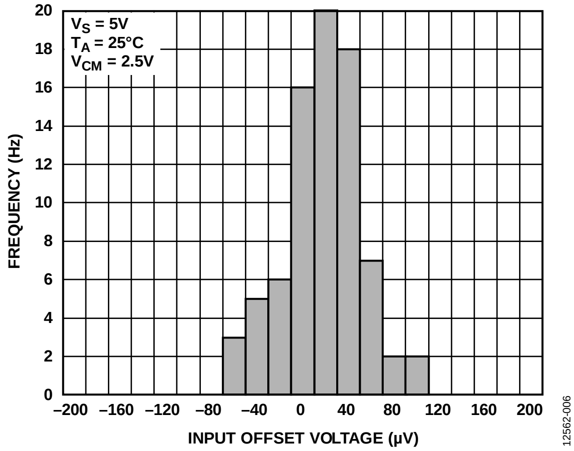

Figure 3. Input Offset Voltage Distribution, V_S = 5 V

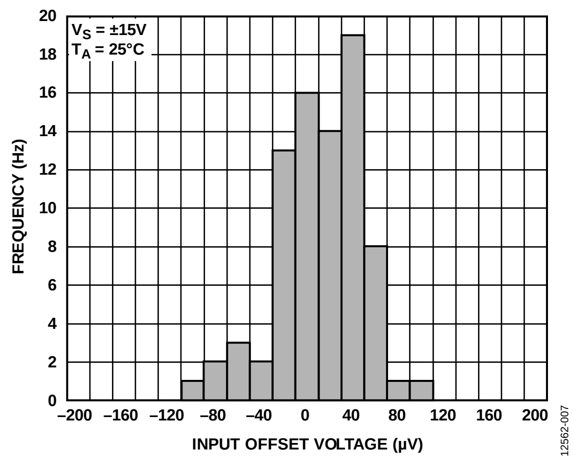

Figure 4. Input Offset Voltage Distribution, V_S = ±15 V

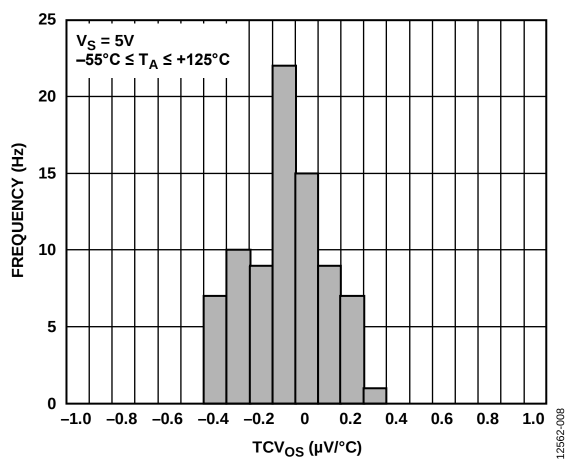

Figure 5. Input Offset Voltage Drift Distribution, V_S = 5 V

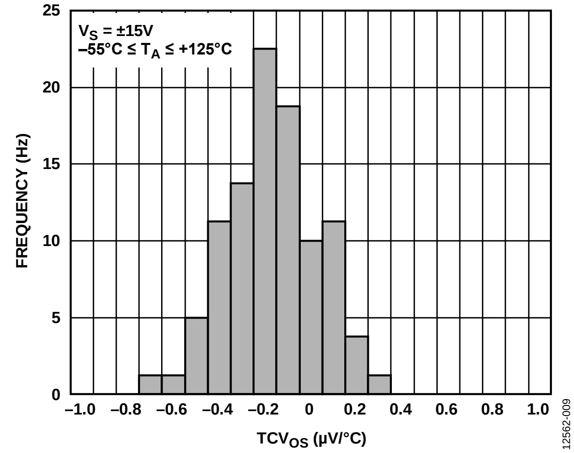

Figure 6. Input Offset Voltage Drift Distribution, V_S = ±15 V

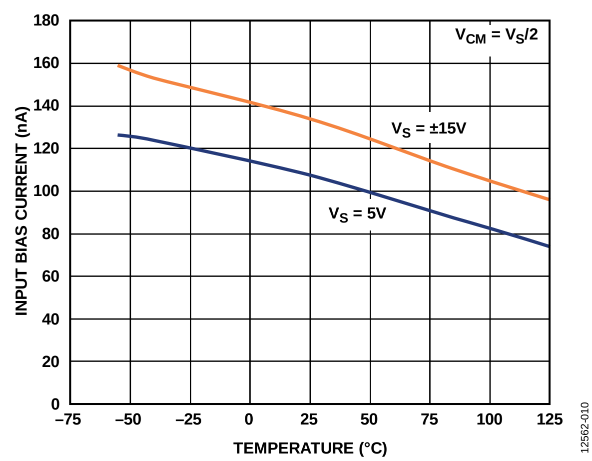

Figure 7. Bias Current vs. Temperature

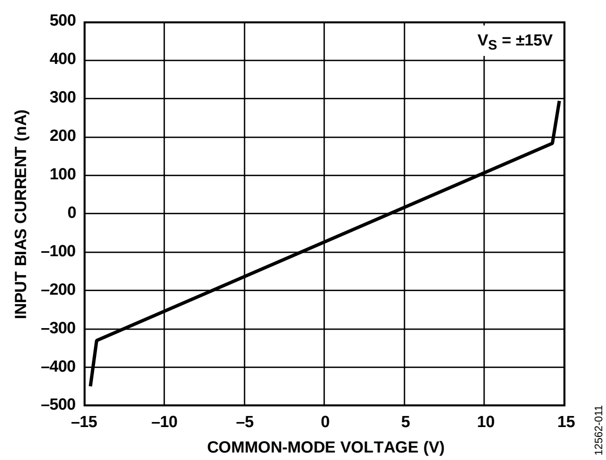

Figure 8. Input Bias Current vs. Common-Mode Voltage

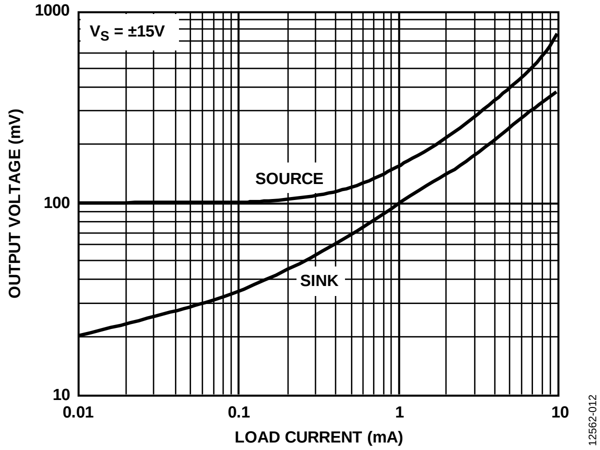

Figure 9. Output Voltage to Supply Rail vs. Load Current

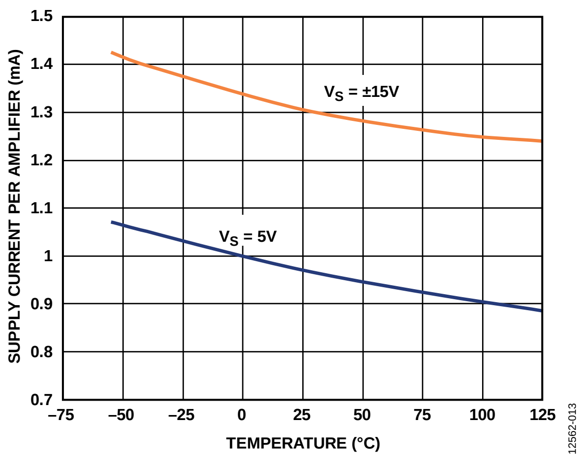

Figure 10. Supply Current vs. Temperature

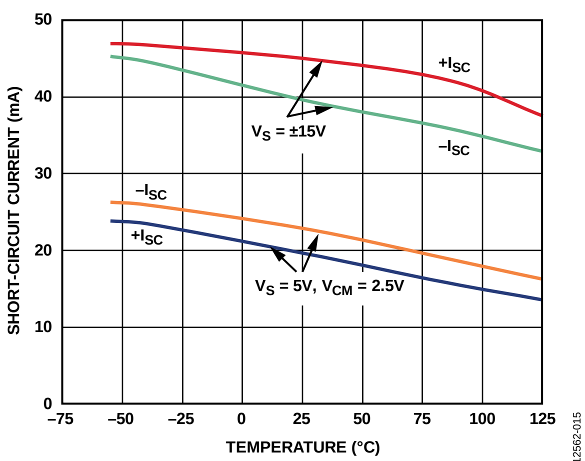

Figure 11. Short-Circuit Current vs. Temperature

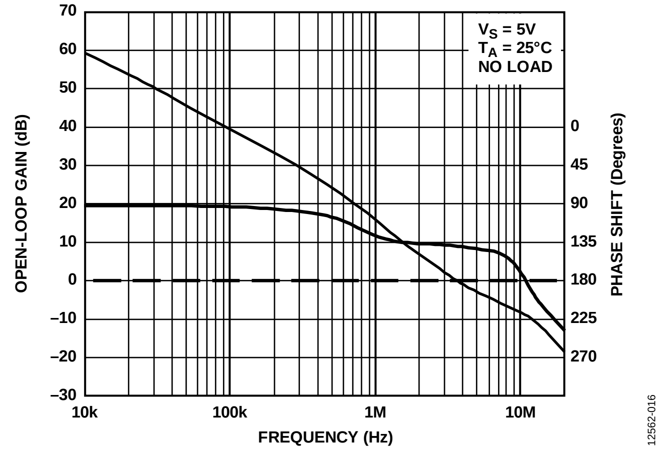

Figure 12. Open-Loop Gain and Phase vs. Frequency (No Load), $V_S = 5$ V

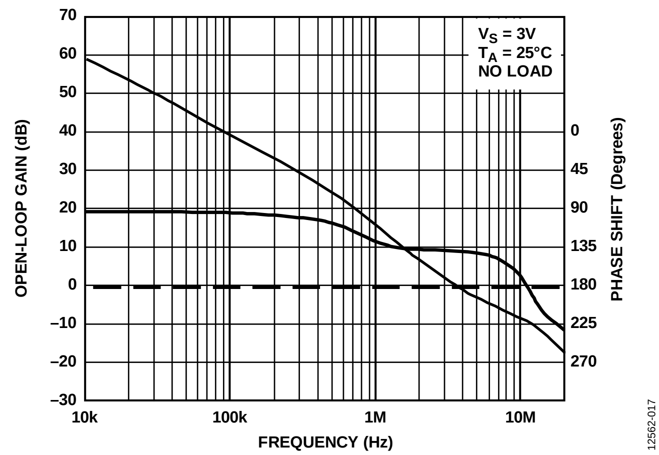

Figure 13. Open-Loop Gain and Phase vs. Frequency (No Load), $V_S = 3$ V

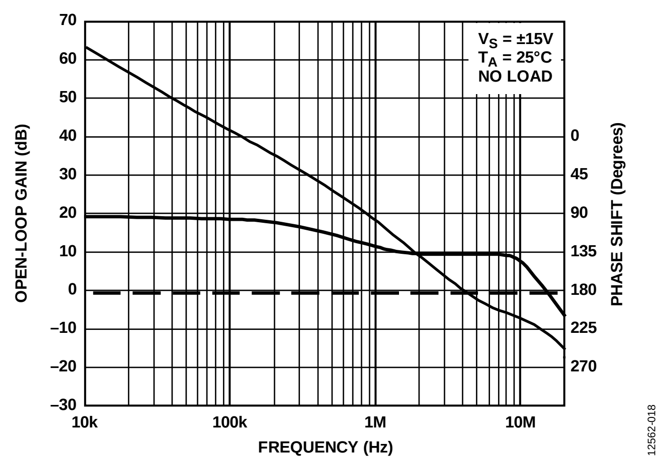

Figure 14. Open-Loop Gain and Phase vs. Frequency (No Load), $V_S = \pm 15$ V

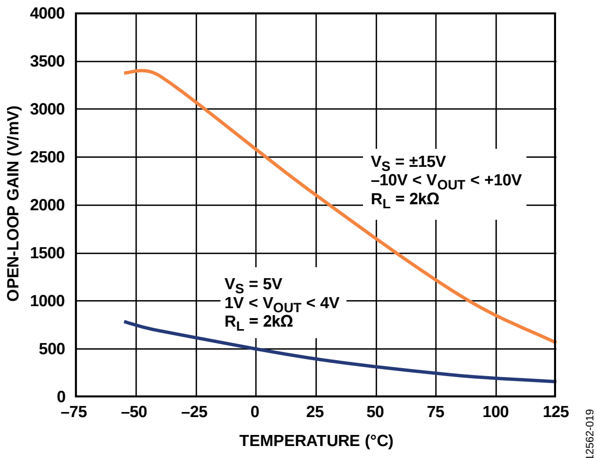

Figure 15. Open-Loop Gain vs. Temperature

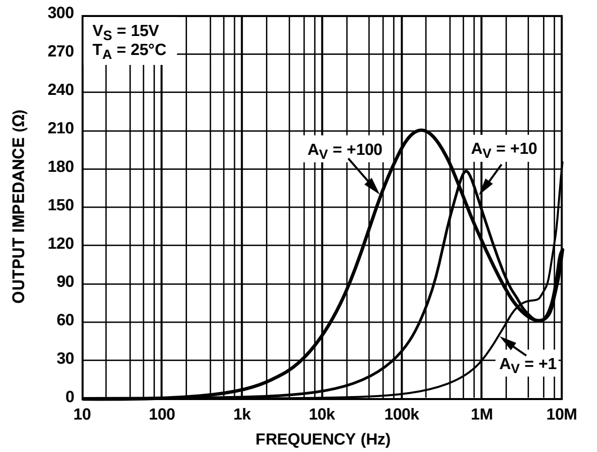

Figure 18. Output Impedance vs. Frequency

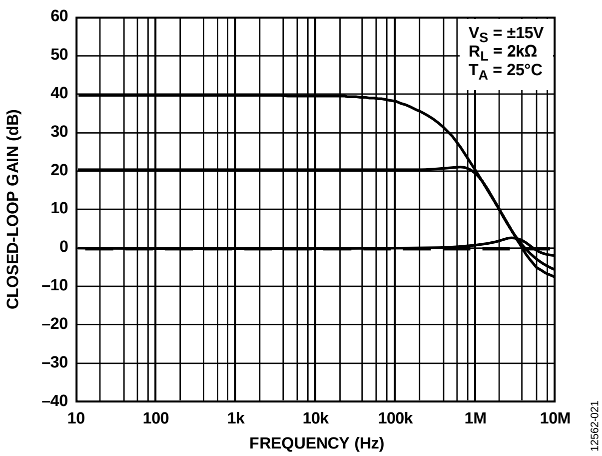

Figure 16. Closed-Loop Gain vs. Frequency (2 kΩ Load)

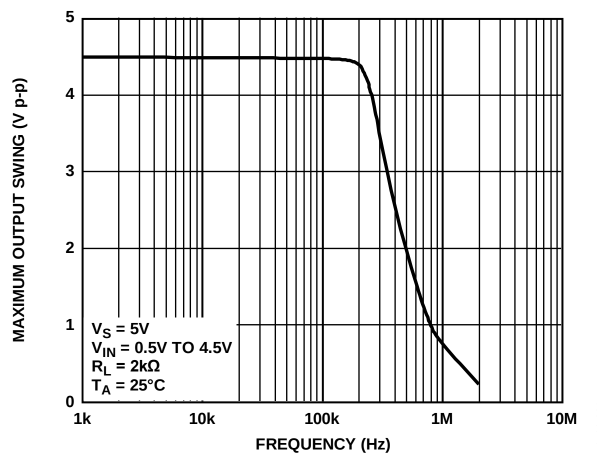

Figure 19. Maximum Output Swing vs. Frequency

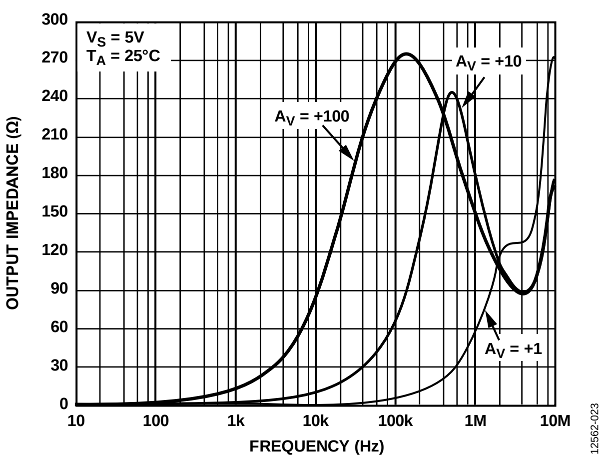

Figure 17. Output Impedance vs. Frequency

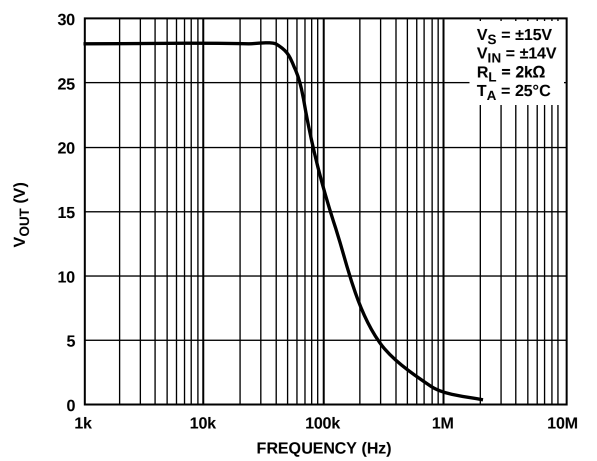

Figure 20. Maximum Output Swing vs. Frequency

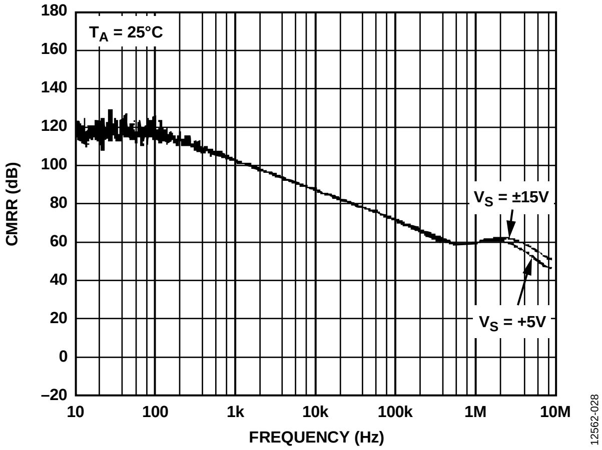

Figure 21. CMRR vs. Frequency

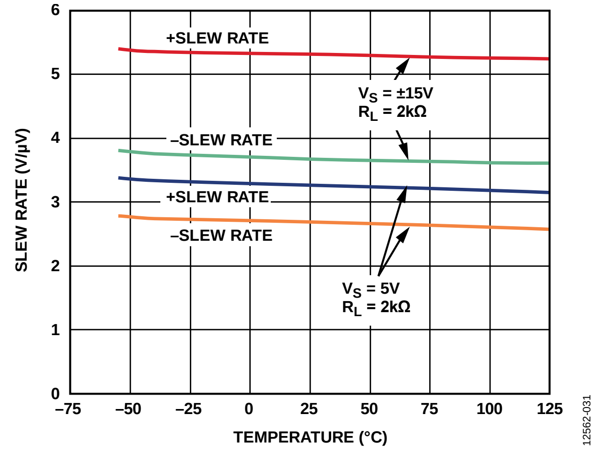

Figure 24. Slew Rate vs. Temperature

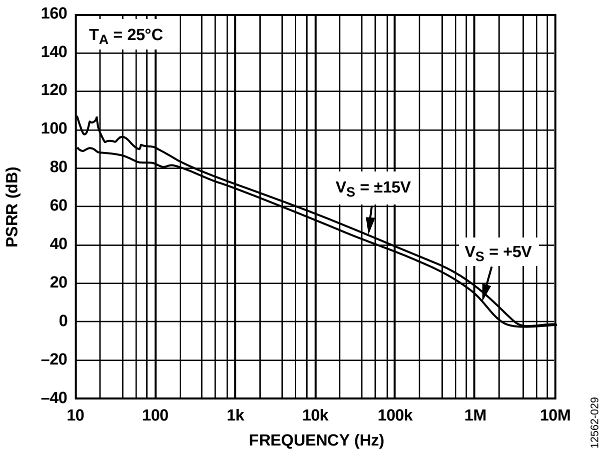

Figure 22. PSRR vs. Frequency

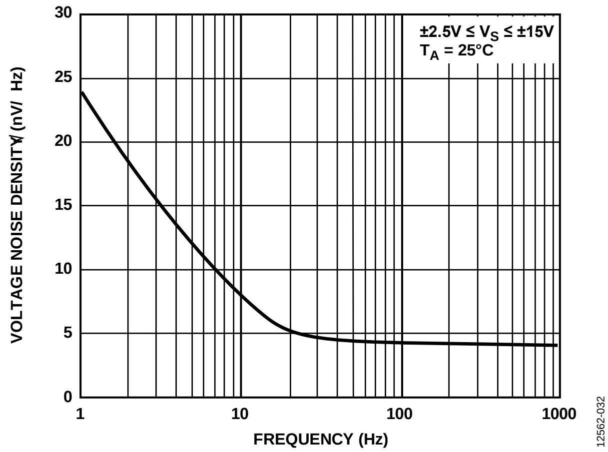

Figure 25. Voltage Noise Density vs. Frequency

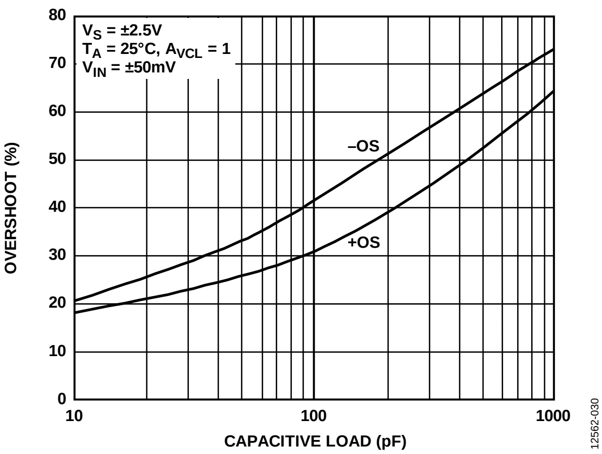

Figure 23. Small Signal Overshoot vs. Capacitive Load

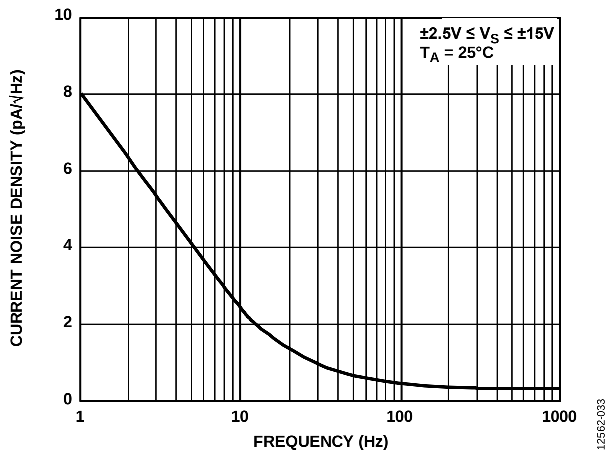

Figure 26. Current Noise Density vs. Frequency

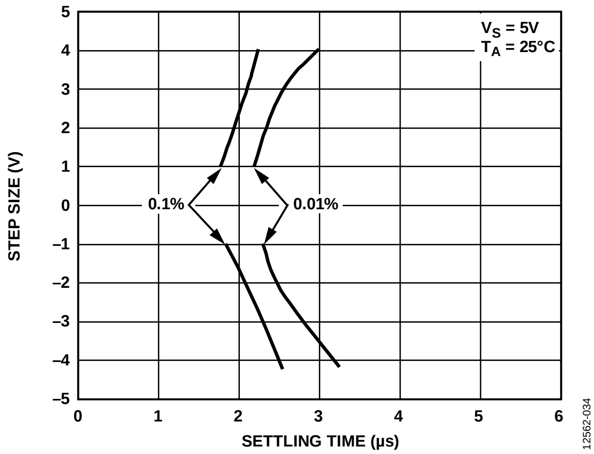

Figure 27. Step Size vs. Settling Time, V_S = 5 V

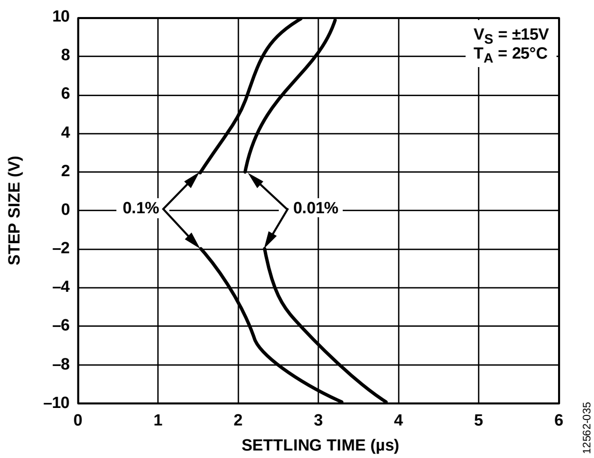

Figure 28. Step Size vs. Settling Time, V_S = ±15 V

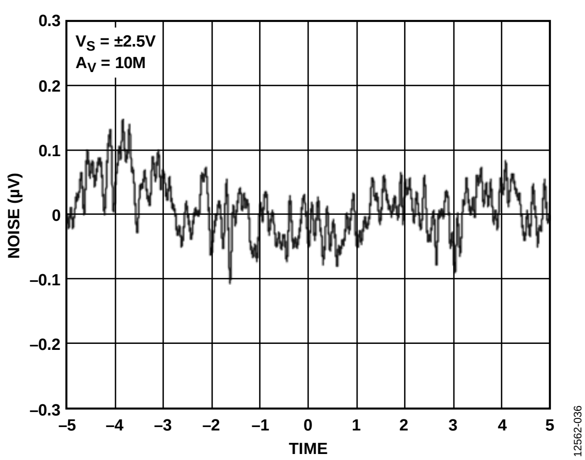

Figure 29. 0.1 Hz to 10 Hz Noise, V_S = ±2.5 V

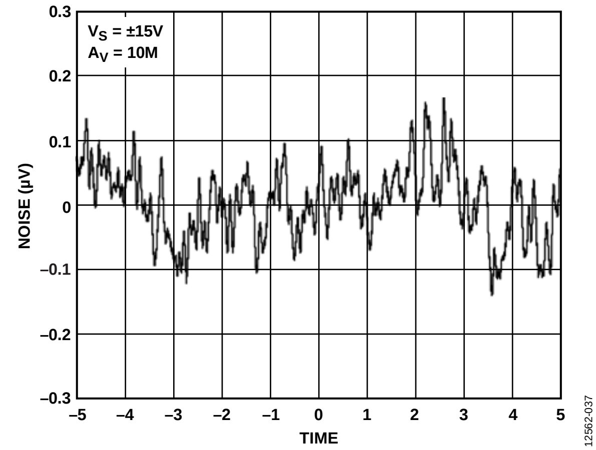

Figure 30. 0.1 Hz to 10 Hz Noise, V_S = ±15 V

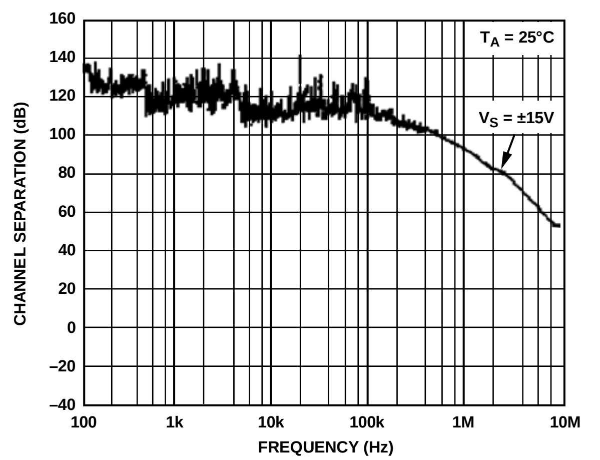

Figure 31. Channel Separation vs. Frequency

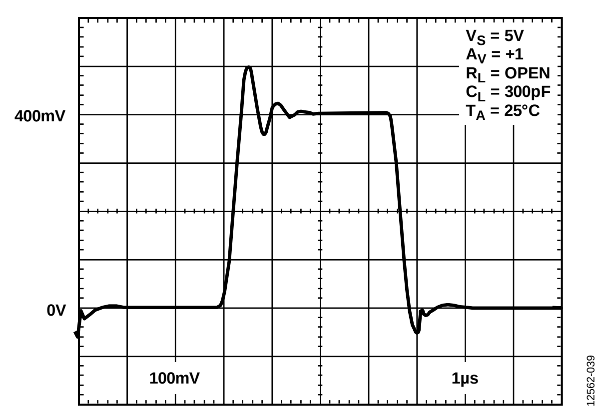

Figure 32. Small Signal Transient Response

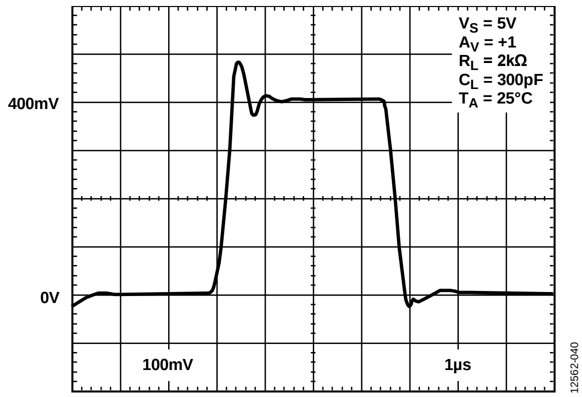

Figure 33. Small Signal Transient Response

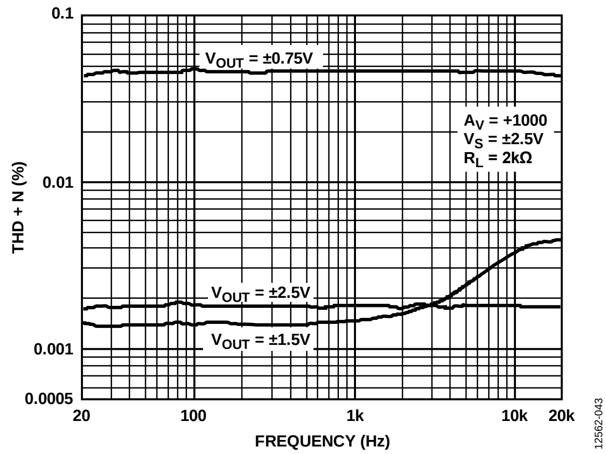

Figure 34. Total Harmonic Distortion + Noise vs. Frequency

OUTLINE DIMENSIONS

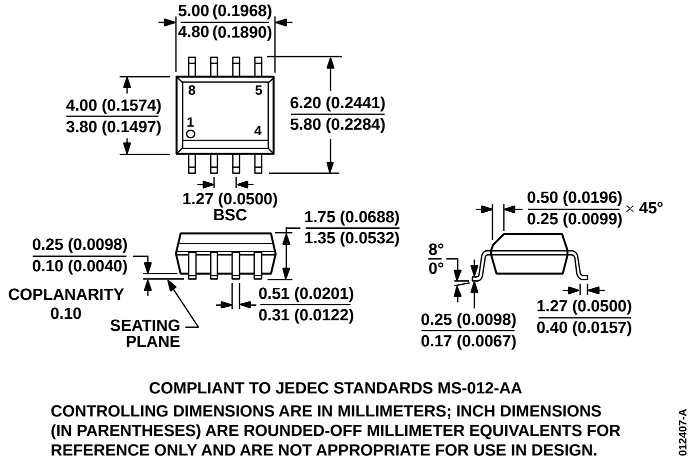

Figure 35. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
OP284TRZ-EP-R7	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.