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NTE849
Integrated Circuit
TV Horizontal/Vertical Countdown
Digital Sync System

Description:

The NTE849 is an integrated circuit in a 14–Lead DIP type package designed for use in TV horizontal/vetical countdown digital sync systems. In some video playback units, there are incorrect frequency relationships between horizontal and field frequencies. Automatic forced asynchronous mode eliminates jitter when equalizer pulses are correct, but these incorrect frequency relationships exist.

Automatic standard mode occurs upon detection of nine or more equalizing pulses during a six–line–width vertical driving period after seven fields of coincidence between integrated vertical (IV) sync and internal counter output. Standard mode is retained for seven fields of missing or mutilated vertical sync pulses.

If two or more noise pulses are detected at Pin12 during a 384–line active scan time, a noise detector reverts the system to standard mode at the next field of coincidence (without seven fields of coincidene delay). Thus, the unit stays in standard mode during tuner channel changes.

An automatic mode–recognition system places the unit in standard mode for NTSC signals or into non–synchronous mode for non–standard sync signals.

An external oscillator (NTE701) supplies an input to Pin9 that is 32 times the horizontal rate. An internal divide–by–16 counter converts this input ($32f_H$) to $2f_H$ for use elsewhere. This $32f_H$ signal is further divided to f_H, which is available at Pin11 to drive the horizontal deflection circuits. A divide–by–525 counter further divides the $2f_H$ signal to generate the vertical ramp generator timing pulses and the vertical blanking pulse.

A phasing circuit (part of the mode recognition and vertical regeneration circuits) insures that the 525 counter is reset in coincidence with the vertical sync. It does this by comparing the internally generated vertical pulse with an extrnal integrated vertical sync signal applied to Pin12. The automatic mode recognition circuit forces the NTE849 into the standard mode for NTSC signals or into the non–synchronous mode for non–standard sync signals such as video games. An input control signal (or no connection) at Pin8 places the NTE849 into non–synchronous operation.

A phasing and timing logic circuit checks to see if the line counter is in sync with the IV signal at Pin12. Seven consecutive fields of in–phase coincidence with the IV signal are needed to achieve standard mode in unless two or more noise pulses are de–detected at input Pin12 during the active scan time. In this case, normal mode will be acquired in one field.

Description (Cont'd):

In the standard divide–by–525 mode, the integrated vertical pulse is used only to provide coincidence with the 545 count (counter preset = 20, 545 – 20 = 525) in the phase detector circuit. The vertical ramp is timed by the output of the 525 counter. In standard mode, the NTE849 will maintain the divide–by–525 count for six fields of lost or mutilated sync. If the seventh field does not have the correct coincidence, the unit will switch to non–standard mode. In this mode, the vertical sync is derived from the integrated vertical pulse on a field–to–field basis. A noise immunity of 384 lines is provided. In the absence of sync pulses, the count will be 684 instead of 525 so that rapid vertical capture may be achieved when sync is restored. Non–satndard mode still may be selected by removing GND from Pin8.

The vertical retrace signal is converted to a ramp signal if a capacitor is connected between Pin3 and GND. The ramp's slope corresponds to vertical size and is controlled by changing the input current to Pin2. The ramp is connected to the inverting input of a diffrence amplifier. The output of this amplifier, connectd to Pin6, is used to drive the vertical output stage. The non–inverting input of the difference amplifier is at Pin5. A voltage derived from yoke current may be applied to this pin for linearity improvement.

The pulse width of the vertical blanking signal at Pin7 is 608 clocks wide in the synchronous mode, and is adjustable in width by changing the monostable RC network at Pin10 for the non–synchronous mode.

The proportional voltage regulator output at Pin4 is about 43% of the supply voltage at Pin12. The maximum external load current is 20mA (Peak).

Features:

- Automatic Forced Asynchronous Mode to Remove Jitter
- Improved Low Voltage Start–Up Operation
- Lower Zero–State Horizontal–Drive Pulse Output
- Improved Symmetry for Horizontal–Drive Output
- Improved Automatic Standard Operation
- Noise Detector
- Handles Standard NTSC and Non–Standard Signals
- Automatic Mode Recognition
- Clock Input
- Vertical Ramp (Sawtooth) Generator
- Vertical Amplifier
- Vertical Blanking Generator
- Horizontal Drive Pulse Output
- Ratio–Voltage Regulator
- Inherent Interlace for NTSC Signals
- Vertical–Hold Control Eliminated
- Supply Voltage Range: 10.8V to 13.2V
- Rapid Pull–In
- Co–Channel Sync Lockout for NTSC Signals
- I^2L Logic

Absolute Maximum Ratings:

DC Supply Voltage 15V

Device Dissipation ($T_A \le +70°C$) 530mW
Derate Linearily Above 70°C . . . . . 6.7mW/°C

Operating Ambient Temperature Range . . . . . 0° to +70°C

Storage Temperature Range . . . . . –55° to +150°C

Lead Temperature (During Soldering, 1/16" from case, 10sec max) . . . . . +265°C

Electrical Characteristics: (T_A = +25°C, all switches open, test pin 2 & 14 = GND unless otherwise specified)

Parameter	Test Conditions	Min	Max	Unit
Amplifier Gain, V6	S2, S5, S6 Colsed, Note 1 Test pin 1 = 12V, 16 = $1V_{RMS}$ at 1kHz	0.178	3.16	V_{RMS}
Horizontal Frequency Divider Ratio, $f_g \div f_{11}$	S3, S7, S8 Closed, Note 7, Test pin 1 = 14.4V	32	32	Ratio
Horizontal Pulse Width, Pin11	S3, S7, S8 Closed, Notes 9, 10, Test pin 1 = 8.4V	28	34	µs
	S3, S7, S8 Closed, Notes 9, 10, 11, Test pin1 = 14.4V	28	34	µs
Asynchronous Non–Coincident Frequency Divide Ratio, $f_g \div f_3$	S3, S7, S8 Closed, Notes 9, 12, 13, 14, 15, Test pin 1 = 14.4V, 8 = 0.2V, 12 = 1.5V	10944	10944	Ratio
Ramp Charge Pulse Width, Pin3	S3, S7, S8 Closed, Notes 13, 15, Test pin 1 = 14.4V, 8 = 0.2V, 12 = 1.5V	585	585	µs
Asynchronous Coincident Noise Immunity, Hold–Off Frequency Divide Ratio, $f_8 \div f_3$	Notes 9, 12, 13, 15, 16, 17, Test pin 1 = 14.4V, 8 = 0.2V	7872	7872	Ratio
Synchronous Divider Ratio, $f_g \div f_3$	S3, S7, S8 Closed, Notes 9, 13, 15, 18, 19, Test pin 1 = 14.4V, 8 = 0.2V, 12 = 1.5V	8400	8400	Ratio
Ramp Charge Pulse Width, Pin3	S3, S7, S8 Closed, Notes 9, 10, 13, 15, 18, 20, Test pin 1 = 14.4V, 8 = 0.2V, 12 = 1.5V	190	194	Clocks
Vertical Blanking Pulse Width, Pin7	S3, S7, S8 Closed, Notes 9, 10, 13, 15, 18, 21, Test pin 1 = 14.4V, 8 = 0.2V, 12 = 1.5V	606	610	Clocks
Mode Recognition Field Count Frequency Divide Ratio, $f_g \div f_3$	S3, S7, S8 Closed, Notes 9, 13, 14, 15, 18, 22, Test pin 1 = 12.0V, 8 = 0.2V, 12 = 1.5V			
Synchronous to Non–Synchronous	Initial Fields 9 Serrations	8400	8400	Ratio
	First Field, 8 Serrations	8400	8400	Ratio
	Second Field, 8 Serrations	8400	8400	Ratio
	Third Field, 8 Serrations	8400	8400	Ratio
	Fourth Field, 8 Serrations	8400	8400	Ratio
	Fifth Field, 8 Serrations	8400	8400	Ratio
	Sixth Field, 8 Serrations	8400	8400	Ratio
	Seventh Field, 8 Serrations	10944	10944	Ratio
Mode Recognition Field Count Frequency Divide Ratio, $f_g \div f_3$	S3, S7, S8 Closed, Notes 9, 13, 15, 18, 23, Test pin 1 = 12.0V, 8 = 0.2V			
Non–Synchronous to Synchronous	First Field	8384	8384	Ratio
	Second Field	8384	8384	Ratio
	Third Field	8384	8384	Ratio
	Fourth Field	8384	8384	Ratio
	Fifth Field	8384	8384	Ratio
	Sixth Field	8384	8384	Ratio
	Seventh Field	8384	8384	Ratio
	Eight Field	8400	8400	Ratio
	Ninth Field	8400	8400	Ratio
Fast Standard–Mode Resynchronization	S3, S7, S8 Closed, Notes 9, 13, 15, Test pin 1 = 12.0V, 8 = 0.2V			

Static Characteristics: (T_A = +25°C V+ = 12V, switches open, test pin 2, 8, 12, & 14 = GND unless otherwise specified)

Parameter	Test Conditions	Connect Test Pins as Shown Below								Min	Max	Unit
		1	3	4	5	6	10	11	13			
Ratio Regulator Voltage, V_4 Load	S2 Closed, Note 1	12V		–20mA	2V					4.9	5.5	V
No Load		14.4V			2V					5.8	6.8	V
Vertical Blanking Output, V_7 Unblanked	S2 Closed	12V		–20mA	GND					2.5	5.0	V
Blanked	Notes 1, 4	12V			GND					0.09	0.5	V
Horizontal Output Voltage, V_{11} High	Test pin 15 = 8V S2 Closed	14.4			GND					7.0	8.1	V
Low	Notes 5, 6	12V			GND			20mA		0	0.12	V
Vertical Output Voltage, V_6 Off	S4 Closed, Note 1	12V			GND	1mA				0.6	1.4	V
On	S3 Closed, Note 1	12V	GND			–20mA				3.4	5.1	V
Difference Voltage, $V_3 – V_5$	S2 Closed, Note 1	12V			4V	–20mA				–0.15	0.15	V
Supply Current, I_1	S2 Closed, Note 1	14.4V			2V					10	35	mA
Clock Current, I_9: Low	Test pin 9 = GND, S2 Closed, Note 2	14.4V			2V					–180	–70	µA
Voltage, V_9	S2 Closed, Note 3	14.4V			2V					–	0.75	V
Composite Sync Input Current, I_{13} Sync High	S2 Closed, Note 1	12V			2V				4V	100	700	µA
Sync Low		14.4V			2V				0V	–25	25	mA
Forced Asynchronous Current, I_8	S2 Closed, Note 3, Test pin 8 = 4.5V	12V			2V					1.0	3.2	mA
Ramp Current, I_3	S3 Closed, Note 1, Test pin 2 = 50µA	12V	4.5V							45	57	µA
ΔRamp Current, ΔI_3		12V	1.5V							–3	3	µA
Async Time Constant Current, I_{10} Charge	S2 Closed, Note 4	12V			2V		3.0V			10	40	µA
Discharge		12V			2V		4.5V			1	5	mA
Vert Sync Input Current, I_{12} Normal	S2 Closed, Note 4, Test pin 12 = 2.3V	12V			2V					–0.1	5.0	µA
Overdrive	S2 Closed, Note 4, Test pin 12 = 3.0V	12V			2V					01	3.0	mA

Notes:

Note 1. Stop clock when Pin7 is high.
Note 2. Stop clock when Pin9 is low.
Note 3. Stop clock when Pin9 is high.
Note 4. Stop clock when Pin7 is low.
Note 5. Stop clock when Pin11 is high.
Note 6. Stop clock when Pin11 is low.
Note 7. Clock frequency = 600kHz, clock amplitude: low ≤ 0.45V, high ≥ 0.95V (5V max).
Note 8. Frequency at Pin9 (clock) divided by frequency at Pin11 (horizontal out).
Note 9. Clock frequency = 500kHz, clock amplitude same as Note 7.
Note 10. Pulse width measured at 2V point on output waveform.
Note 11. Total capacity = 50pF when measuring pulse width.
Note 12. Sync serrations = 8.
Note 13. Sync amplitude: low state ≤ 1.2V, high state ≥ 4V (6V max with positive sync tips).

Notes (Cont'd):

Note 14. Frequency at Pin9 (clock) divided by frequency at Pin3 (ramp control).

Note 15. Initilize or repeat initilization procedure before doing this test.

Note 16. Apply a pulse 1 clock wide, 7808 clocks after first positive transition at Pin3.

Note 17. Default count determined by 684 x 16(H) = 10944.

Note 18. Sync serrations = 9.

Note 19. Hold–off count determined by 492 x 16(H) = 7872.

Note 20. Number of clocks occurring within ramp gate period.

Note 21. Number of clocks occurring during the blanking gate period.

Note 22. This series of tests checks the mode recognition circuits. The first test after initialization applies 9 serrations at the sync input pin. The IC should go to the synchronous count ratio of 8400. During the next seven fields only 8 serrations are applied. The NTE849 should maintain the synchronous count ratio of 8400 for the first six fields. At the seventh field the NTE849 should go to default count of 10944. The test concludes with a 9–serration input. The NTE849 should revert to a synchronous count of 8400.

Note 23. This test checks the operation of the out–of–sync detector by applying out–of–phase sync pulses to Pin12. The NTE849 will count eight fields before resetting to the sync pulse.

Note 24. Initialize by 8364 sync for eight fields before test.

Note 25. This test verifies the operation of the fast resync performance by simulating a noise pulse (5 to 50 clocks wide) applied to the IV pin 4000 to 6000 clocks (8ms to 12ms) after IV sync. Initialize to non–sync mode before performing this test. The IC should resync in the next field and be maintained for the standard confidence count of seven fields.

Pin Connection Diagram