High Voltage Latch-Up Proof, Dual SPST Switches

Data Sheet

ADG5421/ADG5423

FEATURES

- Latch-up immune under all circumstances
- Human body model (HBM) ESD rating: 8 kV
- Low on resistance: 13.5 Ω
- ±9 V to ±22 V dual-supply operation
- 9 V to 40 V single-supply operation
- 48 V supply maximum ratings
- Fully specified at ±15 V, ±20 V, +12 V, and +36 V
- V_{DD} to V_{SS} analog signal range

APPLICATIONS

- High voltage signal routing
- Automatic test equipment
- Analog front-end circuits
- Precision data acquisition
- Industrial instrumentation
- Amplifier gain select
- Relay replacement

FUNCTIONAL BLOCK DIAGRAMS

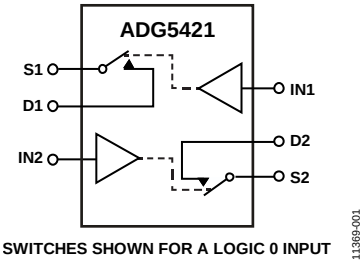

Figure 1. ADG5421

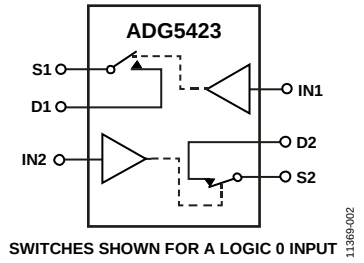

Figure 2. ADG5423

GENERAL DESCRIPTION

The ADG5421/ADG5423 are monolithic industrial, complementary metal oxide semiconductor (CMOS) analog switches containing two independent latch-up immune single-pole/single-throw (SPST) switches. Each switch conducts equally well in both directions when on, and has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. Both ADG5421 switches are turned on with a Logic 1 input, whereas the ADG5423 has one switch turned on and one switch turned off for a Logic 1 input. The ADG5423 exhibits break-before-make action for use in multiplexer applications.

The ultralow on resistance and on-resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications where low distortion is critical. The latch-up immune construction and high ESD rating make these switches more robust in harsh environments.

PRODUCT HIGHLIGHTS

1. Trench isolation guards against latch-up. A dielectric trench separates the P channel and N channel transistors, thereby preventing latch-up even under severe overvoltage conditions.
2. Low R_{ON} of 13.5 Ω.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG5421/ADG5423 can operate from dual supplies up to ±22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG5421/ADG5423 can operate from a single-rail power supply up to 40 V.
5. 3 V logic compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
6. No V_L logic power supply required.
7. Available in 10-lead MSOP and 10-lead 3 mm × 3 mm LFCSP packages.

Rev. A

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REVISION HISTORY

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Changes to Figure 30 ... 14
Updated Outline Dimensions ... 17
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9/13—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	13.5			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 25
	15	19	23	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.8			Ω typ	V_S = ±10 V, I_S = −10 mA
	2.2	2.7	3.1	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 24
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 24
	±0.25	±1	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 23
	±0.4	±4	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	185			ns typ	R_L = 300 Ω, C_L = 35 pF
	220	273	313	ns max	V_S = 10 V; see Figure 30
t_{OFF}	163			ns typ	R_L = 300 Ω, C_L = 35 pF
	196	219	242	ns max	V_S = 10 V; see Figure 30
Break-Before-Make Time Delay, t_D (ADG5423 Only)	73			ns typ	R_L = 300 Ω, C_L = 35 pF
			21	ns min	V_{S1} = V_{S2} = 10 V; see Figure 32
Charge Injection, Q_{INJ}	95			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Total Harmonic Distortion + Noise	0.01			% typ	R_L = 1 kΩ, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 27
−3 dB Bandwidth	250			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
Insertion Loss	−1			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
C_S (Off)	12			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	13			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	44			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			μA typ	Digital inputs = 0 V or V_{DD}
	55		70	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	12.5			Ω typ	V_S = ±15 V, I_S = −10 mA; see Figure 25
	14	18	22	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = ±15 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	2.3			Ω typ	V_S = ±15 V, I_S = −10 mA
	2.7	3.3	3.7	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 24
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 24
	±0.25	±1	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±15 V; see Figure 23
	±0.4	±4	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	168			ns typ	R_L = 300 Ω, C_L = 35 pF, V_S = 10 V; see Figure 30
	199	243	276	ns max	V_S = 10 V; see Figure 30
t_{OFF}	156			ns typ	R_L = 300 Ω, C_L = 35 pF
	184	204	218	ns max	V_S = 10 V; see Figure 30
Break-Before-Make Time Delay, t_D (ADG5423 Only)	65			ns typ	R_L = 300 Ω, C_L = 35 pF
			38	ns min	V_{S1} = V_{S2} = 10 V; see Figure 32
Charge Injection, Q_{INJ}	120			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Total Harmonic Distortion + Noise	0.01			% typ	R_L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 27
−3 dB Bandwidth	250			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
C_S (Off)	11			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	12			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	44			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			μA typ	Digital inputs = 0 V or V_{DD}
	70		110	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	26			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 25
	30	38	44	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	1	1.5	1.6	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	5.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	6.8	8.3	12.3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V; see Figure 24
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V to 10 V, V_D = 10 V to 1 V; see Figure 24
	±0.25	±1	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V to 10 V; see Figure 23
	±0.4	±4	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	295			ns typ	R_L = 300 Ω, C_L = 35 pF
	370	470	540	ns max	V_S = 8 V; see Figure 30
t_{OFF}	192			ns typ	R_L = 300 Ω, C_L = 35 pF
	235	273	295	ns max	V_S = 8 V; see Figure 30
Break-Before-Make Time Delay, t_D (ADG5423 Only)	142			ns typ	R_L = 300 Ω, C_L = 35 pF
			78	ns min	V_{S1} = V_{S2} = 8 V; see Figure 32
Charge Injection, Q_{INJ}	55			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Total Harmonic Distortion + Noise	0.03			% typ	R_L = 1 kΩ, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 27
−3 dB Bandwidth	290			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
Insertion Loss	−1.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
C_S (Off)	14			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	15			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	38			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			μA typ	Digital inputs = 0 V or V_{DD}
	50		65	μA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	14.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA; see Figure 25
	16	20	24	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.1			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	0.8	1.3	1.4	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	3.5			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	4.3	5.5	6.5	Ω max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V; see Figure 24
	±0.25	±1	±10	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V to 30 V, V_D = 30 V to 1 V; see Figure 24
	±0.25	±1	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V to 30 V; see Figure 23
	±0.4	±4	±20	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	6			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	181			ns typ	R_L = 300 Ω, C_L = 35 pF
	210	245	280	ns max	V_S = 18 V; see Figure 30
t_{OFF}	170			ns typ	R_L = 300 Ω, C_L = 35 pF
	192	205	220	ns max	V_S = 18 V; see Figure 30
Break-Before-Make Time Delay, t_D (ADG5423 Only)	66			ns typ	R_L = 300 Ω, C_L = 35 pF
			37	ns min	V_{S1} = V_{S2} = 18 V; see Figure 32
Charge Injection, Q_{INJ}	110			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 31
Off Isolation	−55			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Total Harmonic Distortion + Noise	0.01			% typ	R_L = 1 kΩ, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 27
−3 dB Bandwidth	260			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 28
Insertion Loss	−0.9			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
C_S (Off)	13			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	16			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	38			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}	80			μA typ	Digital inputs = 0 V or V_{DD}
	100		130	μA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT, Sx OR Dx					θ_{JA} = 133.1°C/W
10-Lead MSOP					
V_{DD} = +15 V, V_{SS} = −15 V	84	58	39	mA maximum	
V_{DD} = +20 V, V_{SS} = −20 V	89	60	41	mA maximum	
V_{DD} = 12 V, V_{SS} = 0 V	67	47	32	mA maximum	
V_{DD} = 36 V, V_{SS} = 0 V	87	59	40	mA maximum	
10-Lead LFCSP					θ_{JA} = 48.7°C/W
V_{DD} = +15 V, V_{SS} = −15 V	129	80	48	mA maximum	
V_{DD} = +20 V, V_{SS} = −20 V	135	83	50	mA maximum	
V_{DD} = 12 V, V_{SS} = 0 V	103	37	43	mA maximum	
V_{DD} = 36 V, V_{SS} = 0 V	132	82	49	mA maximum	

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx or Dx Pins	300 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
10-Lead MSOP (4-Layer Board)	133.1°C/W
10-Lead LFCSP	48.7°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
Human Body Model (HBM) ESD	8 kV

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

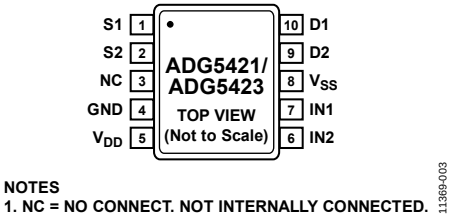

Figure 3. MSOP Pin Configuration

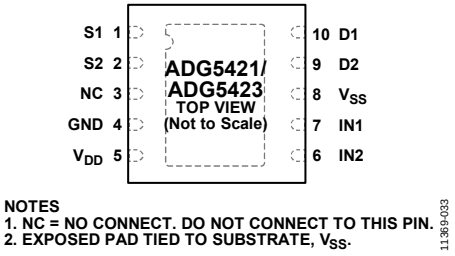

Figure 4. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

MSOP Pin No.[1]	LFCSP Pin No.	Mnemonic	Description
1	1	S1	Source Terminal 1. This pin can be an input or output.
2	2	S2	Source Terminal 2. This pin can be an input or output.
3	3	NC	No Connect. Not internally connected.
4	4	GND	Ground (0 V) Reference.
5	5	V_{DD}	Most Positive Power Supply Potential.
6	6	IN2	Logic Control Input.
7	7	IN1	Logic Control Input.
8	8	V_{SS}	Most Negative Power Supply Potential.
9	9	D2	Drain Terminal 2. This pin can be an input or output.
10	10	D1	Drain Terminal 1. This pin can be an input or output.
N/A	EPAD		Exposed Pad. The exposed pad is tied to substrate, V_{SS}.

[1] N/A means not applicable.

Table 8. ADG5421 Truth Table

INx	Switch Conditions
0	Off
1	On

Table 9. ADG5423 Truth Table

INx	Switch 1 Condition	Switch 2 Condition
0	Off	On
1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

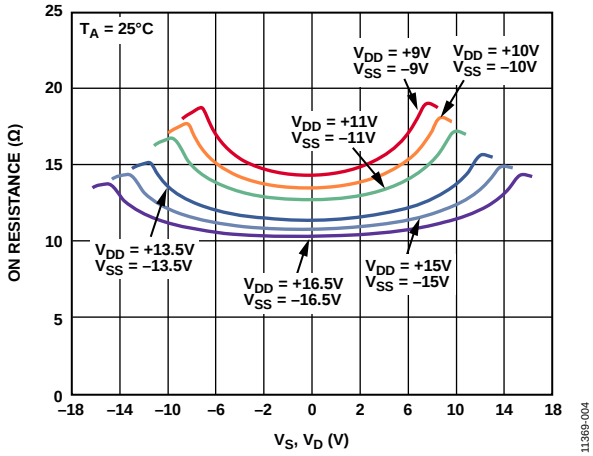

Figure 5. On Resistance as a Function of V_S, V_D (Dual Supply: ±10 V, ±15 V)

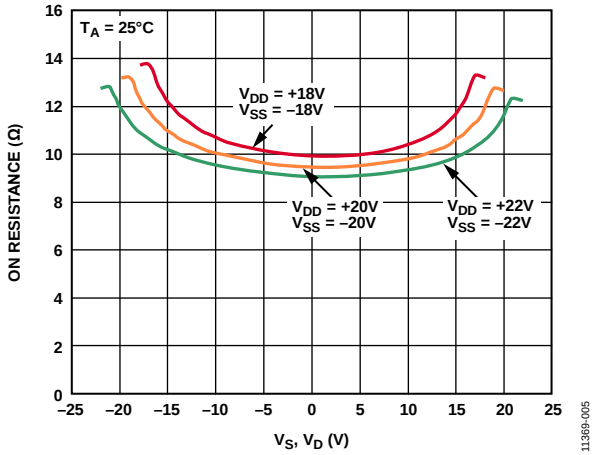

Figure 6. On Resistance as a Function of V_S, V_D (Dual Supply: ±20 V)

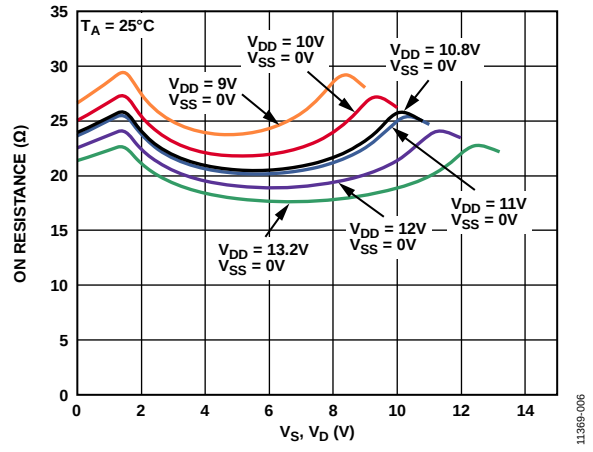

Figure 7. On Resistance as a Function of V_S, V_D (Single Supply: 10 V, 12 V)

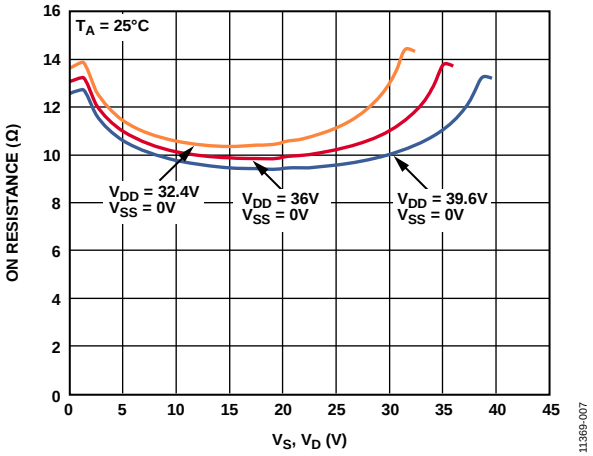

Figure 8. On Resistance as a Function of V_S, V_D (Single Supply: 36 V)

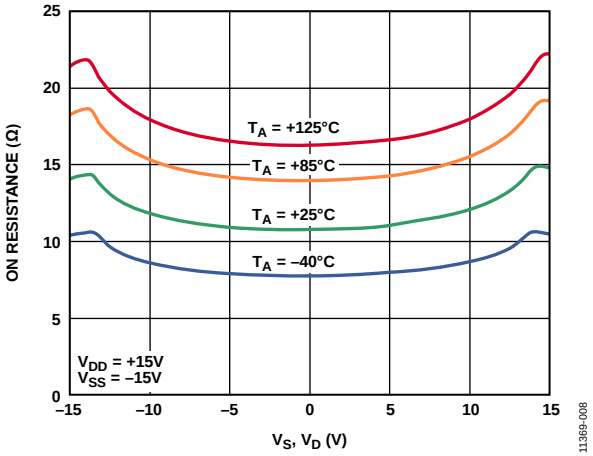

Figure 9. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

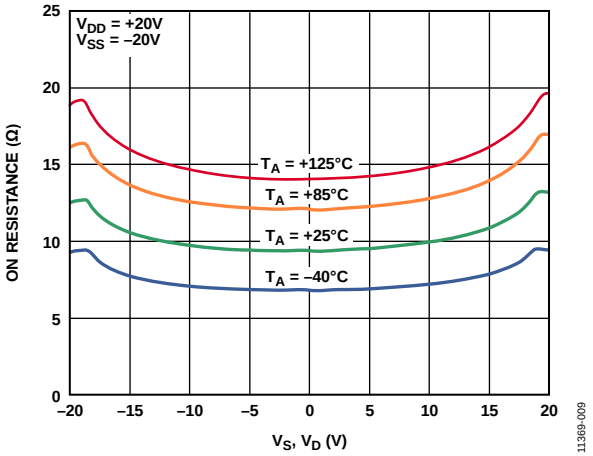

Figure 10. On Resistance as a Function of V_S (V_D) for Different Temperatures, ±20 V Dual Supply

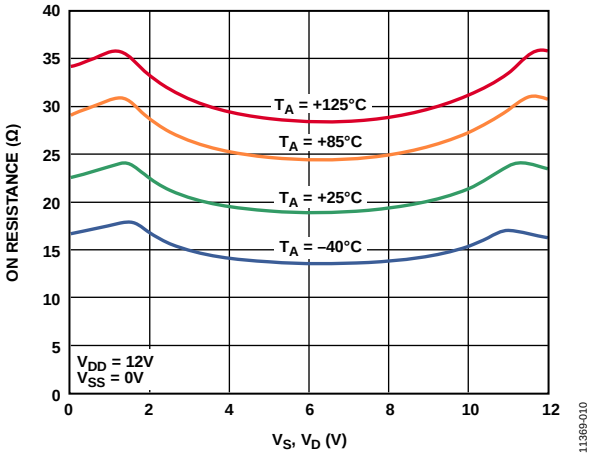

Figure 11. On Resistance as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

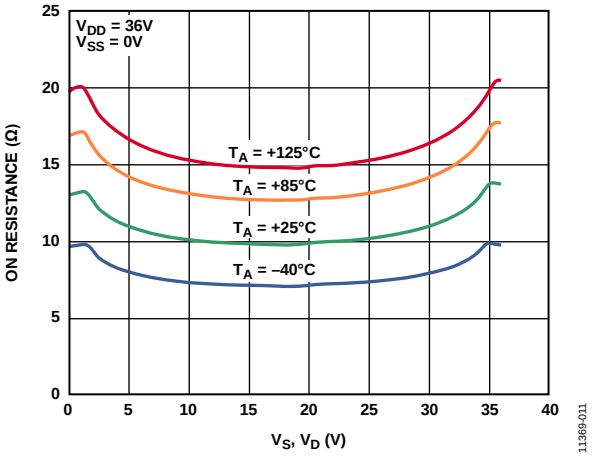

Figure 12. On Resistance as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

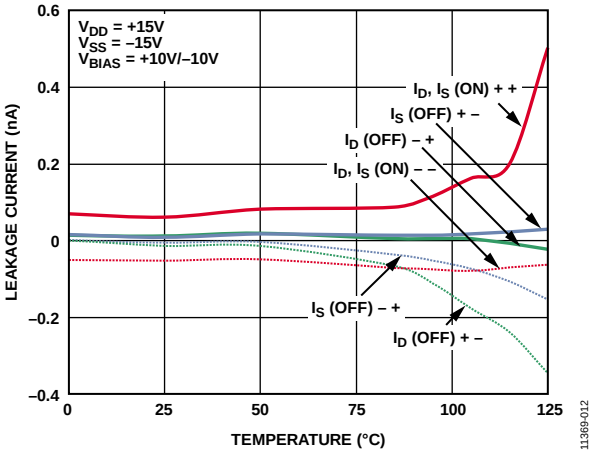

Figure 13. Leakage Currents as a Function of Temperature, ±15 V Dual Supply

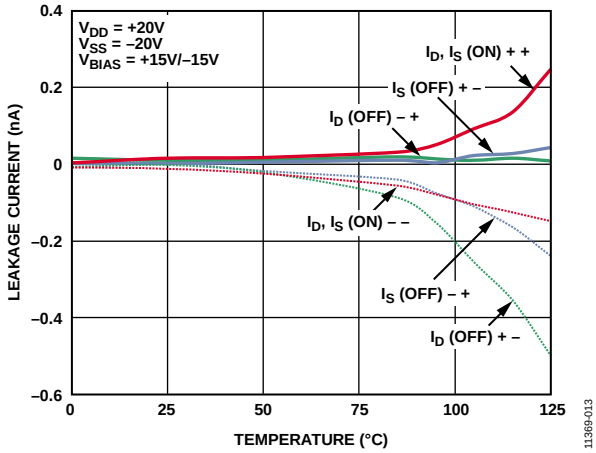

Figure 14. Leakage Currents as a Function of Temperature, ±20 V Dual Supply

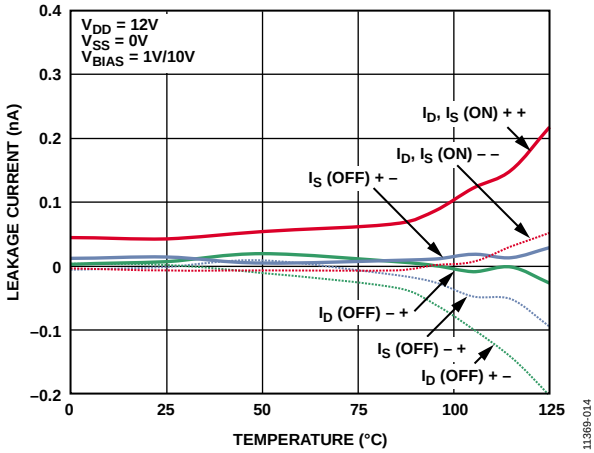

Figure 15. Leakage Currents as a Function of Temperature, 12 V Single Supply

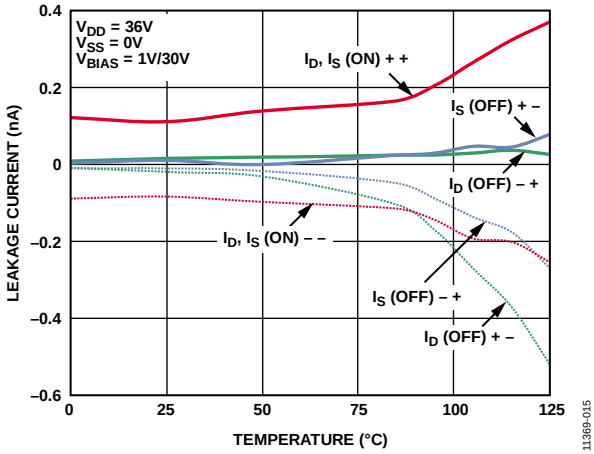

Figure 16. Leakage Currents as a Function of Temperature, 36 V Single Supply

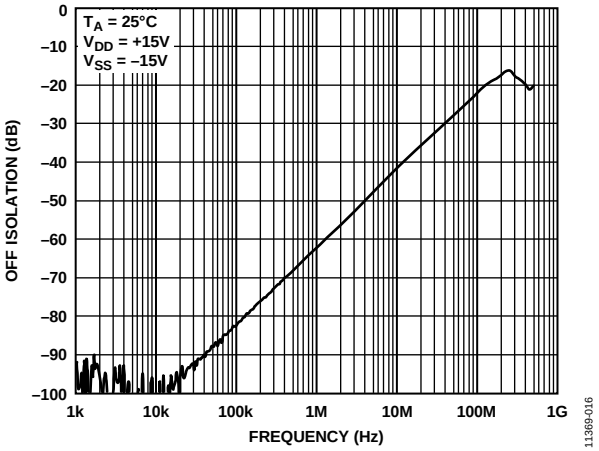

Figure 17. Off Isolation vs. Frequency

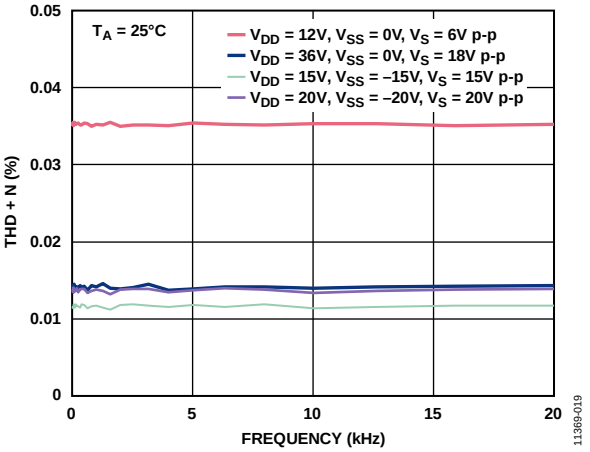

Figure 20. THD + N vs. Frequency

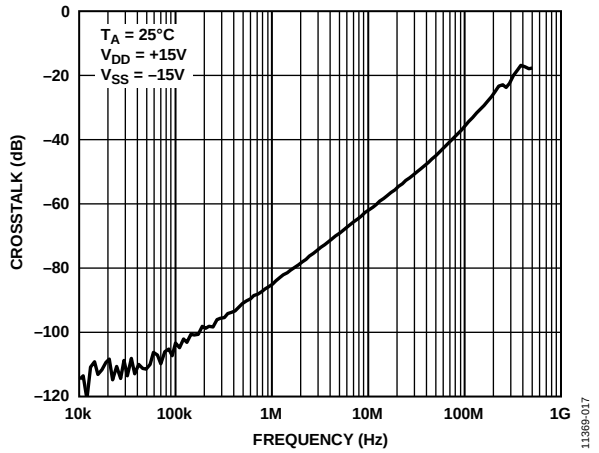

Figure 18. Crosstalk vs. Frequency

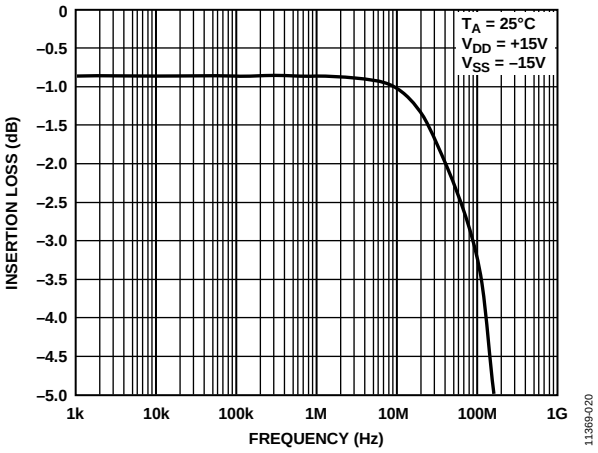

Figure 21. Bandwidth

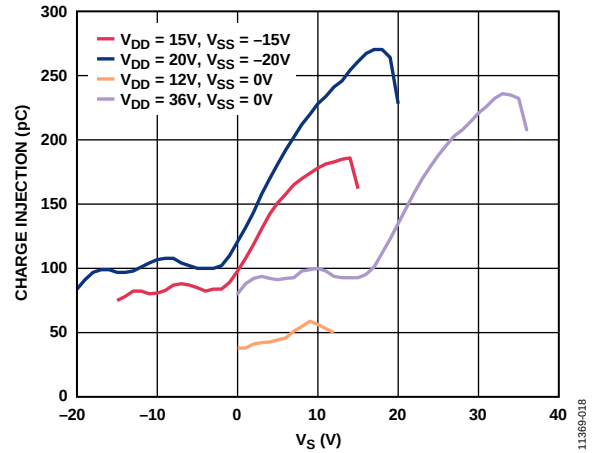

Figure 19. Charge Injection vs. Source Voltage (V_S)

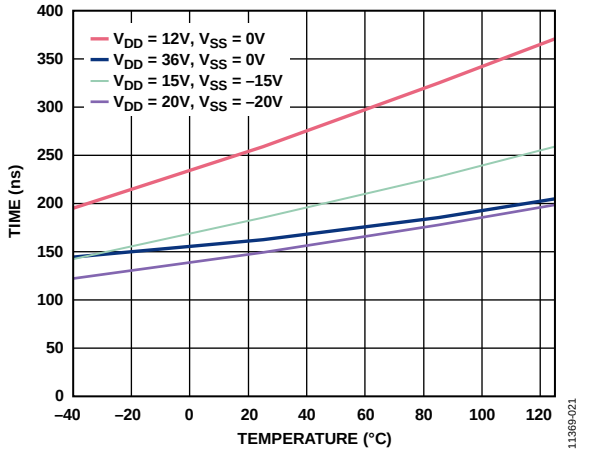

Figure 22. $t_{TRANSITION}$ Times vs. Temperature

TEST CIRCUITS

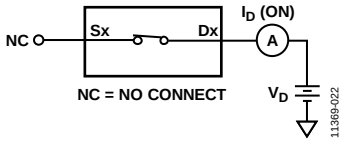

Figure 23. On Leakage

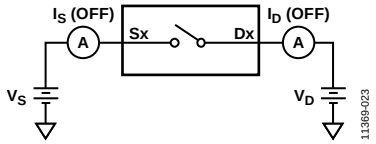

Figure 24. Off Leakage

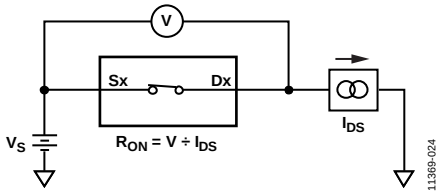

Figure 25. On Resistance

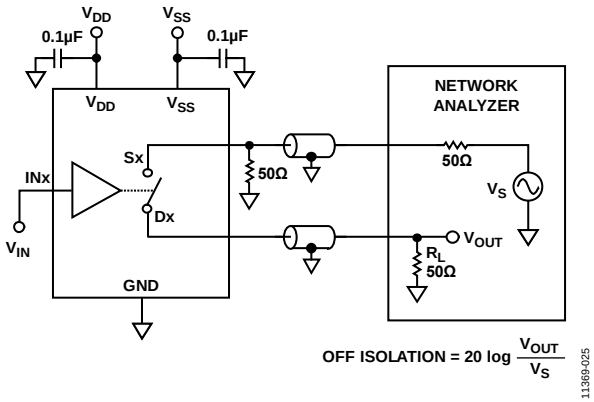

Figure 26. Off Isolation

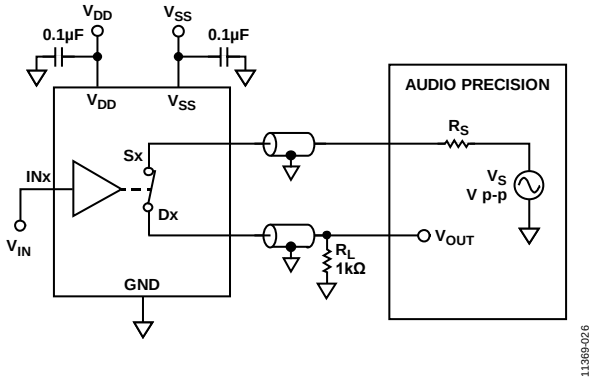

Figure 27. THD + Noise

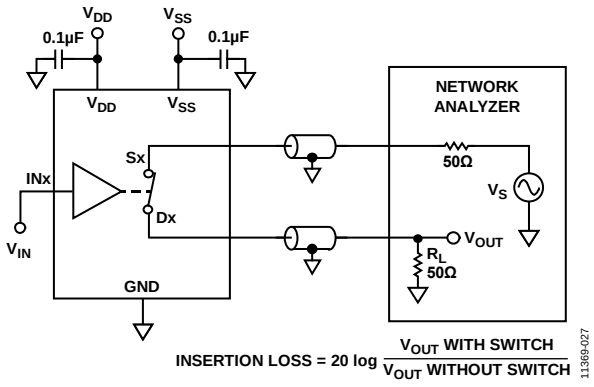

Figure 28. Bandwidth

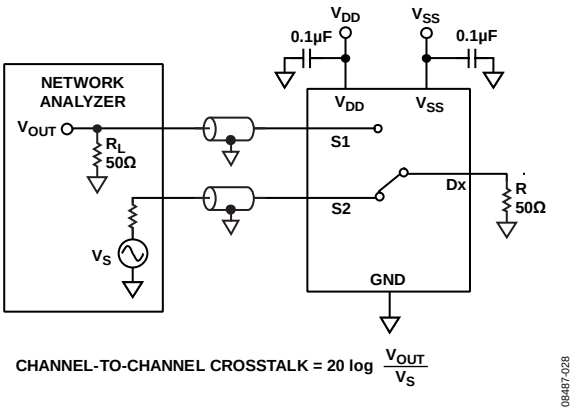

Figure 29. Channel-to-Channel Crosstalk

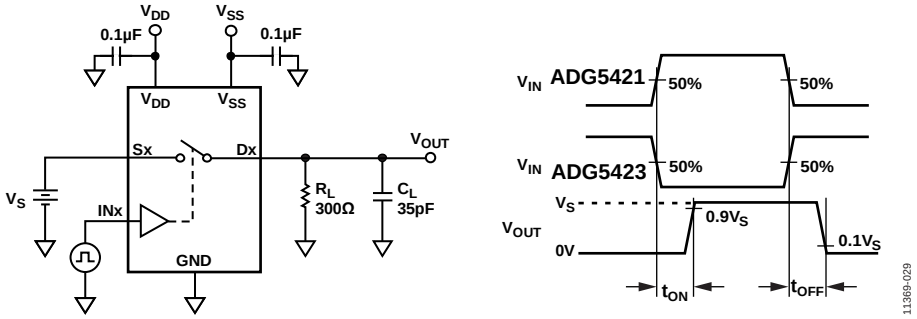

Figure 30. Switching Times, t_{ON} and t_{OFF}

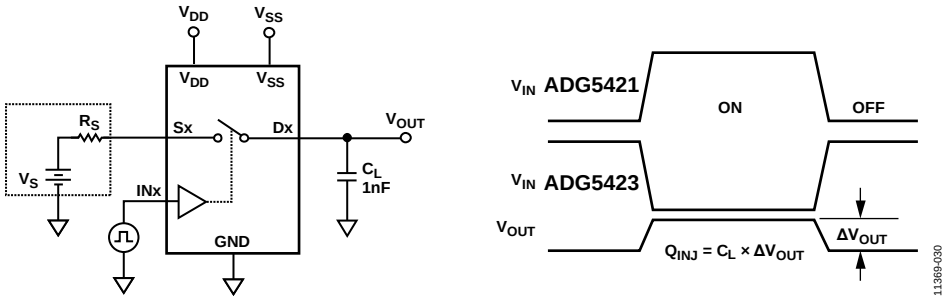

Figure 31. Charge Injection

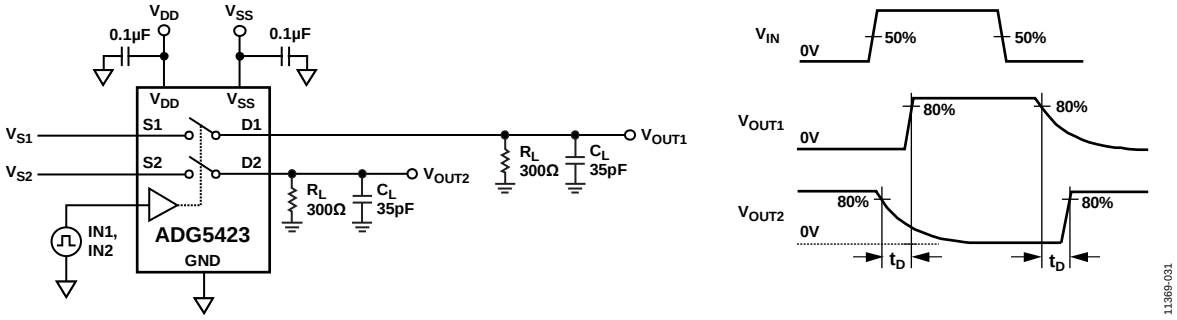

Figure 32. Break-Before-Make Time Delay

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
$R_{FLAT (ON)}$ represents the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} represents digital input capacitance.

t_{ON}
t_{ON} represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}
t_{OFF} represents the delay time between the 50% and 90% points of the digital input and switch off condition.

t_D
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB from its dc level.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

APPLICATIONS INFORMATION

The ADG54xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADG5421/ADG5423 high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V. The ADG5421/ADG5423 (as well as other select devices within this family) achieve an 8 kV human body model ESD rating, which provides a robust solution, eliminating the need for separate protection circuitry designs in some applications.

TRENCH ISOLATION

In the ADG5421/ADG5423, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction-isolated switches, are eliminated, and the result is a completely latch-up immune switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. The two transistors form a silicon-controlled rectifier (SCR) type circuit, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up immune switch.

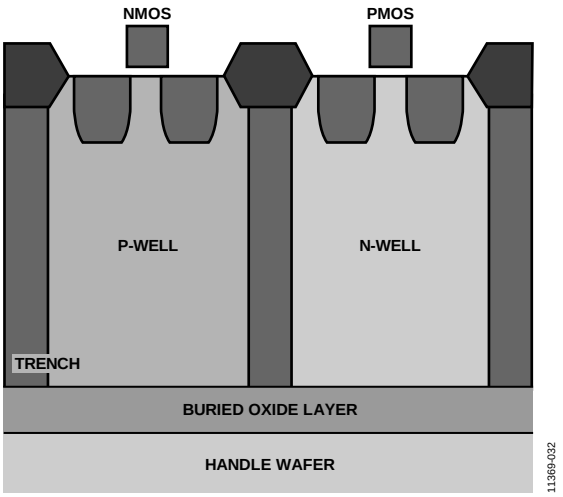

Figure 33. Trench Isolation

OUTLINE DIMENSIONS

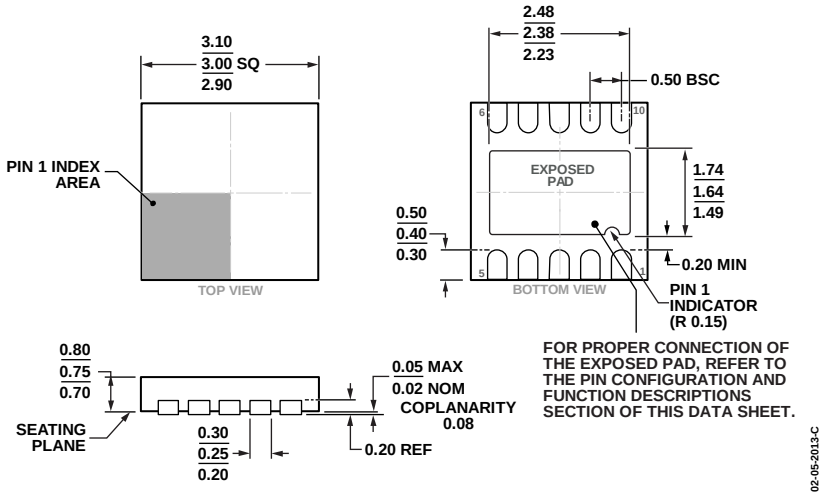

Figure 34. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

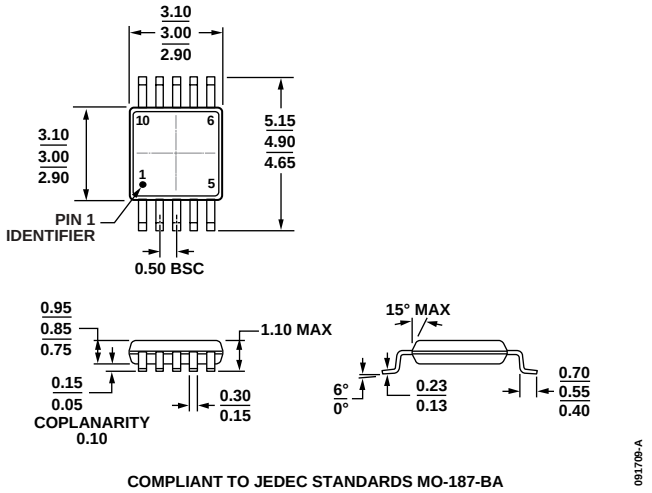

Figure 35. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADG5421BCPZ-RL7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	BN
ADG5421BRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S47
ADG5421BRMZ-RL7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S47
ADG5423BCPZ-RL7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	BM
ADG5423BRMZ	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S3D
ADG5423BRMZ-RL7	−40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S3D

[1] Z = RoHS Compliant Part.