2 CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT

NOVEMBER 2001 REV. 2.0.0

GENERAL DESCRIPTION

The XRT73L02A Dual Channel E3/DS3/STS-1 Transceiver is an improved version of the XRT73L02 and consists of two fully integrated transmitter and receiver line transceivers designed for E3, DS3 or SONET STS-1 applications.

Each channel can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or the SONET STS-1 (51.84 Mbps) rates. Each channel can be configured to operate in a mode/data rate that is independent of the other channel.

In the transmit direction, each channel in the XRT73L02A encodes input data to either B3ZS or HDB3 format and converts the data into the appropriate pulse shapes for transmission over coaxial cable via a 1:1 transformer.

In the receive direction, the XRT73L02A can perform Equalization on incoming signals, perform Clock Recovery, decode data from either B3ZS or HDB3 format, convert the receive data into TTL/CMOS format, check for LOS or LOL conditions and detect and declare the occurrence of Line Code Violations.

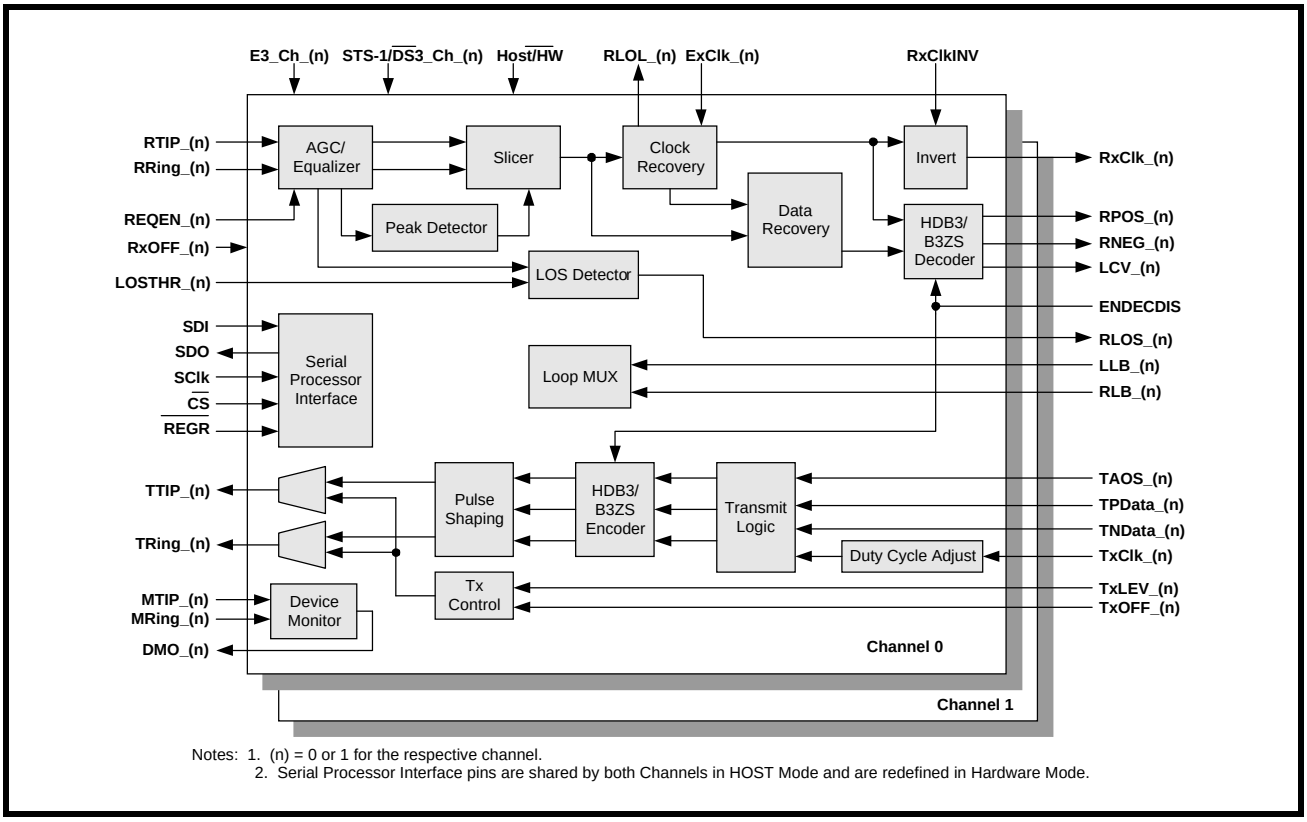
FEATURES

- Incorporates an improved Timing Recovery circuit and is pin and functional compatible to XRT73L02
- Meets E3/DS3/STS-1 Jitter Tolerance Requirements
- Contains a 4-Wire Microprocessor Serial Interface
- Full Loop-back Capability
- Transmit and Receive Power Down Modes
- Full Redundancy Support
- Single +3.3V Power Supply
- Uses Minimum External components
- Operates over -40°C to +85°C Temperature Range
- Available in an 80 pin TQFP package

APPLICATIONS

- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals
- Multiplexers
- ATM Switches

XRT73L02A BLOCK DIAGRAM



Notes: 1. (n) = 0 or 1 for the respective channel.
2. Serial Processor Interface pins are shared by both Channels in HOST Mode and are redefined in Hardware Mode.

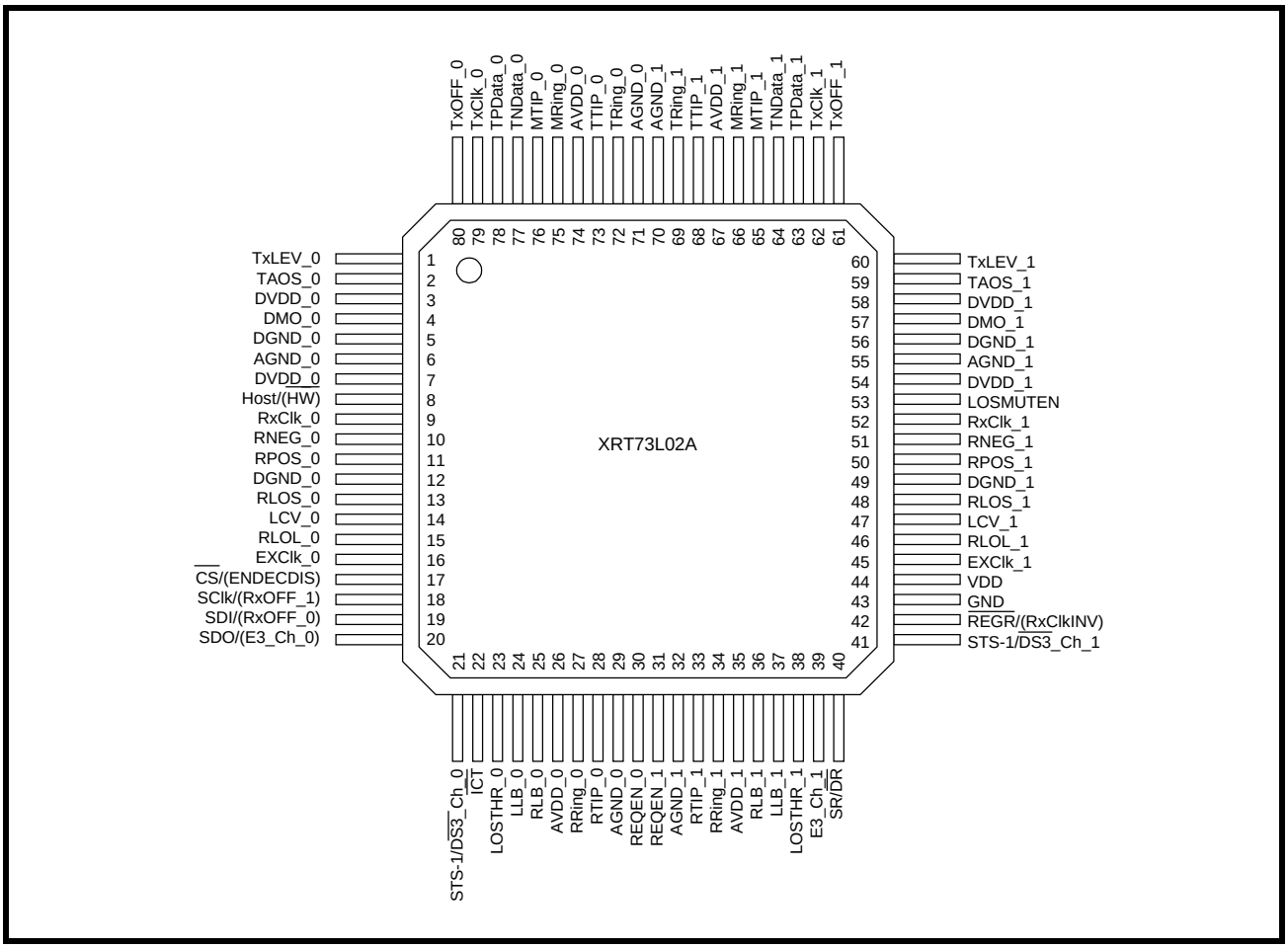
TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Contains Transmit Clock Duty Cycle Correction Circuit on-chip
- Generates pulses that comply with the ITU-T G.703 pulse template (E3 applications)
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (Optional) and Timing Recovery
- Declares and Clears the LOS alarm per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be automatically muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment
- Receiver can be powered down in order to conserve power in redundancy designs

PIN OUT OF THE XRT73L02A



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PIN DESCRIPTIONS

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
1	TxLEV_0	I	**Transmit Line Build-Out Enable/Disable Select - Channel 0:** This input pin is used to enable or disable the Transmit Line Build-Out circuit of Channel 0. Setting this pin to "High" disables the Line Build-Out circuit of Channel 0. In this mode, Channel 0 outputs partially-shaped pulses onto the line via the TTIP_0 and TRing_0 output pins. Setting this pin to "Low" enables the Line Build-Out circuit of Channel 0. In this mode, Channel 0 outputs shaped pulses onto the line via the TTIP_0 and TRing_0 output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set this input pin to "1" if the cable length between the Cross-Connect and the transmit output of Channel 0 is greater than 225 feet. 2. Set this input pin to "0" if the cable length between the Cross-Connect and the transmit output of Channel 0 is less than 225 feet. This pin is active only if the following two conditions are true: a. The XRT73L02A is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT73L02A is configured to operate in the **Hardware Mode**. ***NOTE:*** *If the XRT73L02A is going to be operating in the **Host Mode**, this pin should be tied to GND.*
2	TAOS_0	I	**Transmit All Ones Select - Channel 0:** A “High" on this pin causes the Transmit Section of Channel 0 to generate and transmit a continuous AMI all “1’s" pattern onto the line. The frequency of this "1’s" pattern is determined by TxClk_0. ***NOTES:*** 1. *This input pin is ignored if the XRT73L02A is operating in the **Host Mode**.* 2. *If the XRT73L02A is going to be operating in the **Host Mode**, this pin should be tied to GND.*
3	DVDD_0	****	**Transmit Digital VDD (for Transmitter 0)**
4	DMO_0	O	**Drive Monitor Output - Channel 0:** If no transmitted AMI signal is present on MTIP_0 and MRing_0 input pins for 128±32 TxClk periods, then DMO_0 toggles and remains "High" until the next AMI signal is detected.
5	DGND_0	****	**Transmit Digital GND (for Transmitter 0)**
6	AGND_0		**Analog GND (Substrate Connection) - Channel 0**
7	DVDD_0	****	**Receive Digital VDD (for Receiver 0)**
8	Host/($\overline{HW}$)	I	**Host/Hardware Mode Select:** This input pin is used to enable or disable the Microprocessor Serial Interface (e.g., consisting of the SDI, SDO, SClk, and $\overline{CS}$ pins). Setting this input pin "High" enables the Microprocessor Serial Interface (e.g. configures the XRT73L02A to operate in the **Host Mode**). In this mode, configure the XRT73L02A via the Microprocessor Serial Interface. When the XRT73L02A is operating in the **Host Mode**, it ignores the states of many of the discrete input pins. Setting this input pin "Low" disables the Microprocessor Serial Interface (e.g., configures the XRT73L02A to operate in the **Hardware Mode**). In this mode, many of the external input control pins are functional.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
9	RxClk_0	O	**Receive Clock Output pin - Channel 0:** This output pin is the Recovered Clock signal from the incoming line signal for Channel 0. The receive section of Channel 0 outputs data via the RPOS_0 and RNEG_0 output pins on the rising edge of this clock signal. ***NOTE:*** *The Receive Section of Channel 0 is configured to update the data on the RPOS_0 and RNEG_0 output pins on the falling edge of RxClk_0 by doing one of the following:* **a. Operating in the Hardware Mode** Pull the RClkINV pin to "High". **b. Operating in the Host Mode** Write a "1" into the RClkINV bit-field within the Command Register.
10	RNEG_0	O	**Receive Negative Data Output - Channel 0:** This output pin pulses "High" whenever Channel 0 of the XRT73L02A has received a Negative Polarity pulse in the incoming line signal at the RTIP_0/ RRing_0 inputs. ***NOTE:*** *If the Channel 0 B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are not reflected at this output.*
11	RPOS_0	O	**Receive Positive Pulse Output - Channel 0:** This output pin pulses "High" whenever Channel 0 of the XRT73L02A has received a Positive Polarity pulse in the incoming line signal at the RTIP_0/ RRing_0 inputs. ***NOTE:*** *If the Channel 0 B3ZS/HDB3 Decoder is enabled, the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") are not reflected at this output.*
12	DGND_0	****	**Receive Digital GND - Channel 0**
13	RLOS_0	O	**Receive Loss of Signal Output Indicator - Channel 0:** This output pin toggles "High" if Channel 0 in the XRT73L02A has detected a Loss of Signal Condition in the incoming line signal. The criteria the XRT73L02A uses to declare an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode.
14	LCV_0	O	**Line Code Violation Indicator - Channel 0:** Whenever the Receive Section of Channel 0 detects a Line Code Violation, it pulses this output pin "High". This output pin remains "Low" at all other times. ***NOTE:*** *The XRT73L02A outputs an NRZ pulse via this output pin. It is advisable to sample this output pin via the RxClk_0 clock output signal.*
15	RLOL_0	O	**Receive Loss of Lock Output Indicator - Channel 0:** This output pin toggles "High" if Channel 0 of the XRT73L02A has detected a Loss of Lock Condition. Channel 0 declares an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXClk_(n) input pin) by more than 0.5%.
16	EXClk_0	I	**External Reference Clock Input - Channel 0:** Apply a 34.368 MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications. ***NOTES:*** 1. *It is permissible to use the same clock which is also driving the TxClk input pin.* 2. *It is permissible to operate the two Channels at different data rates.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
17	CS/(ENDECDIS)	I	**Microprocessor Serial Interface - Chip Select Input/Encoder-Decoder Disable Input:** This pin's functionality depends on whether the XRT73L02A is operating in the Host or Hardware Mode. **Host Mode - Chip Select Input** The Local Microprocessor must assert this pin (set it to "0") in order to enable communication with the XRT73L02A via the Microprocessor Serial Interface. ***NOTE:*** *This pin is internally pulled "High".* **Hardware Mode - Encoder/Decoder Disable Input** Setting this input pin "High" disables the B3ZS/HDB3 Encoder & Decoder blocks in the XRT73L02A and configures it to transmit and receive the line signal in an AMI format. Setting this input pin "Low" enables the B3ZS/HDB3 Encoder & Decoder blocks and configures it to transmit and receive the line signal in the B3ZS format for STS-1/DS3 operation or in the HDB3 format for E3 operation. ***NOTE:*** *If the XRT73L02A is operating in the **Hardware Mode**, this pin setting configures the B3ZS/HDB3 Encoder and Decoder Blocks for both Channels.*
18	SClk/(RxOFF_1)	I	**Microprocessor Serial Interface Clock Signal/Channel 1 Receiver Shut OFF Input:** The function of this pin depends on whether the XRT73L02A is operating in the **Host Mode** or in the **Hardware Mode**. **Host Mode** - Microprocessor Serial Interface Clock Signal: This signal is used to sample the data on the SDI pin on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. **Hardware Mode** - Channel 1 Receiver Shut OFF input pin: Setting this input pin "High" shuts off the Channel 1 receiver. Setting this input pin "Low" enables the Receive Section for full operation.
19	SDI/(RxOFF_0)	I	**Serial Data Input for the Microprocessor Serial Interface/Channel 0 - Receiver Shut OFF Input pin:** The function of this input pin depends on whether the XRT73L02A is operating in the **Host Mode** or in the **Hardware Mode**. **Host Mode** - Serial Data Input for the Microprocessor Serial Interface: To read or write data into the Command Registers over the Microprocessor Serial Interface, apply the Read/Write bit, the Address Values of the Command Registers and Data Value to be written during Write Operations to this pin. This input is sampled on the rising edge of the SClk pin. **Hardware Mode** - Channel 0 Receiver Shut OFF Input pin: Setting this input pin "High" shuts off the Channel 0 receiver. Setting this input pin "Low" enables the Receive Section for full operation.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
20	SDO/(E3_Ch_0)	I/O	**Serial Data Output from the Microprocessor Serial Interface/E3_Mode Select - Channel 0:** The function of this pin depends on whether the XRT73L02A is operating in the **Host Mode** or in the **Hardware Mode**. **Host Mode** Operation - Serial Data Output for the Microprocessor Serial Interface: This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SClk input signal and tri-stated upon completion of data transfer. **Hardware Mode** Operation - E3 Mode Select - Channel 0: This input pin is used to configure Channel 0 in the XRT73L02A to operate in the E3 or STS/DS3 Modes. Setting this input pin to "High" configures Channel 0 to operate in the E3 Mode. Setting this input pin to "Low" configures Channel 0 to operate in either the DS3 or STS-1 Modes, depending upon the state of the STS-1/$\overline{\text{DS3}}$_Ch_0 input pin.
21	STS-1/$\overline{\text{DS3}}$_Ch_0	I	**STS-1/DS3 Select Input - Channel 0:** Set this input pint to “High” for STS-1 and “Low” for DS3 Operation. The XRT73L02A ignores this pin if the E3_Ch_0 pin is set to “1". This input pin is ignored if the XRT73L02A is operating in the **Host Mode**. If the XRT73L02A is operating in the **Host Mode**, the pin should be tied to GND.
22	$\overline{\text{ICT}}$	I	**In-Circuit Test Input**: Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, set this pin "High". ***NOTE:*** *This pin is internally pulled “High".*
23	LOSTHR_0	I	**Loss of Signal Threshold Control - Channel 0**: The voltage forced on this pin controls the input loss of signal threshold for Channel 0. Forcing the LOSTHR_0 pin to GND or VDD provides two settings. This pin must be set to the desired level upon power up and should not be changed during operation. ***NOTE:*** *This pin is only applicable during DS3 or STS-1 operations.*
24	LLB_0	I	**Local Loop-back - Channel 0**: This input pin along with RLB_0 dictates the Loop-Back mode in which Channel 0 in the XRT73L02A is operating. A "High" on this pin with RLB_0 set to "Low" configures Channel 0 of the XRT73L02A to operate in the Analog Local Loop-back Mode. A "High" on this pin with RLB_0 set to "High" configures Channel 0 of the XRT73L02A to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the **Host Mode**.*
25	RLB_0	I	**Remote Loop-back - Channel 0:** This input pin along with LLB_0 dictates the Loop-Back mode in which Channel 0 in the XRT73L02A is operating. A "High" on this pin with LLB_0 being set to “Low" configures Channel 0 of the XRT73L02A to operate in the Remote Loop-back Mode. A "High" on this pin with LLB_0 also being set to "High" configures Channel 0 of the XRT73L02A to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the **Host Mode**.*
26	AVDD_0	****	**Receive Analog VDD - Channel 0:**
27	RRing_0	I	**Receive Ring Input - Channel 0:** This input pin along with RTIP_0 is used to receive the bipolar line signal from the Remote DS3/E3 Terminal.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
28	RTIP_0	I	**Receive TIP Input - Channel 0:** This input pin along with RRing_0 is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
29	AGND_0	****	**Receive Analog GND - Channel 0**
30	REQEN_0	I	**Receive Equalization Enable Input - Channel 0:** Setting this input pin "High" enables the Internal Receive Equalizer of Channel 0. Setting this pin "Low" disables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the* ***Host Mode****.*
31	REQEN_1	I	**Receive Equalization Enable Input - Channel 1:** Setting this input pin "High" enables the Internal Receive Equalizer of Channel 1. Setting this pin "Low" disables the Internal Receive Equalizer. The guidelines for enabling and disabling the Receive Equalizer are described in Section 3.2. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the* ***Host Mode****.*
32	AGND_1	****	**Receive Analog GND - Channel 1**
33	RTIP_1	I	**Receive TIP Input - Channel 1:** This input pin along with RRing_1 is used to receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.
34	RRing_1	I	**Receive Ring Input - Channel 1:** This input pin along with RTIP_1 is used to receive the bipolar line signal from the Remote DS3/E3 Terminal.
35	AVDD_1	****	**Receive Analog VDD - Channel 1**
36	RLB_1	I	**Remote Loop-back - Channel 1:** This input pin along with LLB_1 dictates the Loop-Back mode in which Channel 1 in the XRT73L02A is operating. A "High" on this pin with LLB_1 being set to “Low" configures Channel 1 of the XRT73L02A to operate in the Remote Loop-back Mode. A "High" on this pin with LLB_1 also being set to "High" configures Channel 1 of the XRT73L02A to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the* ***Host Mode****.*
37	LLB_1	I	**Local Loop-back - Channel 1**: This input pin along with RLB_1 dictates the Loop-Back mode in which Channel 1 of the XRT73L02A is operating. A "High" on this pin with RLB_1 set to "Low" configures Channel 1 of the XRT73L02A to operate in the Analog Local Loop-back Mode. A "High" on this pin with RLB_1 set to "High" configures Channel 1 of the XRT73L02A to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the* ***Host Mode****.*
38	LOSTHR_1	I	**Loss of Signal Threshold Control - Channel 1**: The voltage forced on this pin controls the input loss of signal threshold for Channel 1. Forcing the LOSTHR_1 pin to GND or VDD provides two settings. This pin must be set to the desired level upon power up and should not be changed during operation. ***NOTE:*** *This pin is only applicable during DS3 or STS-1 operations.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
39	E3_Ch_1	I	**E3 Select Input - Channel 1:** A "High" on this pin configures Channel 1 of the XRT73L02A to operate in the E3 Mode. A "Low" on this pin configures Channel 1 of the XRT73L02A to check the state of the STS-1/$\overline{DS3}$_Ch_1 input pin ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the* ***Host Mode****.*
40	SR/$\overline{DR}$	I	**Receive Output Single-Rail/Dual-Rail Select:** Setting this pin "High" configures the Receive Sections of all Channels to output data in a Single-Rail Mode to the Terminal Equipment. Setting this pin "Low" configures the Receive Section of all Channels to output data in a Dual-Rail Mode to the Terminal Equipment.
41	STS-1/$\overline{DS3}$_Ch_1	I	**STS-1/DS3 Select Input - Channel 1:** Set this pin to “High” for STS-1 and “Low” for DS3 Operation. The XRT73L02A ignores this pin if the E3_Ch_1 pin is set to “1". This input pin is ignored if the XRT73L02A is operating in the **Host Mode**. If the XRT73L02A is operating in the **Host Mode**, the pin should be tied to GND.
42	$\overline{REGR}$/ (RxClkNV)	I	**Register Reset Input pin (Invert RxClk_(n)) Output - Select):** The function of this pin depends upon whether the XRT73L02A is operating in the **Host Mode** or in the **Hardware Mode**. ***NOTE:*** *This pin is internally pulled "High".* In the Host-Mode - Register Reset Input pin: Setting this input pin "Low" causes the XRT73L02A to reset the contents of the Command Registers to their default settings and default operating configuration. In the **Hardware Mode** - Invert RxClk Output Select: Setting this input pin "High" configures the Receive Section of all Channels in the XRT73L02A to invert their RxClk_(n) clock output signals and configures Channel (n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the falling edge of RxClk_(n). Setting this pin "Low" configures Channel (n) to output the recovered data via the RPOS_(n) and RNEG_(n) output pins on the rising edge of RxClk_(n).
43	GND	****	**ExClk Reference GND**
44	VDD	****	**ExClk Reference VDD**
45	EXClk_1	I	**External Reference Clock Input - Channel 1:** Apply a 34.368 MHz clock signal for E3 applications, a 44.736 MHz clock signal for DS3 applications or a 51.84 MHz clock signal for SONET STS-1 applications. The Clock Recovery PLL in Channel 1 uses this signal as a Reference Signal for Declaring and Clearing the Receive Loss of Lock Alarm. ***NOTES:*** 1. *It is permissible to use the same clock which is also driving the TxClk input pin.* 2. *It is permissible to operate the two Channels at different data rates*
46	RLOL_1	O	**Receive Loss of Lock Output Indicator - Channel 1:** This output pin toggles "High" if Channel 1 of the XRT73L02A has detected a Loss of Lock Condition. Channel 1 declares an LOL (Loss of Lock) Condition if the recovered clock frequency deviates from the Reference Clock frequency (available at the EXClk_(n) input pin) by more than 0.5%.

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
47	LCV_1	O	**Line Code Violation Indicator - Channel 1:** Whenever the Receive Section of Channel 1 detects a Line Code Violation, it pulses this output pin "High". This output pin remains "Low" at all other times. ***NOTE:*** *The XRT73L02A outputs an NRZ pulse via this output pin. It is advisable to sample this output pin via the RxClk_1 clock output signal.*
48	RLOS_1	O	**Receive Loss of Signal Output Indicator - Channel 1:** This output pin toggles "High" if Channel 1 in the XRT73L02A has detected a Loss of Signal Condition in the incoming line signal. The criteria the XRT73L02A uses to declare an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode.
49	DGND_1	****	**Receive Digital Ground - Channel 1**
50	RPOS_1	O	**Receive Positive Data Output - Channel 1:** This output pin pulses “High" whenever Channel 1 of the XRT73L02A has received a Positive Polarity pulse in the incoming line signal at the RTIP_1/ RRing_1 inputs. ***NOTE:*** *If the Channel 1 B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
51	RNEG_1	O	**Receive Negative Data Output - Channel 1:** This output pin pulses "High" whenever Channel 1 of the XRT73L02A has received a Negative Polarity pulse in the incoming line signal at the RTIP_1/ RRing_1 inputs. ***NOTE:*** *If the Channel 1 B3ZS/HDB3 Decoder is enabled, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is not reflected at this output.*
52	RxClk_1	O	**Receive Clock Output pin - Channel 1:** This output pin is the Recovered Clock signal from the incoming line signal for Channel 1. The receive section of Channel 1 outputs data via the RPOS_1 and RNEG_1 output pins on the rising edge of this clock signal. ***NOTE:*** *The Receive Section of Channel 1 is configured to update the data on the RPOS_1 and RNEG_1 output pins on the falling edge of RxClk_1 by doing one of the following:* **a. Operating in the Hardware Mode** Pull the RxClkINV pin to "High". **b. Operating in the Host Mode** Write a "1" into the RxClkINV bit-field of the Command Register.
53	LOSMUTEN	I	**MUTE-upon-LOS Enable Input (Hardware Mode):** This input pin is used to configure the XRT73L02A while it is operating in the **Hardware Mode** to Mute the recovered data via the RPOS_(n), RNEG_(n) output pins whenever one of the Channels declares an LOS condition. Setting this input pin "High" configures all Channels to automatically pull the RPOS_(n) and RNEG_(n) output pins to GND whenever it is declaring an LOS condition, Muting the data being output to the Terminal Equipment. Setting this input pin "Low" configures all Channels to NOT automatically Mute the recovered data whenever an LOS condition is declared. ***NOTES:*** 1. *This input pin is ignored and should be connected to GND if the XRT73L02A is operating in the **Host Mode**.* 2. *This pin is internally pulled "High".*
54	DVDD_1	****	**Receive Digital VDD - Channel 1**

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
55	AGND_1	****	**Analog Ground (Substrate Connection) - Channel 1**
56	DGND_1	****	**Transmit Digital GND - Channel 1**
57	DMO_1	O	**Drive Monitor Output - Channel 1:** If no transmitted AMI signal is present on MTIP_1 and MRing_1 input pins for 128±32 TxClk periods, then DMO_1 toggles and remains "High" until the next AMI signal is detected.
58	DVDD_1	****	**Transmit Digital VDD - Channel 1**
59	TAOS_1	I	**Transmit All Ones Select - Channel 1:** A "High" on this pin causes the Transmit Section of Channel 1 to generate and transmit a continuous AMI all "1's" pattern onto the line. The frequency of this "1's" pattern is determined by TxClk_1. ***NOTES:*** 1. *This input pin is ignored if the XRT73L02A is operating in the **Host Mode**.* 2. *If the XRT73L02A is going to be operating in the **Host Mode**, this pin should be tied to GND.*
60	TxLEV_1	I	**Transmit Line Build-Out Enable/Disable Select - Channel 1:** This input pin is used to enable or disable the Transmit Line Build-Out circuit of Channel 1. Setting this pin to "High" disables the Line Build-Out circuit of Channel 1. In this mode, Channel 1 outputs partially-shaped pulses onto the line via the TTIP_1 and TRing_1 output pins. Setting this pin to "Low" enables the Line Build-Out circuit of Channel 1. In this mode, Channel 1 outputs shaped pulses onto the line via the TTIP_1 and TRing_1 output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set this input pin to "1" if the cable length between the Cross-Connect and the transmit output of Channel 1 is greater than 225 feet. 2. Set this input pin to "0" if the cable length between the Cross-Connect and the transmit output of Channel 1 is less than 225 feet. This pin is active only if the following two conditions are true: a. The XRT73L02A is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT73L02A is configured to operate in the **Hardware Mode**. ***NOTE:*** *If the XRT73L02A is going to be operating in the **Host Mode**, this pin should be tied to GND.*
61	TxOFF_1	I	**Transmitter OFF Input - Channel 1:** Setting this input pin "High" configures the XRT73L02A to turn off the Transmit Section of Channel 1. In this mode, the TTIP_1 and TRing_1 outputs is tri-stated. ***NOTES:*** 1. *This input pin controls the TTIP_1 and TRing_1 outputs even when the XRT73L02A is operating in the **Host Mode**.* 2. *For **Host Mode** Operation, tie this pin to GND if the Transmitter is intended to be turned off via the Microprocessor Serial Interface.*

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
62	TxClk_1	I	**Transmit Clock Input for TPData and TNData - Channel 1:** This input pin must be driven at 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications or 51.84 MHz for SONET STS-1 applications. The XRT73L02A uses this signal to sample the TPData_1 and TNData_1 input pins. By default, the XRT73L02A is configured to sample these two pins on the falling edge of this signal. If operating in the **Host Mode**, the XRT73L02A can be configured to sample the TPData_1 and TNData_1 input pins on either the rising or falling edge of TxClk_1.
63	TPData_1	I	**Transmit Positive Data Input - Channel 1**: The XRT73L02A samples this pin on the falling edge of TxClk_1. If it samples a "1", then it generates and transmits a positive polarity pulse to the line. ***NOTES:*** *1. The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If operating in the **Host Mode**, the XRT73L02A can be configured to sample the TPData_1 pin on either the rising or falling edge of TxClk_1.*
64	TNData_1	I	**Transmit Negative Data Input - Channel 1:** The XRT73L02A samples this pin on the falling edge of TxClk_1. If it samples a "1", then it generates and transmits a negative polarity pulse to the line. ***NOTES:*** *1. This input pin is ignored and tied to GND if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* *2. If operating in the **Host Mode**, the XRT73L02A can be configured to sample the TNData_1 pin on either the rising or falling edge of TxClk_1.*
65	MTIP_1	I	**Monitor Tip Input - Channel 1:** The bipolar line output signal from TTIP_1 is connected to this pin via a 270-ohm resistor to check for line driver failure. This pin is internally pulled "High".
66	MRing_1	I	**Monitor Ring Input - Channel 1:** The bipolar line output signal from TRing_1 is connected to this pin via a 270-ohm resistor to check for line driver failure. This pin is internally pulled "High".
67	AVDD_1	****	**Transmit Analog VDD - Channel 1:**
68	TTIP_1	O	**Transmit TTIP Output - Channel 1:** The XRT73L02A uses this pin with TRing_1 to transmit a bipolar line signal via a 1:1 transformer.
69	TRing_1	O	**Transmit Ring Output - Channel 1:** The XRT73L02A uses this pin with TTIP_1 to transmit a bipolar line signal via a 1:1 transformer.
70	AGND_1	****	**Transmit Analog GND - Channel 1**
71	AGND_0	****	**Transmit Analog GND - Channel 0**
72	TRing_0	O	**Transmit Ring Output - Channel 0:** The XRT73L02A uses this pin with TTIP_0 to transmit a bipolar line signal via a 1:1 transformer.
73	TTIP_0	O	**Transmit TTIP Output - Channel 0:** The XRT73L02A uses this pin with TRing_0 to transmit a bipolar line signal via a 1:1 transformer.
74	AVDD_0	****	**Transmit Analog VDD - Channel 0**

PIN DESCRIPTION

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
75	MRing_0	I	**Monitor Ring Input - Channel 0:** The bipolar line output signal from TRing_0 is connected to this pin via a 270-ohm resistor to check for line driver failure. This pin is internally pulled "High".
76	MTIP_0	I	**Monitor Tip Input - Channel 0:** The bipolar line output signal from TTIP_0 is connected to this pin via a 270-ohm resistor to check for line driver failure. This pin is internally pulled "High".
77	TNData_0	I	**Transmit Negative Data Input - Channel 0:** The XRT73L02A samples this pin on the falling edge of TxClk_0. If it samples a "1", then it generates and transmits a negative polarity pulse to the line. ***NOTES:*** 1. *This input pin is ignored and tied to GND if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* 2. *If operating in the **Host Mode**, it can be configured to sample the TNData_0 pin on either the rising or falling edge of TxClk_0.*
78	TPData_0	I	**Transmit Positive Data Input - Channel 0**: The XRT73L02A samples this pin on the falling edge of TxClk_0. If it samples a "1", then it generates and transmits a positive polarity pulse to the line. ***NOTES:*** 1. *The data should be applied to this input pin if the Transmit Section is configured to accept Single-Rail data from the Terminal Equipment.* 2. *If the XRT73L02A is operating in the **Host Mode** it can be configured to sample the TPData_0 pin on either the rising or falling edge of TxClk_0.*
79	TxClk_0	I	**Transmit Clock Input for TPData and TNData - Channel 0:** This input pin must be driven at 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications or 51.84 MHz for SONET STS-1 applications. The XRT73L02A uses this signal to sample the TPData_0 and TNData_0 input pins. By default, the XRT73L02A is configured to sample these two pins on the falling edge of this signal. If operating in the **Host Mode**, the XRT73L02A can be configured to sample the TPData_0 and TNData_0 input pins on either the rising or falling edge of TxClk_0.
80	TxOFF_0	I	**Transmitter OFF Input - Channel 0:** Setting this input pin "High" configures the XRT73L02A to turn off the Transmit Section of Channel 0. In this mode, the TTIP_0 and TRing_0 outputs is tri-stated. ***NOTES:*** 1. *This input pin controls the TTIP_0 and TRing_0 outputs even when the XRT73L02A is operating in the **Host Mode**.* 2. *For **Host Mode** Operation, tie this pin to GND if the Transmitter is intended to be turned off via the Microprocessor Serial Interface.*

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	- 65°C to + 150°C
Operating Temperature	- 40°C to + 85°C
Supply Voltage Range	-0.5V to +6.0V
Theta-JA	23° C/W
Theta-JC	5.32° C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DC Electrical Characteristics					
V_{DDD}	DC Supply Voltage (Digital)	3.135	3.3	3.465	V
V_{DDA}	DC Supply Voltage (Analog)	3.135	3.3	3.465	V
I_{CC}	Supply Current (Measured while Transmitting and Receiving all "1's")			310	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, IOUT = -4.0mA	0		0.4	V
V_{OH}	Output High Voltage, IOUT = 4.0mA	2.8			V
I_L	Input Leakage Current*			±10	µA

NOTE: ** Not applicable to pins with pull-down resistors.*

ELECTRICAL CHARACTERISTICS (CONTINUED) (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

AC ELECTRICAL CHARACTERISTICS (SEE *f*IGURE 1)

TERMINAL SIDE TIMING PARAMETERS (SEE *f*IGURE 2 AND *f*IGURE 3)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
	TxClk_(n) Clock Duty Cycle (DS3/STS-1)	30	50	70	%
	TxClk_(n) Clock Duty Cycle (E3)	30	50	70	%
	TxClk_(n) Frequency (SONET STS-1)		51.84		MHz
	TxClk_(n) Frequency (DS3)		44.736		MHz
	TxClk_(n) Frequency (E3)		34.368		MHz
t_{RTX}	TxClk_(n) Clock Rise Time (10% to 90%)		3.0	5.0	ns
t_{FTX}	TxClk_(n) Clock Fall Time (90% to 10%)		3.0	5.0	ns
t_{TSU}	TPData/TNData to TxClk_(n) Falling Set up time	3.0	1.5		ns
t_{THO}	TPData/TNData to TxClk_(n) Falling Hold time	3.0	1.5		ns
t_{LCVO}	RxClk_(n) to rising edge of LCV_(n) output delay		2.5		ns
t_{TDY}	TTIP_(n)/TRing_(n) to TxClk_(n) Rising Propagation Delay time		8.0		ns
	RxClk_(n), RxClk_(n)Clock Duty Cycle		50		%
	RxClk_(n), RxClk_(n) Frequency (SONET STS-1)		51.84		MHz
	RxClk_(n), RxClk_(n) Frequency (DS3)		44.736		MHz
	RxClk_(n), RxClk_(n) Frequency (E3)		34.368		MHz
t_{CO}	RxClk_(n) to RPOS_(n)/RNEG_(n) Delay Time		2.5		ns
t_{RRX}	RxClk_(n), RxClk_(n) Clock Rise Time (10% to 90%)		1.5		ns
t_{FRX}	RxClk_(n), RxClk_(n) Clock Fall Time (10% to 90%)		1.5		ns
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

FIGURE 1. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES (TYPICAL CHANNEL SHOWN)

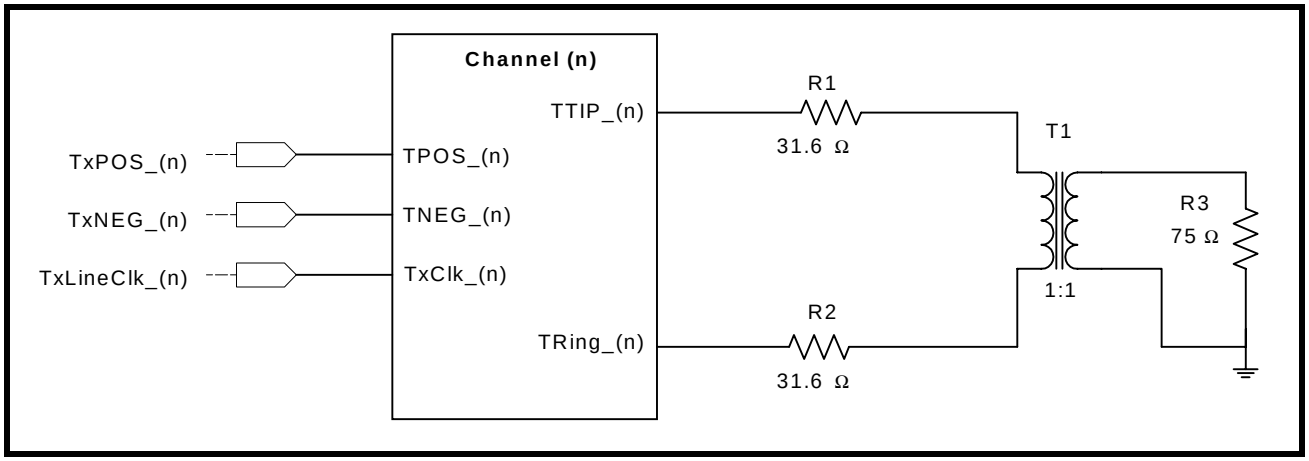


FIGURE 2. TIMING DIAGRAM OF THE TRANSMIT TERMINAL INPUT INTERFACE

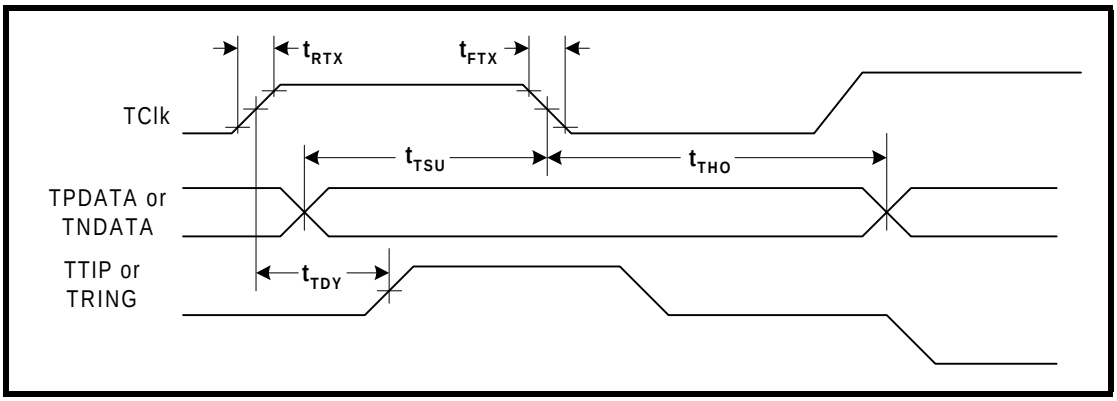
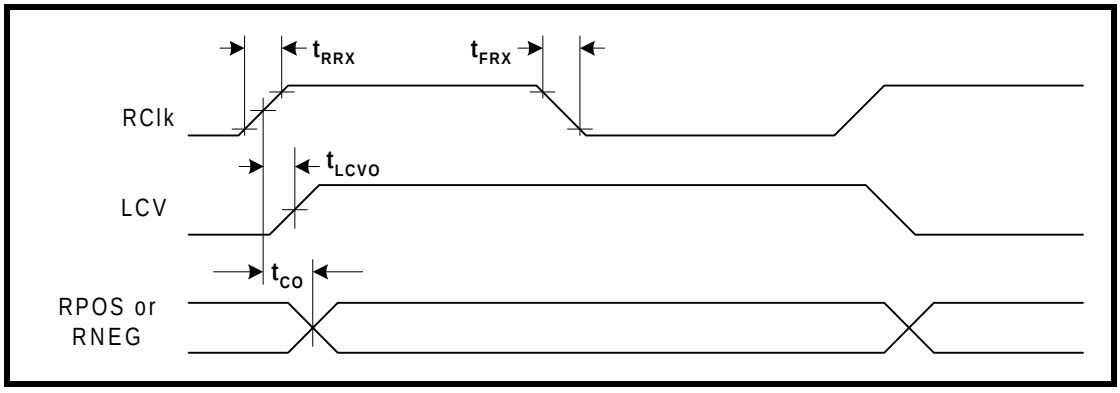


FIGURE 3. TIMING DIAGRAM OF THE RECEIVE TERMINAL OUTPUT INTERFACE



ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS E3 APPLICATION					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
TRANSMIT CHARACTERISTICS (SEE *FIGURE* 1)					
	Transmit Output Pulse Amplitude (Measured at Secondary Output of Transformer)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
	Transmit Output Pulse Width	12.5	14.55	16.5	ns
	Transmit Output Pulse Width Ratio	0.95	1.00	1.05	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UIpp
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	1200	1400		feet
	Interference Margin	-20	-15		dB
	Signal Level to Declare Loss of Signal			-35	dB
	Signal Level to Clear Loss of Signal	-15			dB
	Occurrence of LOS to LOS Declaration Time	10		255	UI
	Termination of LOS to LOS Clearance Time	10		255	UI
	Intrinsic Jitter (all “1’s” Pattern)		0.01		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	30			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	4			UI
	Jitter Tolerance @ Jitter Frequency = 800kHz	0.15	0.20		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3V ± 5%, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS SONET STS-1 APPLICATION					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
Transmit Characteristics (See *f*igure 1)					
	Transmit Output Pulse Amplitude (Measured with TxLEV=0)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured with TxLEV=1)	0.93	0.98	1.08	Vpk
	Transmit Output Pulse Width	8.6	9.65	10.6	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UI
Receive Line Characteristics					
	Receive Sensitivity (Length of cable)	900	1100		feet
	Signal Level to Declare or Clear Loss of Signal (See Table 5)				mV
	Intrinsic Jitter (all “1’s” Pattern)		0.03		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 400kHz	0.15	0.35		UI

ELECTRICAL CHARACTERISTICS (CONTINUED), ($T_A = 25^0C$, $V_{DD} = 3.3V \pm 5\%$, UNLESS OTHERWISE SPECIFIED)

LINE SIDE PARAMETERS DS3 APPLICATION					
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX**	**UNITS**
TRANSMIT CHARACTERISTICS (SEE *f*IGURE 1)					
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=0)	0.68	0.75	0.85	Vpk
	Transmit Output Pulse Amplitude (Measured at 0 feet, TxLEV=1)	0.9	1.0	1.1	Vpk
	Transmit Output Pulse Width	10.10	11.18	12.28	ns
	Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
	Transmit Output Jitter with jitter-free input @ TxClk_(n)		0.02	0.05	UI
Receive Line Characteristics					
	Receive Sensitivity (Length of Cable)	900	1100		feet
	Receive Intrinsic Jitter (all “1’s” Pattern)		0.01		UI
	Receive Intrinsic Jitter (Using PRBS 2^{23-1} Pattern)		0.02		UI
	Signal Level to Declare or clear Loss of Signal (see Table 5)				mV
	Intrinsic Jitter (all “1’s” Pattern)		0.01		UI
	Jitter Tolerance @ Jitter Frequency = 100Hz	64			UI
	Jitter Tolerance @ Jitter Frequency = 1kHz	64			UI
	Jitter Tolerance @ Jitter Frequency = 10kHz	5			UI
	Jitter Tolerance @ Jitter Frequency = 300kHz -- (Cat II)	0.35	0.45		UI

figure 4, figure 5 and figure 6 present the Pulse Template requirements for the E3, DS3 and STS-1 Rates.

FIGURE 4. ITU-T G.703 TRANSMIT OUTPUT PULSE TEMPLATE FOR E3 APPLICATIONS

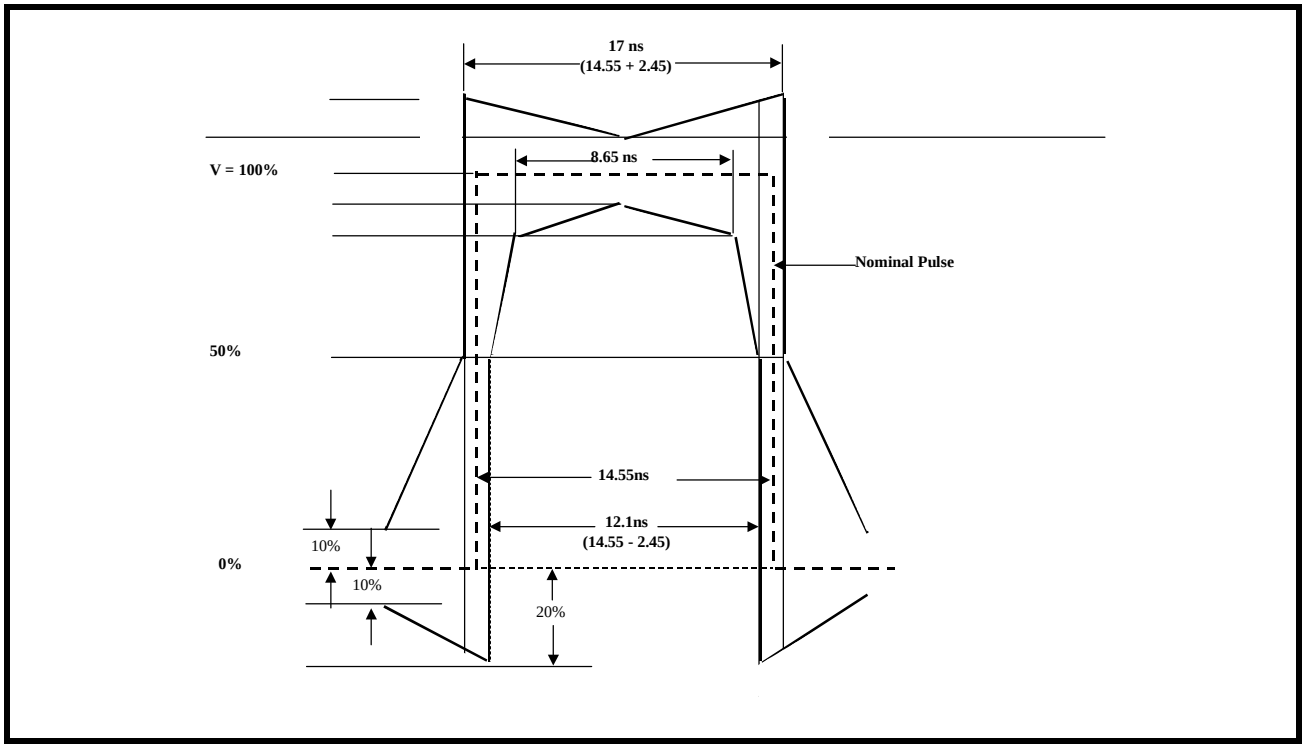


FIGURE 5. BELLCORE GR-499-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR DS3 APPLICATIONS

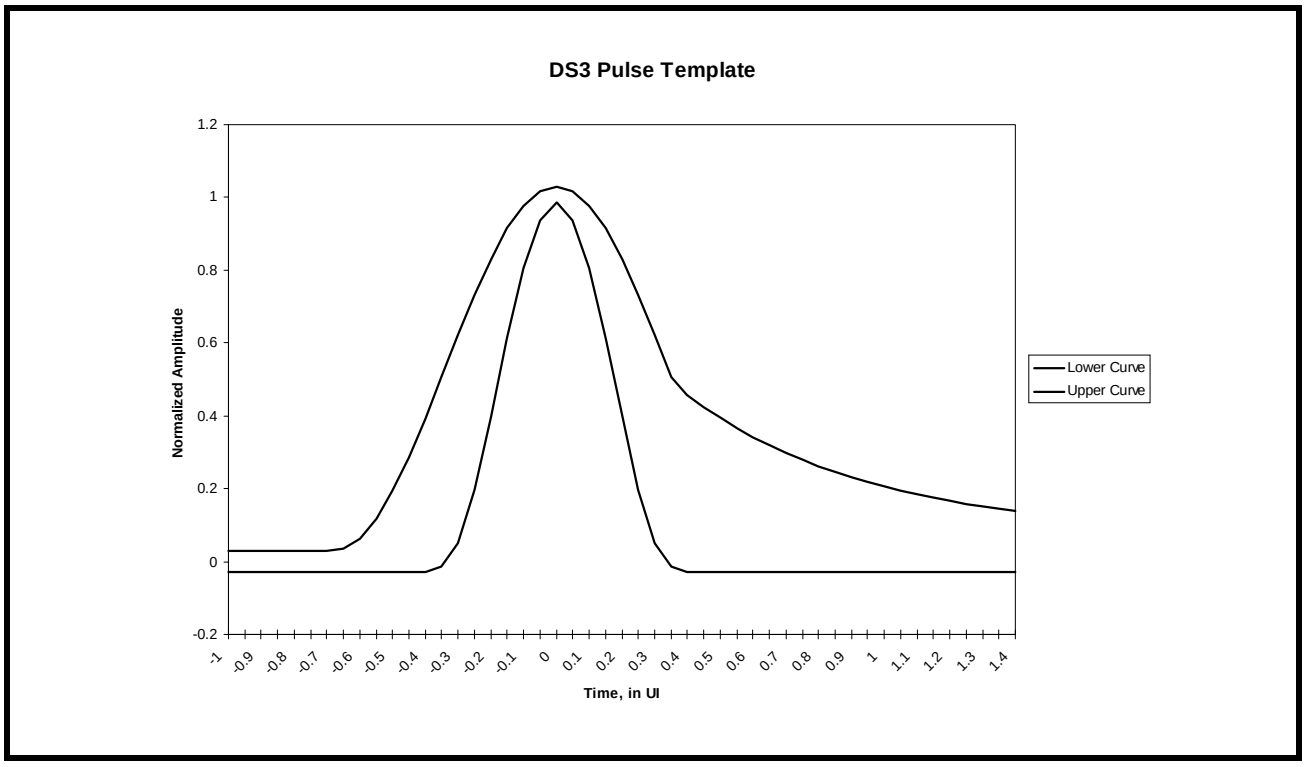


FIGURE 6. BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

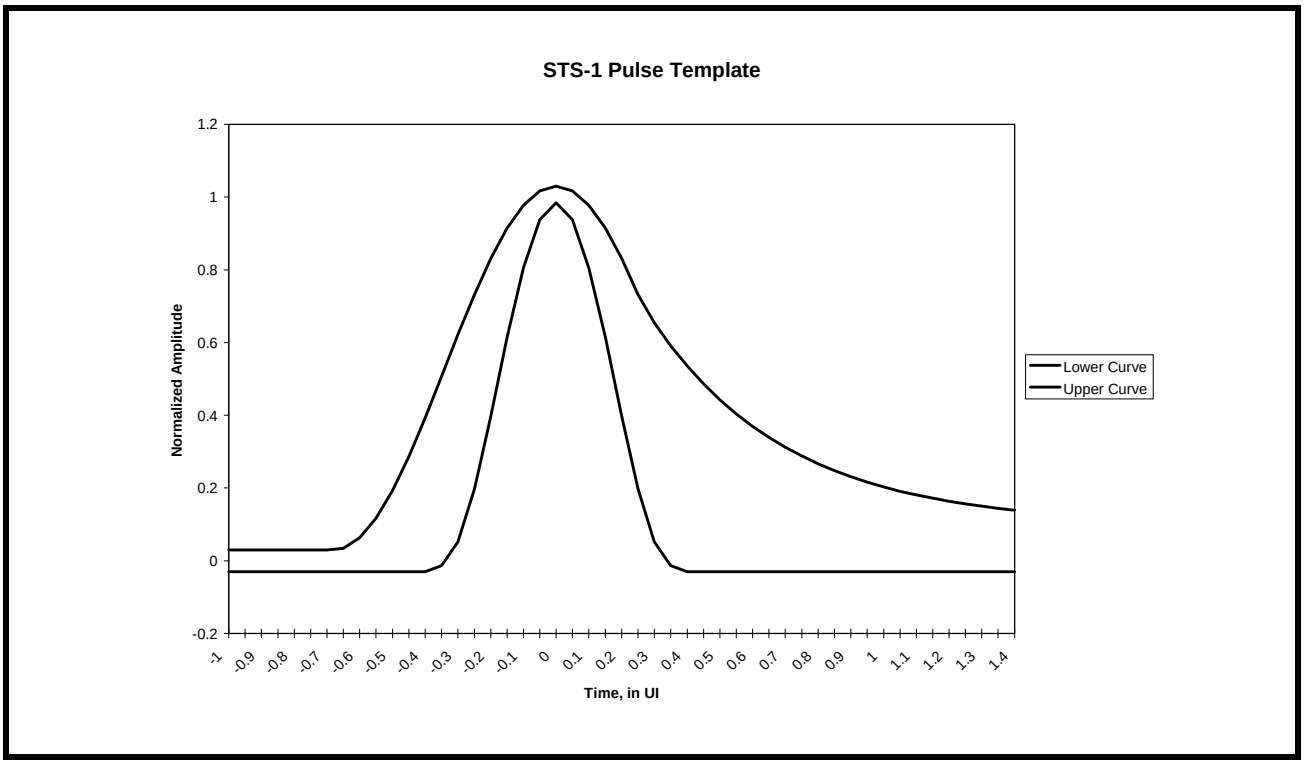
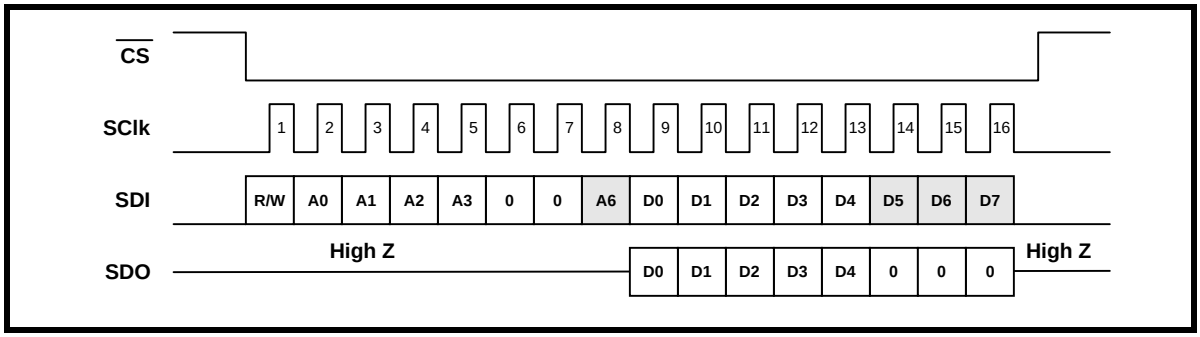


FIGURE 7. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE



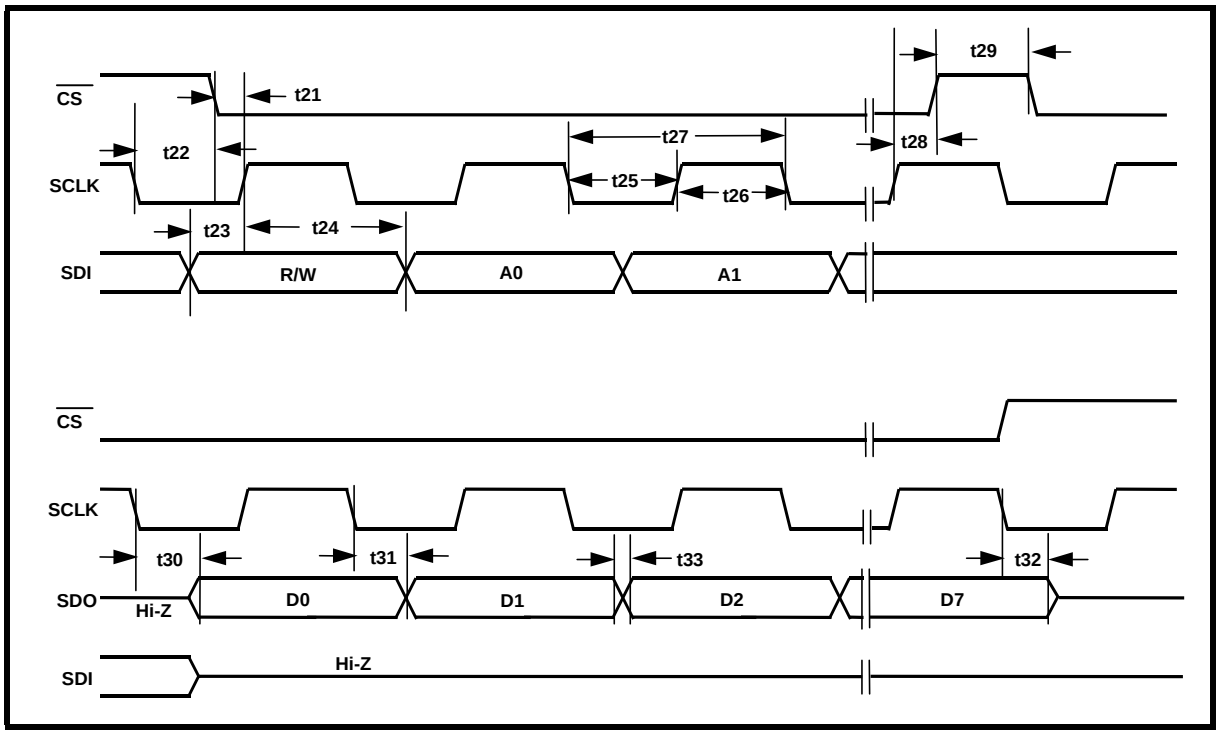
NOTES:

1. *A4 and A5 are always "0".*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*
4. *A shaded pulse, denotes a “don’t care” value.*

ELECTRICAL CHARACTERISTICS (CONTINUED), (T_A = 25°C, V_{DD} = 3.3 ± 5%, UNLESS OTHERWISE SPECIFIED)

MICROPROCESSOR SERIAL INTERFACE TIMING (SEE *f*IGURE 8)					
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk Setup Time	5			ns
t_{22}	$\overline{CS}$ High to Rising Edge of SClk Hold Time	5			ns
t_{23}	SDI to Rising Edge of SClk Setup Time	5			ns
t_{24}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{25}	SClk "Low" Time	65	80		ns
t_{26}	SClk "High" Time	65	80		ns
t_{27}	SClk Period	160			ns
t_{28}	$\overline{CS}$ Low to Rising Edge of SClk Hold Time	5			ns
t_{29}	$\overline{CS}$ "Inactive" Time	160			ns
t_{30}	Falling Edge of SClk to SDO Valid Time			80	ns
t_{31}	Falling Edge of SClk to SDO Invalid Time			65	ns
t_{32}	Falling Edge of SClk, or rising edge of $\overline{CS}$ to High Z		100		ns
t_{33}	Rise/Fall time of SDO Output			20	ns

FIGURE 8. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE



SYSTEM DESCRIPTION

A functional block diagram of the XRT73L02A E3/DS3/STS-1 Transceiver IC is presented in Figure 9. The XRT73L02A contains three independent transmitter and receiver sections and a common microprocessor interface section.

THE TRANSMIT SECTION - CHANNELS 0 AND 1

The Transmit Section of each Channel accepts TTL/CMOS level signals from the Terminal Equipment in either a Single-Rail or Dual-Rail format. The Transmit Section takes this data and does the following:

- Encode this data into the B3ZS format if the DS3 or SONET STS-1 Modes have been selected, or into the HDB3 format if the E3 Mode has been selected.
- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements.
- Drive these pulses onto the line via the TTIP_(n) and TRing_(n) output pins across a 1:1 Transformer.

NOTE: *The Transmit Section drives a "1" (or a Mark) onto the line by driving either a positive or negative polarity pulse across the 1:1 Transformer in a given bit period. The Transmit Section drives a "0" (or a Space) onto the line by driving no pulse onto the line.*

THE RECEIVE SECTION - CHANNELS 0 AND 1

The Receive Section of each Channel receives a bipolar signal from the line via the RTIP and RRing signals across a 1:1 Transformer or a 0.01µF Capacitor. The Receive Section will do the following:

- Adjust the signal level through an AGC circuit.
- Optionally equalize this signal for cable loss.
- Route the sliced data to the HDB3/B3ZS Decoder, during which the original data content as transmitted by the Remote Terminal Equipment is restored to its original content.
- The recovered clock and data outputs to the Local Terminal Equipment in the form of CMOS level signals via the RPOS_(n), RNEG_(n) and RxClk_(n) output pins.

THE MICROPROCESSOR SERIAL INTERFACE

The XRT73L02A contains two identical channels. The Microprocessor Interface Inputs are common to both channels. The descriptions that follow refer to Channel (n) where (n) represents Channel 0 or Channel 1.

The XRT73L02A can be configured to operate in either the Hardware Mode or the HOST Mode.

a. Operating in the Hardware Mode

The XRT73L02A can be configured to operate in the Hardware Mode by tying the HOST/($\overline{HW}$) input pin to GND.

When the XRT73L02A is operating in the Hardware Mode, the following is true:

1. The Microprocessor Serial Interface block is disabled.
2. The XRT73L02A is configured via input pin settings.

Each of the pins associated with the Microprocessor Serial Interface takes on their alternative role as defined in Table 1.

TABLE 1: ROLE OF MICROPROCESSOR SERIAL INTERFACE PINS WHEN THE XRT73L02A IS IN THE HARDWARE MODE

PIN #	PIN NAME	FUNCTION WHILE IN HARDWARE MODE
17	$\overline{CS}$/(ENDECDIS)	ENDECDIS
18	SClk/(RxOFF_1)	RxOFF_1
19	SDI/(RxOFF_0)	RxOFF_0
20	SDO/(E3_Ch_0)	E3_Ch_0
42	$\overline{REGR}$/(RxClkINV)	RxClkINV

When the XRT73L02A is operating in the Hardware Mode, all of the remaining input pins become active.

b. Operating in the HOST Mode

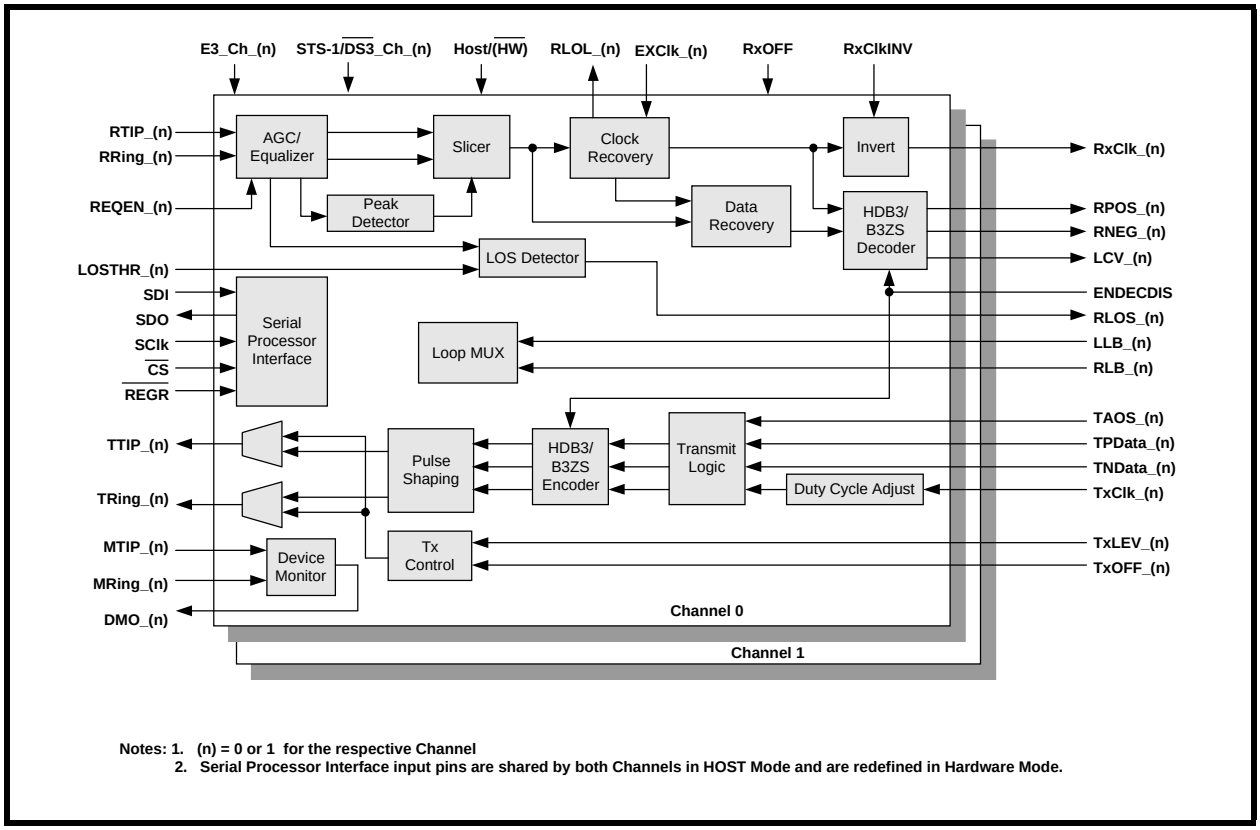
The XRT73L02A can be configured to operate in the HOST Mode by tying the HOST/($\overline{HW}$) input pin to VDD.

When the XRT73L02A is operating in the HOST Mode, the following is true:

1. The Microprocessor Serial Interface block is enabled. Writing the appropriate data into the on-chip Command Registers makes many configuration selections.
2. All of the following input pins are disabled and should be connected to GND.
   - Pins 1, 60 - TxLEV_(n)
   - Pins 2, 59 - TAOS_(n)
   - Pins 30, 31 - REQEN_(n)
   - Pins 25, 36 - RLB_(n)
   - Pins 24, 37 - LLB_(n)
   - Pin 39 - E3_Ch_(n)
   - Pins 21, 41 - STS1/$\overline{DS3}$_Ch_(n)

In HOST Mode Operation, the TxOFF_(n) input pins can still be used to turn on or turn off the Transmit Output Drivers in Channels 0 and 1, respectively. The intent behind this feature is to permit a system designed for redundancy to quickly switch out a defective line card and switch-in the back-up line card.

FIGURE 9. FUNCTIONAL BLOCK DIAGRAM OF THE XRT73L02A



Notes: 1. (n) = 0 or 1 for the respective Channel
2. Serial Processor Interface input pins are shared by both Channels in HOST Mode and are redefined in Hardware Mode.

1.0 SELECTING THE DATA RATE

Each channel in the XRT73L02A can be configured to support the E3 (34.368 Mbps), DS3 (44.736 Mbps) or SONET STS-1 (51.84 Mbps) rates and to operate in a mode/data rate that is independent of the other channel.

Two methods are available to select the data rate for each channel of the XRT73L02A.

1.1 CONFIGURING CHANNEL (n)

Refer to Table 2 to determine the appropriate Address for each Command Register of each channel in the XRT73L02A. The Command Register description refers to CR(m)-(n), where (m) = 0 to 7 and (n) refers to a particular channel of the XRT73L02A.

TABLE 2: ADDRESSES AND BIT FORMATS OF THE XRT73L02A COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	TYPE	D4	D3	D2	D1	D0
CHANNEL0							
0x00	CR0-0	RO	RLOL_0	RLOS_0	ALOS_0	DLOS_0	DMO_0
0x01	CR1-0	R/W	TxOFF_0	TAOS_0	TxClkINV_0	TxLEV_0	TxBIN_0
0x02	CR2-0	R/W	Reserved	ENDECDIS_0	ALOSDIS_0	DLOSDIS_0	REQEN_0
0x03	CR3-0	R/W	SR/($\overline{DR}$)_0	LOSMUT_0	RxOFF_0	RxClk_0INV	Reserved
0x04	CR4-0	R/W	Reserved	STS-1/$\overline{DS3}$_Ch_0	E3_Ch_0	LLB_0	RLB_0
0x05	CR5-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL1							
0x08	CR0-1	RO	RLOL_1	RLOS_1	ALOS_1	DLOS_1	DMO_1
0x09	CR1-1	R/W	TxOFF_1	TAOS_1	TxClkINV_1	TxLEV_1	TxBIN_1
0x0A	CR2-1	R/W	Reserved	ENDECDIS_1	ALOSDIS_1	DLOSDIS_1	REQEN_1
0x0B	CR3-1	R/W	SR/($\overline{DR}$)_1	LOSMUT_1	RxOFF_1	RxClk_1INV	Reserved
0x0C	CR4-1	R/W	Reserved	STS-1/$\overline{DS3}$_Ch_1	E3_Ch_1	LLB_1	RLB_1
0x0D	CR5-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0E	CR6-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0F	CR7-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Address:

The register addresses presented in the **Hexadecimal** format.

Type:

The Command Registers are either Read-Only (RO) or Read/Write (R/W) type of registers.

The default value for each of the bit-fields in these registers is "0".

a. Operating in the Hardware Mode

To configure individual Channel Data Rate, set the E3_Ch_(n) and the STS-1/$\overline{DS3}$_Ch_(n) input pins (where n = 0 or 1) to the appropriate logic states referenced in Table 3.

TABLE 3: SELECTING THE DATA RATE FOR CHANNEL (N) OF THE XRT73L02A, VIA THE E3_CH_(N) AND STS-1/$\overline{DS3}$_CH_(N) INPUT PINS (HARDWARE MODE)

DATA RATE	STATE OF E3_CH_(n) PIN (PIN 20 OR 39)	STATE OF STS-1/$\overline{DS3}$_CH_(n) PIN (PIN 21 OR 41)	MODE OF B3ZS/HDB3 ENCODER/ DECODER BLOCKS
E3 (34.368 Mbps)	1	X (Don't Care)	HDB3
DS3 (44.736 Mbps)	0	0	B3ZS
STS-1 (51.84 Mbps)	0	1	B3ZS

b. Operating in the HOST Mode.

To configure the Data Rate of a Channel, write the appropriate values into the STS-1/$\overline{DS3}$_Ch_(n) and E3_Ch_(n) bit-fields in Command Register CR4-(n).

NOTE: Reference Table 2 for the correct address of each channel.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/($\overline{DS3}$)_(n)	E3_Ch_(n)	LLB_(n)	RLB_(n)
X	X	X	X	X

Table 4 relates the values of these two bit-fields to the selected data rates.

TABLE 4: SELECTING THE DATA RATE FOR CHANNEL (n) OF THE XRT73L02A VIA THE STS-1/$\overline{DS3}$_CH_(n) AND THE E3_CH_(n) BIT-FIELDS IN THE APPROPRIATE COMMAND REGISTER (HOST MODE)

SELECTED DATA RATE	STS-1/$\overline{DS3}$_CH_(n) (D3)	E3_CH_(n) (D2)
E3	X (Don't Care)	1
DS3	0	0
STS-1	1	0

Making these selections does the following:

- Configure the VCO Center Frequency of Channel (n) of the Clock Recovery Phase-Locked Loop to match the selected data rate.
- If the DS3 or STS-1 data rates are selected, it configures the B3ZS/(HDB3) Encoder and Decoder blocks to support B3ZS Encoding/Decoding.
- If the E3 data rate is selected, it configures the B3ZS/(HDB3) Encoder and Decoder blocks to support HDB3 Encoding/Decoding.
- Configure the on-chip Pulse-Shaping circuitry to generate Transmit Output pulses of the appropriate shape and width to meet the applicable pulse template requirement.
- Establishes the LOS Declaration/Clearance Criteria for Channel (n) (Section 3.5).

2.0 THE TRANSMIT SECTION

Figure 9 shows the Transmit Section in each Channel of the XRT73L02A, consisting of the following blocks:

- Transmit Logic Block
- TxClk_(n) Duty Cycle Adjust Block
- HDB3/(B3ZS) Encoder
- Pulse Shaping Block

The purpose of the Transmit Section in each Channel of the XRT73L02A is to take TTL/CMOS level data from the Terminal Equipment and encode it into a format that can:

1. be efficiently transmitted over coaxial cable at E3, DS3 or STS-1 data rates,
2. be reliably received by the Remote Terminal Equipment at the other end of the E3, DS3 or STS-1 data link, and
3. comply with the applicable pulse template requirements.

The circuitry that the Transmit Section in each Channel of the XRT73L02A takes to accomplish this goal is discussed below.

2.1 THE TRANSMIT LOGIC BLOCK

The purpose of the Transmit Logic Block is to accept either Dual-Rail or Single-Rail (binary data stream) TTL/CMOS level data and timing information from the Terminal Equipment.

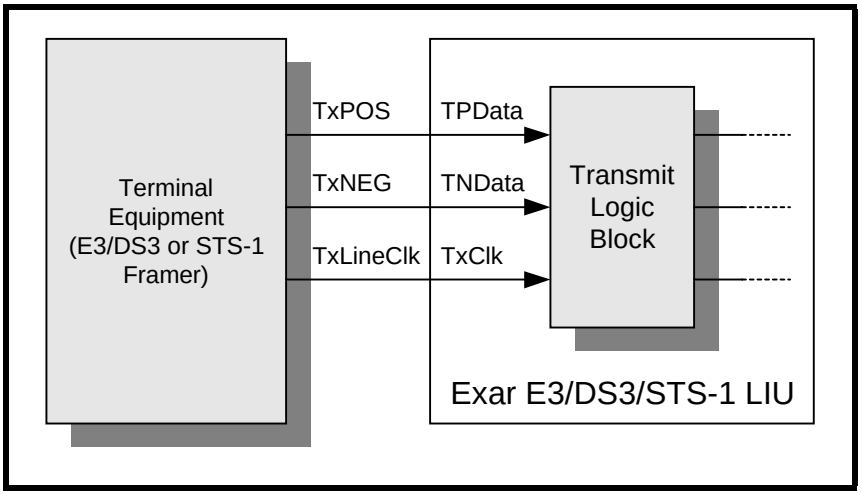
2.1.1 Accepting Dual-Rail Data from the Terminal Equipment

Whenever the XRT73L02A accepts Dual-Rail data from the Terminal Equipment, it does so via the following input signals:

- TPData_(n)
- TNData_(n)
- TxClk_(n)

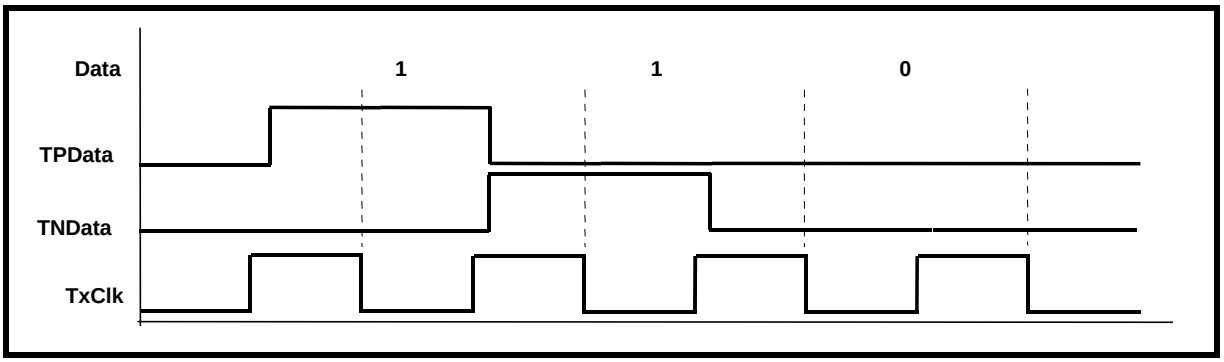
Figure 10 illustrates the typical interface for the transmission of data in a Dual-Rail Format between the Terminal Equipment and the Transmit Section of the XRT73L02A.

FIGURE 10. THE TYPICAL INTERFACE FOR DATA TRANSMISSION IN DUAL-RAIL FORMAT FROM THE TRANSMITTING TERMINAL EQUIPMENT TO THE TRANSMIT SECTION OF A CHANNEL OF THE XRT73L02A



The manner that the LIU handles Dual-Rail data is described below and illustrated in Figure 11. The Transmit Section of a Channel typically samples the data on the TPData and TNData input pins on the falling edge of TxClk_(n).

FIGURE 11. HOW THE XRT73L02A SAMPLES THE DATA ON THE TPDATA AND TNDATA INPUT PINS



TxClk_(n) is the clock signal that is of the selected data rate frequency for E3 = 34.368 MHz, DS3 = 44.736 MHz and STS-1 = 51.84 MHz. If the Transmit Section samples a “1" on the TPData input pin, the Transmit Section of the XRT73L02A generates a positive polarity pulse via the TTIP_(n) and TRing_(n) output pins across a 1:1 transformer. If the Transmit Section samples a "1" on the TNData input pin, then the Transmit Section ultimately generates a negative polarity pulse via the TTIP_(n) and TRing_(n) output pins across a 1:1 transformer.

2.1.2 Configure Channel (n) to accept Single-Rail Data from the Terminal Equipment

To transmit data in a Single-Rail data from the Terminal Equipment, configure the XRT73L02A in the HOST Mode.

Write a "1" into the TxBin_(n) (TRANSMIT BINary) bit-field of Command Register CR1-(n) shown below.

NOTE: *Please refer to Table 2 for the Address of the individual Channel (n).*

COMMAND REGISTER CR1-(N)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	TxBin_(n)
X	X	X	X	1

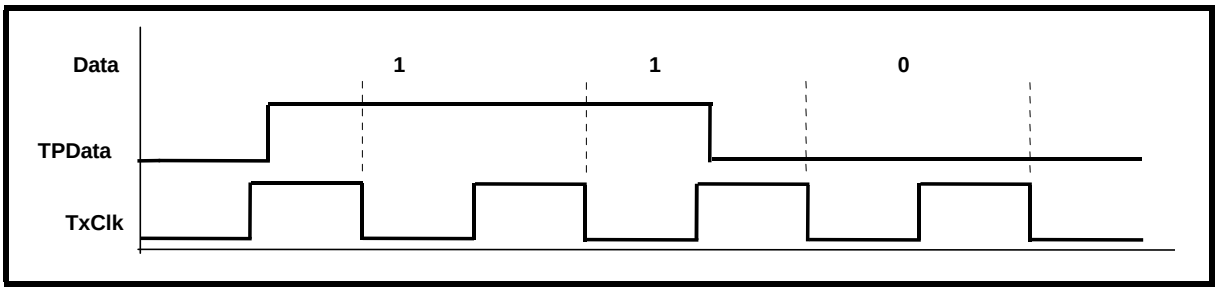
The Transmit Section of each channel samples this input pin on the falling edge of the TxClk_(n) clock signal and encodes this data into the appropriate bipolar line signal across the TTIP_(n) and TRing_(n) output pins.

NOTES:

1. *In this mode the Transmit Logic Block ignores the TNData input pin.*
2. *If the Transmit Section of a given channel is configured to accept Single-Rail data from the Terminal Equipment, the B3ZS/HDB3 Encoder must be enabled.*

Figure 12 illustrates the behavior of the TPData and TxClk_(n) signals when the Transmit Logic Block has been configured to accept Single-Rail data from the Terminal Equipment.

FIGURE 12. THE BEHAVIOR OF THE TPDATA AND TXCLK INPUT SIGNALS WHILE THE TRANSMIT LOGIC BLOCK IS ACCEPTING SINGLE-RAIL DATA FROM THE TERMINAL EQUIPMENT



2.2 THE TRANSMIT CLOCK DUTY CYCLE ADJUST CIRCUITRY

The on-chip Pulse-Shaping circuitry in the Transmit Section of each Channel of the XRT73L02A generates pulses of the appropriate shapes and width to meet the applicable pulse template requirements. The widths of these output pulses are defined by the width of the half-period pulses in the TxClk_(n) signal.

However, if the widths of the pulses in the TxClk_(n) clock signal are allowed to vary significantly, this could jeopardize the chip's ability to generate Transmit Output pulses of the appropriate width, thereby not meeting the Pulse Template requirement specification. Consequently, the chip's ability to generate compliant pulses could depend upon the duty cycle of the clock signal applied to the TxClk_(n) input pin.

The Transmit Clock Duty Cycle Adjust Circuitry accepts clock pulses via the TxClk_(n) input pin at duty cycles ranging from 30% to 70% and converts them to a 50% duty cycle.

2.3 THE HDB3/B3ZS ENCODER BLOCK

The purpose of the HDB3/B3ZS Encoder Block is to aid in the Clock Recovery process at the Remote Terminal Equipment by ensuring an upper limit on the number of consecutive zeros that can exist in the line signal.

2.3.1 B3ZS Encoding

If the XRT73L02A has been configured to operate in the DS3 or SONET STS-1 Modes, the HDB3/B3ZS Encoder blocks operate in the B3ZS Mode. When the Encoder is operating in this mode it parses through and searches the Transmit Binary Data Stream from the Transmit Logic Block for the occurrence of three (3) consecutive zeros (e.g., "000"). If the B3ZS Encoder finds an occurrence of three consecutive zeros, then it substitutes these three "0's" with either a "00V" or a "B0V" pattern.

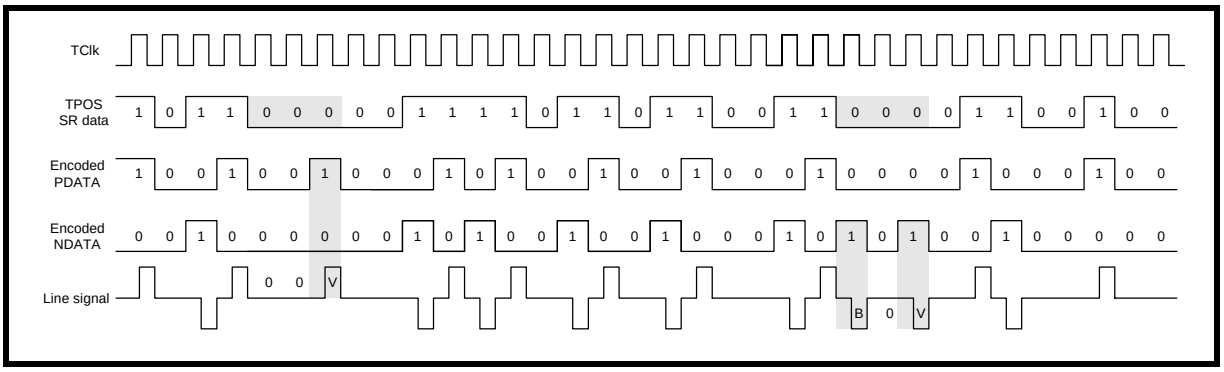
"B" represents a Bipolar pulse that is compliant with the Alternating Polarity requirements of the AMI (Alternate Mark Inversion) line code.

"V" represents a Bipolar Violation (e.g., a Bipolar pulse that violates the Alternating Polarity requirements of the AMI line code).

The B3ZS Encoder decides whether to substitute with either the "00V" or the "B0V" pattern in order to insure that an odd number of Bipolar pulses exist between any two consecutive violation pulses.

Figure 13 illustrates the B3ZS Encoder at work with two separate strings of three or more consecutive zeros.

FIGURE 13. AN EXAMPLE OF B3ZS ENCODING

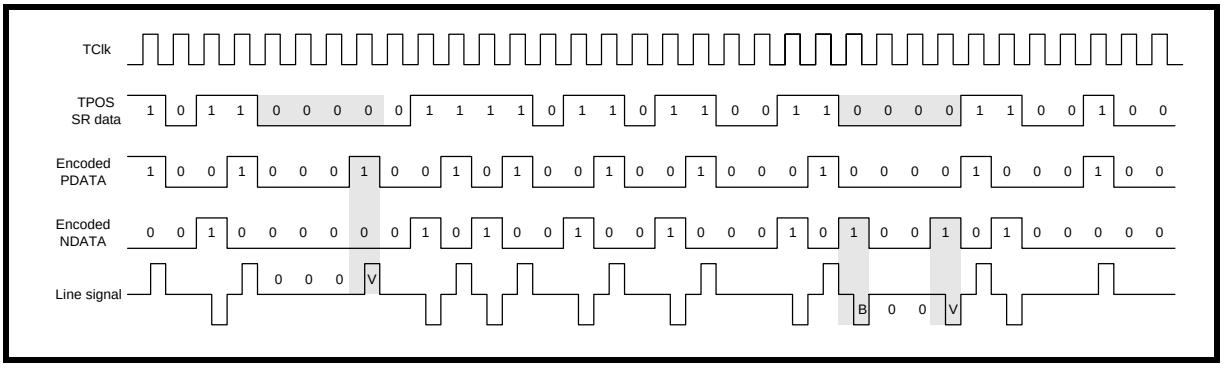


2.3.2 HDB3 Encoding

If the XRT73L02A has been configured to operate in the E3 Mode, the HDB3/B3ZS Encoder blocks operate in the HDB3 Mode. When the Encoder is operating in this mode it parses through and searches the Transmit Data Stream from the Transmit Logic Block for the occurrence of four (4) consecutive zeros ("0000"). If the HDB3 Encoder finds an occurrence of four consecutive zeros then it substitutes these four "0's" with either a "000V" or a "B00V" pattern. The HDB3 Encoder decides whether to substitute with either the "000V" or the "B00V" pattern in order to insure that an odd number of Bipolar pulses exist between any two consecutive violation pulses.

Figure 14 illustrates the HDB3 Encoder at work with two separate strings of four or more consecutive zeros.

FIGURE 14. AN EXAMPLE OF HDB3 ENCODING



2.3.3 Disabling the HDB3/B3ZS Encoder

The XRT73L02A HDB3/B3ZS Encoder can be disabled by two methods.

a. Operating in the Hardware Mode.

The HBD3/B3ZS Encoder blocks of all channels are disabled by setting the ENDECDIS (Encoder/Decoder Disable) input pin to “0".

NOTE: *By executing this step the HDB3/B3ZS Encoder and Decoder blocks in all channels of the XRT73L02A are globally disabled.*

b. Operating in the HOST Mode.

When the XRT73L02A is operating in the HOST Mode the HDB3/B3ZS Encoders in each channel can be individually enabled or disabled. Disable the HDB3/B3ZS Encoder block in Channel (n) by setting the ENDECDIS_(n) bit-field in Command Register (CR2-(n)), to "1".

COMMAND REGISTER CR2-(N)

D4	D3	D2	D1	D0
Reserved	ENDECDIS_(n)	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	1	X	X	X

If either of these two methods is used to disable the HDB3/B3ZS Encoder, the LIU transmits the data as received via the TPData and TNData input pins.

2.4 The Transmit Pulse Shaping Circuitry

The Transmit Pulse Shaper Circuitry consists of a Transmit Line Build-Out circuit which can be enabled or disabled by setting the TxLEV_(n) input pin or TxLEV_(n) bit-field to "High" or "Low". The purpose of the Transmit Line Build-Out circuit is to permit configuration of each channel in the XRT73L02A to transmit an output pulse which is compliant to either of the following pulse template requirements when measured at the Digital Cross Connect System. Each of these Bellcore specifications state that the cable length between the Transmit Output and the Digital Cross Connect system can range anywhere from 0 to 450 feet.

The Isolated DSX-3 Pulse Template Requirement per Bellcore GR-499-CORE is illustrated in Figure 15 and the Isolated STSX-1 Pulse Template Requirement per Bellcore GR-253-CORE is illustrated in Figure 16.

Figure 15. The Bellcore GR-499-CORE Transmit Output Pulse Template for DS3 Applications

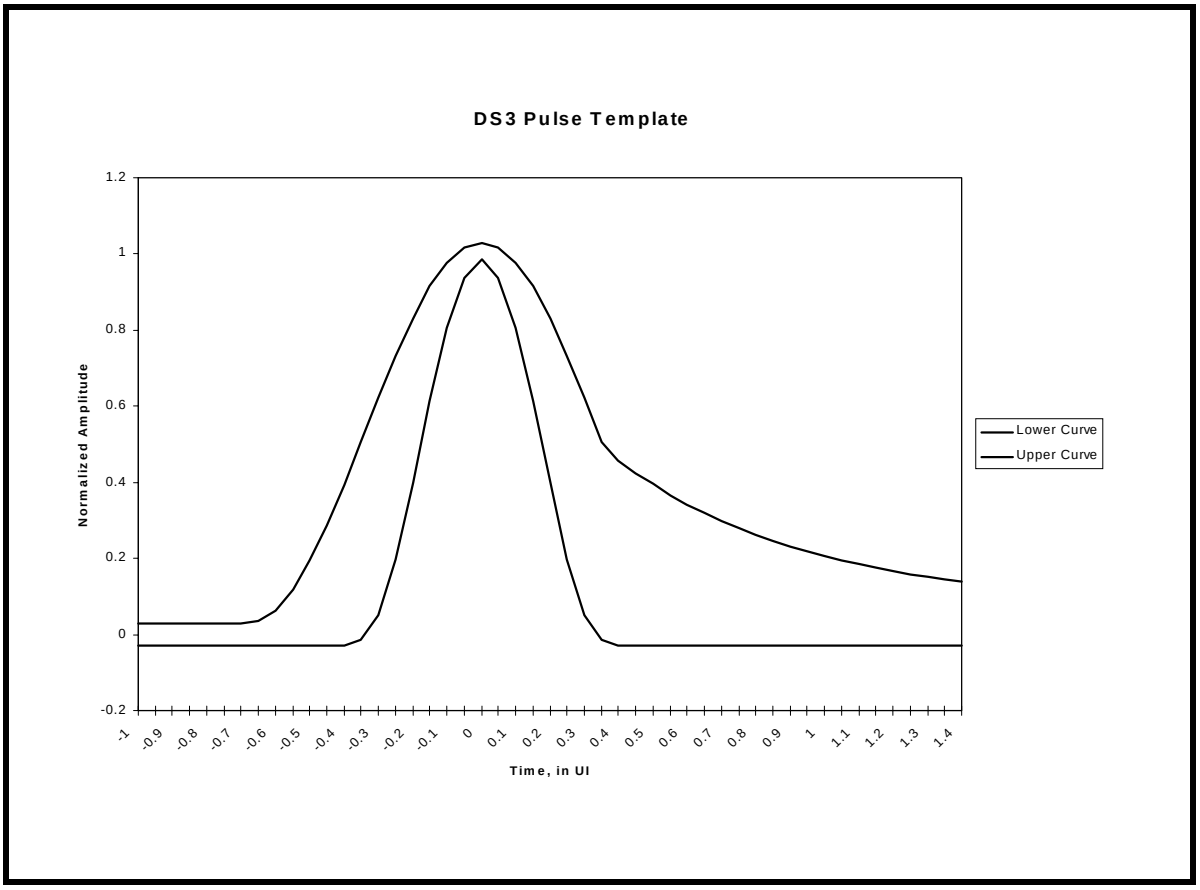
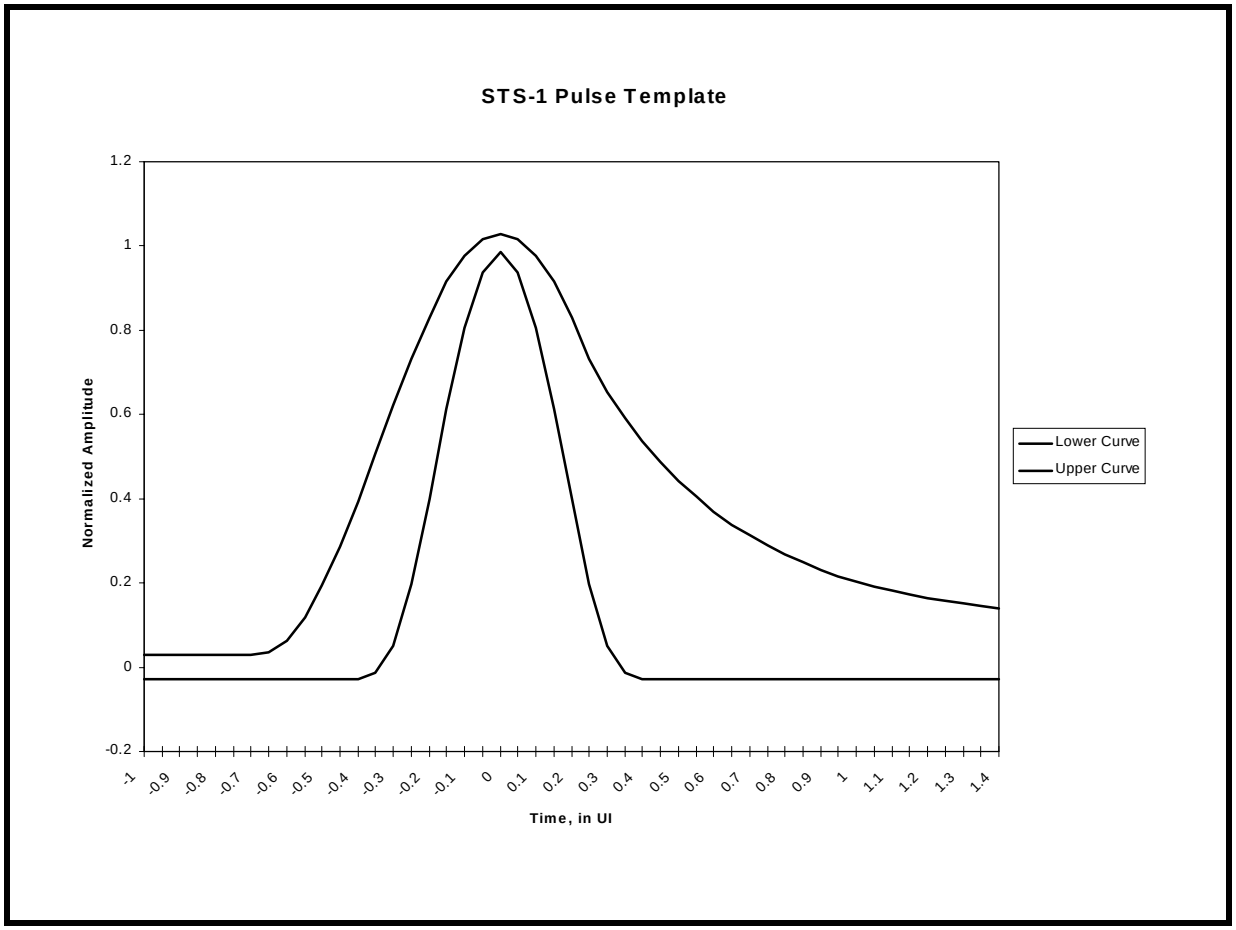


FIGURE 16. THE BELLCORE GR-253-CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS



2.4.1 Enabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out Circuit is enabled, the Transmit Section of Channel (n) of the XRT73L02A outputs shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

Enable the Transmit Line Build-Out circuit for each channel in the XRT73L02A by doing the following:

a. Operating in the Hardware Mode

Set the TxLEV_(n) input pin to "Low"

b. Operating in the HOST Mode

Set the TxLEV_(n) bit-field to "0".

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	TxBIN_(n)
0	X	X	0	X

2.4.2 Disabling the Transmit Line Build-Out Circuit

If the Transmit Line Build-Out circuit is disabled, the XRT73L02A outputs partially-shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

To disable the Transmit Line Build-Out circuit, do the following:

a. Operating in the Hardware Mode

Set the TxLEV_(n) input pin to "High".

b. Operating in the HOST Mode

Set the TxLEV_(n) bit-field to "1" as illustrated below.

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	TxBin_(n)
0	X	X	1	X

2.4.3 Design Guideline for Setting the Transmit Line Build-Out Circuit

The TxLEV_(n) input pins or bit-fields should be set based upon the overall cable length between the Transmitting Terminal and the Digital Cross Connect system where the pulse template measurements are made.

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is less than 225 feet, enable the Transmit Line Build-Out circuit by setting the TxLEV_(n) input pin or bit-field to "0".

NOTE: *In this case, the configured channel outputs shaped (e.g., not square-wave) pulses onto the line via its TTIP_(n) and TRing_(n) output pins. The shape of this output pulse is such that it complies with the pulse template requirements even when subjected to cable loss ranging from 0 to 225 feet.*

If the cable length between the Transmitting Terminal and the DSX-3 or STSX-1 is greater than 225 feet, disable the Transmit Line Build-Out circuit by setting the TxLEV_(n) input pin or bit-field to "1".

NOTE: *In this case, the configured channel in the XRT73L02A outputs partially-shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins. The cable loss that these pulses experience over long cable lengths (e.g., greater than 225 feet) causes these pulses to be properly shaped and comply with the appropriate pulse template requirement.*

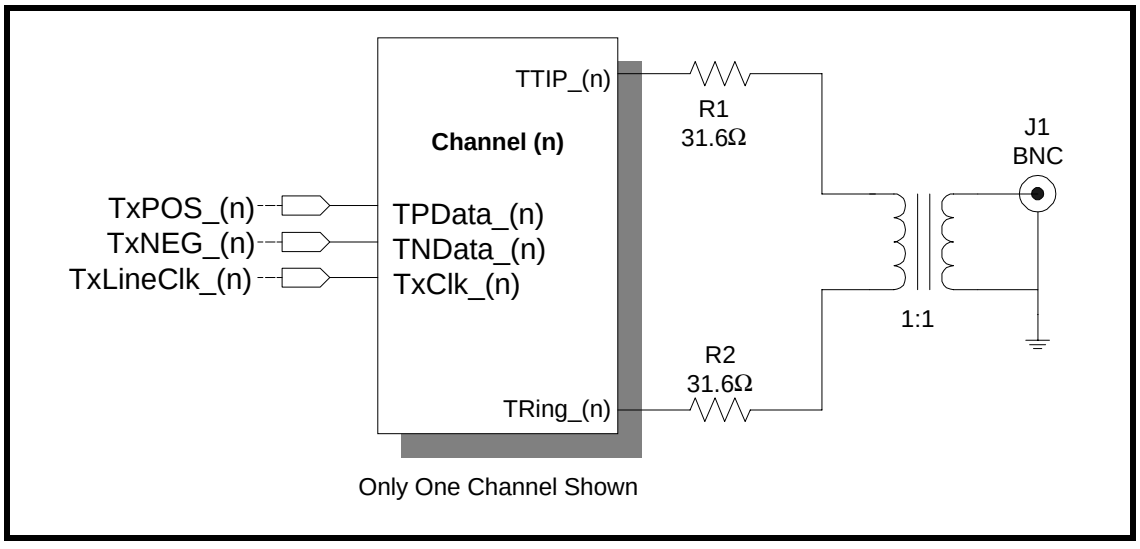
2.4.4 The Transmit Line Build-Out Circuit and E3 Applications

The ITU-T G.703 Pulse Template Requirements for E3 states that the E3 transmit output pulse should be measured at the Secondary Side of the Transmit Output Transformer for Pulse Template compliance. In other words, there is no Digital Cross Connect System pulse template requirement for E3. Consequently, the Transmit Line Build-Out circuit in a given Channel in the XRT73L02A is disabled whenever that channel has been configured to operate in the E3 Mode.

2.5 INTERFACING THE TRANSMIT SECTIONS OF THE XRT73L02A TO THE LINE

The E3, DS3 and SONET STS-1 specification documents all state that line signals transmitted over coaxial cable are to be terminated with 75 Ohm resistor. Interface the Transmit Section of the XRT73L02A in the manner illustrated in Figure 17 to accomplish this.

FIGURE 17. RECOMMENDED SCHEMATIC FOR INTERFACING THE TRANSMIT SECTION OF THE XRT73L02A TO THE LINE



TRANSFORMER RECOMMENDATIONS

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	40µH
Isolation Voltage	1500Vrms
Leakage Inductance	0.6µH

PART NUMBER	VENDOR	INSULATION	PACKAGE TYPE
PE-68629	Pulse	3000V	Large Thru-Hole
PE-65966	Pulse	1500V	Small Thru-Hole
PE-65967	Pulse	1500V	Small SMT
T3001	Pulse	1500V	Small SMT
TG01-0406NS	Halo	1500V	Small SMT
TTI 7601-SM	Trans-Power	1500V	Small SMT

TRANSFORMER VENDOR INFORMATION

Pulse

Corporate Office

12220 World Trade Drive
San Diego, CA 92128
Tel: (858)-674-8100
FAX: (858)-674-8262

Europe

1 & 2 Huxley Road
The Surrey Research Park
Guildford, Surrey GU2 5RE
United Kingdom
Tel: 44-1483-401700
FAX: 44-1483-401701

Asia

150 Kampong Ampat
#07-01/02
KA Centre
Singapore 368324
Tel: 65-287-8998
FAX: 65-280-0080

Website: http://www.pulseeng.com

Halo Electronics

Corporate Office

P.O. Box 5826
Redwood City, CA 94063
Tel: (650)568-5800
FAX: (650)568-6165

Email: info@haloelectronics.com

Website: http://www.haloelectronics.com

Transpower Technologies, Inc.

Corporate Office

Park Center West Building
9805 Double R Blvd, Suite # 100
Reno, NV 89511
(800)500-5930 or (775)852-0140

Email: info@trans-power.com

Website: http://www.trans-power.com

3.0 THE RECEIVE SECTION

Figure 9 indicates that the Receive Section in the XRT73L02A consists of the following blocks:

- AGC/Equalizer
- Peak Detector
- Slicer
- Clock Recovery PLL
- Data Recovery
- HDB3/B3ZS Decoder

The purpose of each Receive Section of the XRT73L02A is to take an incoming attenuated/distorted bipolar signal from the line and encode it back into the TTL/CMOS format where it can be received and processed by the Terminal Equipment.

3.1 INTERFACING THE RECEIVE SECTIONS OF THE XRT73L02A TO THE LINE

The design of the Receive Circuitry in the XRT73L02A allows for transformer-coupling or capacitive-coupling of the Receive Section to the line. As mentioned earlier, the specification documents for E3, DS3 and STS-1 all specify 75 Ohm termination loads when transmitting over coaxial cable. The recommended method of Transformer-Coupling the Receive Section of the XRT73L02A to the line is shown in Figure 18 and the Capacitive-Coupling method is shown in Figure 19.

FIGURE 18. RECOMMENDED SCHEMATIC FOR TRANSFORMER-COUPLING THE RECEIVE SECTION OF THE XRT73L02A TO THE LINE

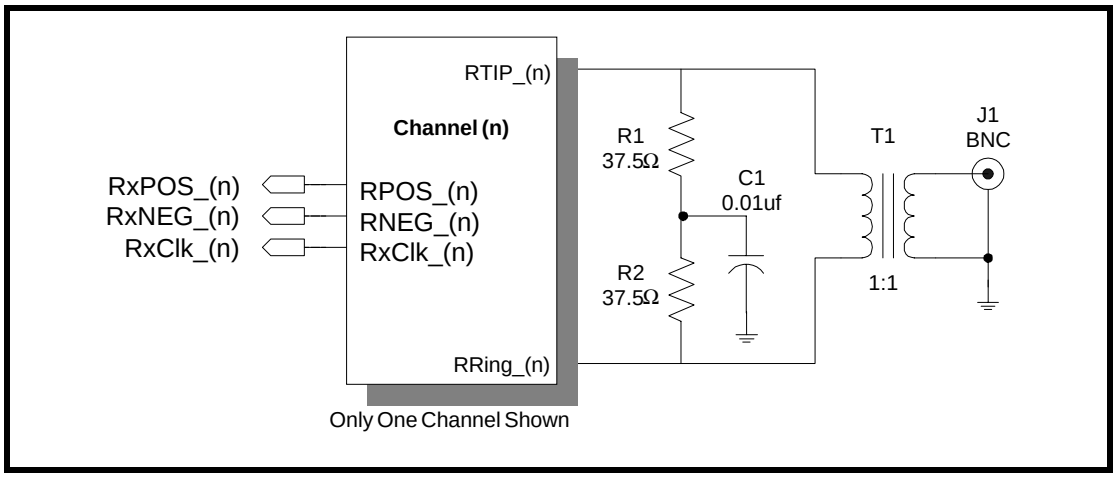
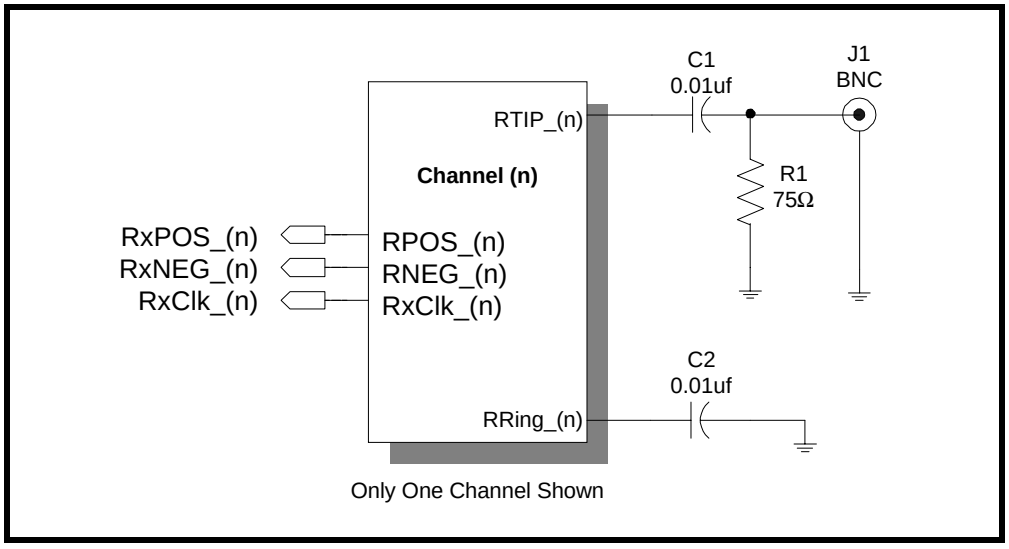


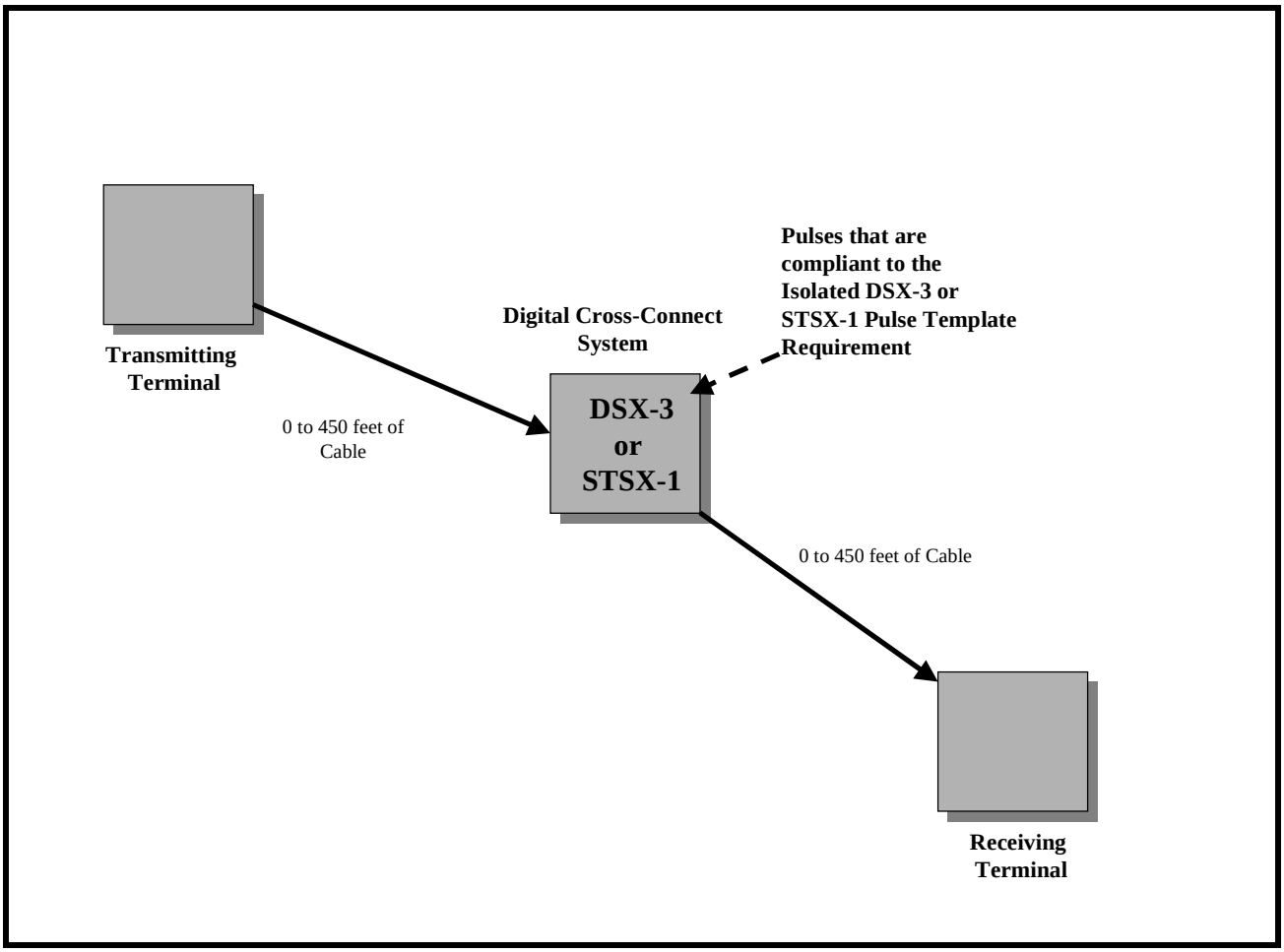
FIGURE 19. RECOMMENDED SCHEMATIC FOR CAPACITIVE-COUPLING THE RECEIVE SECTION OF THE XRT73L02A TO THE LINE



3.2 THE RECEIVE EQUALIZER BLOCK

The purpose of this block is to equalize the incoming distorted signal due to cable loss. The Receive Equalizer attempts to restore the shape of the line signal so that the transmitted data and clock can be recovered reliably.

FIGURE 20. THE TYPICAL APPLICATION FOR THE SYSTEM INSTALLER



- **Design Considerations for DS3 and STS-1 Applications**

When installing equipment into environments depicted in Figure 20, we recommend that the Receive Equalizer be enabled by setting the REQEN_(n) input pin for Channel (n) or the respective bit-fields to "1". The only time that the Receive Equalizer should be disabled is when an off-chip equalizer is in the Receive path between the Digital Cross-Connect system and the RTIP/RRing input pins, or in applications where the Receiver is monitoring the transmit output signal directly.

- **Design Considerations for E3 Applications or if the Overall Cable Length is known**

Figure 20 indicates the following:

a. The length of cable between the Transmitting Terminal and the Digital Cross-Connect system can range between 0 and 450 feet.

b. The length of cable between the Digital Cross-Connect system and the Receive Terminal can range between 0 and 450 feet.

Consequently, the overall cable length between the Transmitting Terminal and the Receiving Terminal can range between very short cable length (e.g., near 0 feet) up to 900 feet.

If during System Installation the overall cable length is known, to optimize the performance of the XRT73L02A in terms of receive jitter performance, etc., enable or disable the Receive Equalizer based upon the following recommendations:

The Receive Equalizer should be turned ON if the Receive Section of a given channel is going to re-

ceive a line signal with an overall cable length of 300 feet or greater. Conversely, turn OFF the Receive Equalizer if the Receive Section of a given channel is going to receive a line signal with an overall cable length of less than 300 feet.

NOTES:

1. *If the Receive Equalizer block is turned ON when it is receiving a line signal over short cable length the received line signal may be over-equalized, which could degrade performance by increasing the amount of jitter that exists in the recovered data and clock signals or by creating bit-errors.*
2. *The Receive Equalizer has been designed to counter the frequency-dependent cable loss that a line signal experiences as it travels from the transmitting terminal to the receiving terminal. However, the Receive Equalizer was not designed to counter flat loss where all of the Fourier frequency components within the line signal are subject to the same amount of attenuation. Flat loss is handled by the AGC block.*

Disable the Receive Equalizer block by doing either of the following:

a. Operating in the Hardware Mode

Set the REQEN_(n) input pin "Low".

b. Operating in the HOST Mode

Write a "0" to the REQEN_(n) bit-field in Command Register CR2.

COMMAND REGISTER CR2_(n))

D4	D3	D2	D1	D0
RESERVED	ENDECDIS_(n)	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	X	X	X	0

3.3 PEAK DETECTOR AND SLICER

After the incoming line signal has passed through the Receive Equalizer block, it is routed to the Slicer block. The Slicer block quantifies a given bit-period (or symbol) within the incoming line signal as either a “1” or a “0”.

3.4 CLOCK RECOVERY PLL

The purpose of the Clock Recovery PLL is to track the incoming Dual-Rail data stream and to derive and generate a recovered clock signal.

It is important to note that the Clock Recovery PLL requires a line rate clock signal at the ExClk input pin.

The Clock Recovery PLL operates in one of two modes:

- The Training Mode
- The Data/Clock Recovery Mode

3.4.1 The Training Mode

If a given channel in the XRT73L02A is not receiving a line signal via the RTIP and RRing input pins, or if the frequency difference between the line signal and that applied via the ExClk input pin exceeds 0.5%, the channel operates in the Training Mode. When the channel is operating in the Training Mode, it does the following:

a. Declare a Loss of Lock indication by toggling its respective RLOL_(n) output pin “High".

b. Output a clock signal via the RxClk_(n) output pin which is derived from the signal applied to the EXClk_(n) input pin.

3.4.2 The Data/Clock Recovery Mode

If the frequency difference between the line signal and that applied via the ExClk input pin is less than 0.5%, the channel operates in the Data/Clock Recovery mode. In this mode, the Clock Recovery PLL locks onto the line signal via the RTIP and RRing input pins.

3.5 THE HDB3/B3ZS DECODER

The Remote Transmitting Terminal typically encodes the line signal into some sort of Zero Suppression Line Code (e.g., HDB3 for E3 and B3ZS for DS3 and STS-1). The purpose of this encoding activity was to aid in the Clock Recovery process of this data from the Near-End Receiving Terminal. However, once the data has made it across the E3, DS3 or STS-1 Transport Medium and has been recovered by the Clock Recovery PLL, it is now necessary to restore the original content of the data. The purpose of the HDB3/B3ZS Decoding block is to restore the data transmitted over the E3, DS3 or STS-1 line to its original content prior to Zero Suppression Coding.

3.5.1 B3ZS Decoding DS3/STS-1 Applications

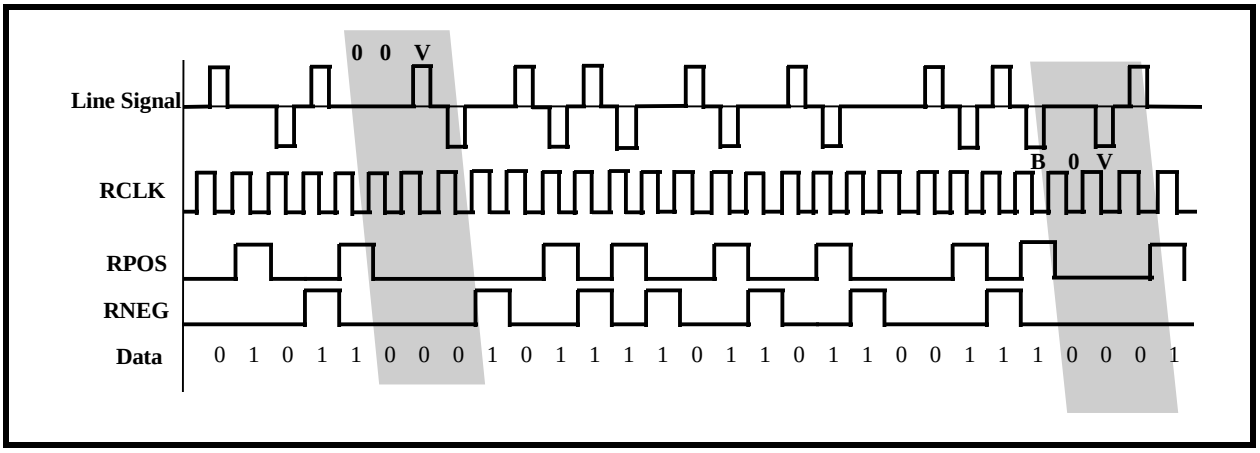
If the XRT73L02A is configured to operate in the DS3 or STS-1 Modes, then the HDB3/B3ZS Decoding Blocks perform B3ZS Decoding. When the Decoders are operating in this mode, each of the Decoders parses through its respective incoming Dual-Rail data

and checks for the occurrence of either a "00V" or a "B0V" pattern. If the B3ZS Decoder detects this particular pattern, it substitutes these bits with a "000" pattern.

NOTE: If the B3ZS Decoder detects any bipolar violations that is not in accordance with theB3ZS Line Code format or if the B3ZS Decoder detects a string of 3 or more consecutive "0's" in the incoming line signal, the B3ZS Decoder flags this event as a Line Code Violation by pulsing the LCV output pin "High".

Figure 21 illustrates the B3ZS Decoder at work with two separate Zero Suppression patterns in the incoming Dual-Rail Data Stream.

FIGURE 21. AN EXAMPLE OF B3ZS DECODING

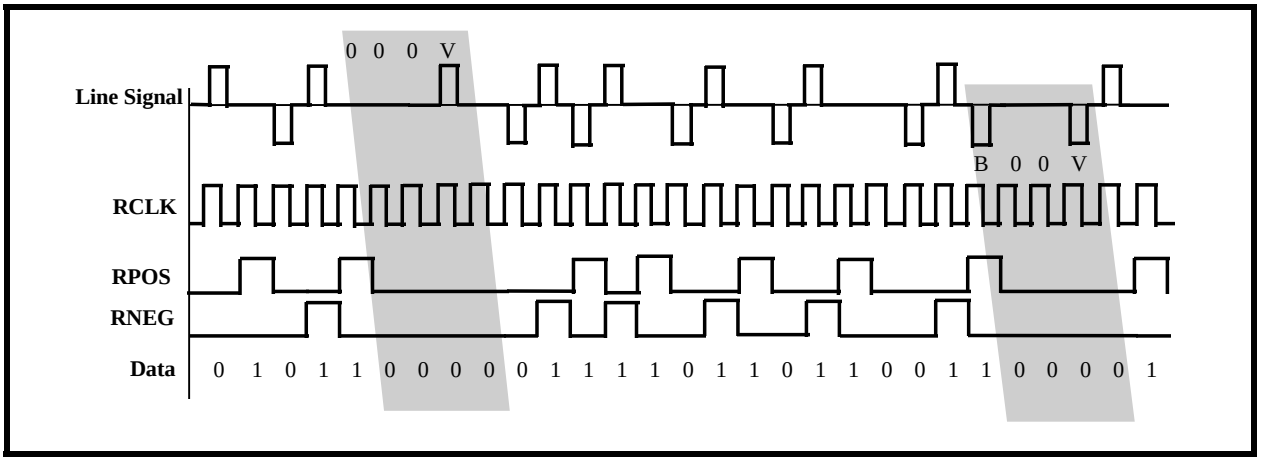


3.5.2 HDB3 Decoding E3 Applications

If the XRT73L02A is configured to operate in the E3 Mode, then each of the HDB3/B3ZS Decoding Blocks performs HDB3 Decoding. When the Decoders are operating in this mode, they each parse through the incoming Dual-Rail data and check for the occurrence of either a "000V" or a "B00V" pattern. If the HDB3 Decoder detects this particular pattern, it substitutes these bits with a "0000" pattern.

Figure 22 illustrates the HDB3 Decoder at work with two separate Zero Suppression patterns in the incoming Dual-Rail Data Stream.

FIGURE 22. AN EXAMPLE OF HDB3 DECODING



NOTE: If the HDB3 Decoder detects any bipolar violation (e.g., "V") pulses that is not in accordance with the HDB3 Line Code format, or if the HDB3 Decoder detects a string of 4 or more "0's" in the incoming line signal, the HDB3 Decoder flags this event as a Line Code Violation by pulsing the LCV output pin "High".

3.5.3 Configuring the HDB3/B3ZS Decoder

The XRT73L02A can enable or disable the HDB3/B3ZS Decoder blocks of each Channel by either of the following means.

a. Operating in the HOST Mode

Enable the HDB3/B3ZS Decoder block of Channel (n) by writing a "0" into the ENDECDIS_(n) bit-field in Command Register CR2-(n).

COMMAND REGISTER CR2-(n)

D4	D3	D2	D1	D0
Reserved	ENDEC_DIS	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	0	X	X	1

b. Operating in the Hardware Mode

To globally enable all HDB3/B3ZS Decoder blocks in the XRT73L02A, pull the ENDEC_DIS input pin “Low". To globally disable all HDB3/B3ZS Decoder blocks in the XRT73L02A and configure the XRT73L02A to transmit and receive in an AMI format, pull the ENDEC_DIS input pin "High".

3.6 LOS Declaration/Clearance

Each channel of the XRT73L02A contains circuitry that monitors the following two parameters associated with the incoming line signals.

1. The amplitude of the incoming line signal via the RTIP and RRing inputs.
2. The number of pulses detected in the incoming line signal within a certain amount of time.

If a given channel of the XRT73L02A determines that the incoming line signal is missing due to either insufficient amplitude or a lack of pulses in the incoming line signal, it declares a Loss of Signal (LOS) condition. The channel declares the LOS condition by toggling its respective RLOS_(n) output pin “High” and by setting its corresponding RLOS_(n) bit field in Command Register 0 or Command Register 8 to "1".

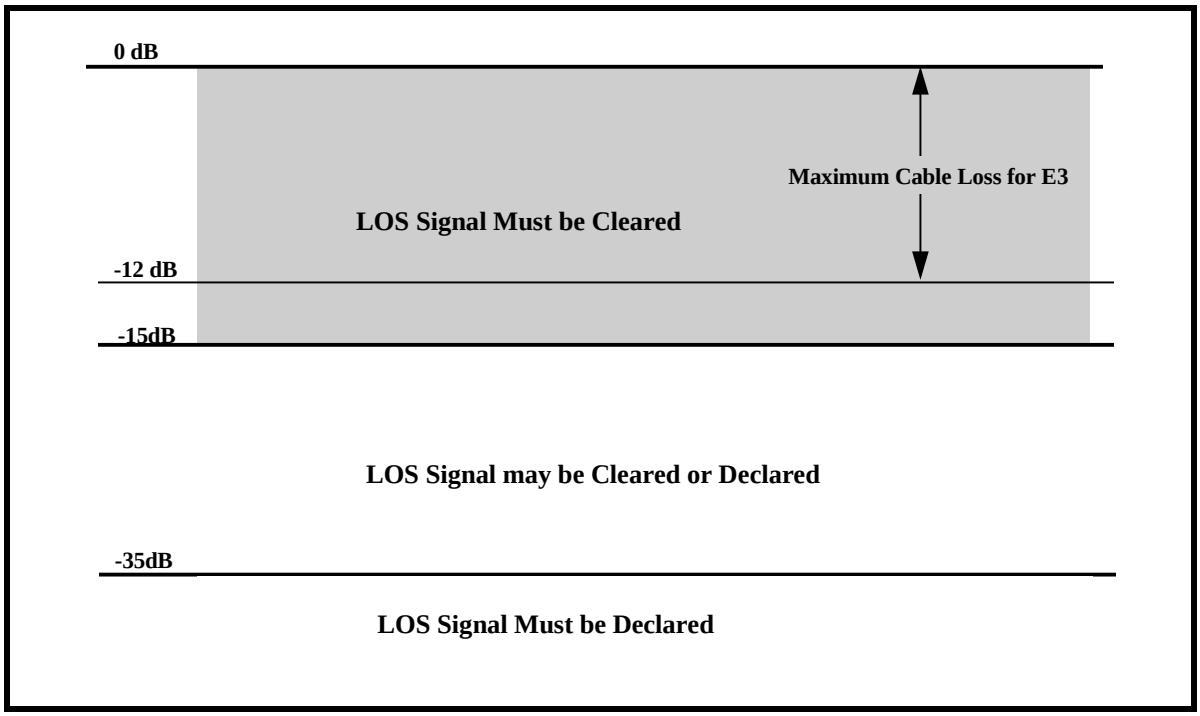
Conversely, if the channel determines that the incoming line signal has been restored (e.g., there is sufficient amplitude and pulses in the incoming line signal), it clears the LOS condition by toggling its respective RLOS_(n) output pin "Low" and setting its corresponding RLOS_(n) bit-field to "0".

In general, the LOS Declaration/Clearance scheme that is employed in the XRT73L02A is based upon ITU-T Recommendation G.775 for both E3 and DS3 applications.

3.6.1 The LOS Declaration/Clearance Criteria for E3 Applications

When the XRT73L02A is operating in the E3 Mode, a given channel declares an LOS Condition if its receive line signal amplitude drops to -35dB or below. Further, the channel clears the LOS Condition if its receive line signal amplitude rises back to -15dB or above. Figure 23 illustrates the signal levels at which each channel of the XRT73L02A declares and clears LOS.

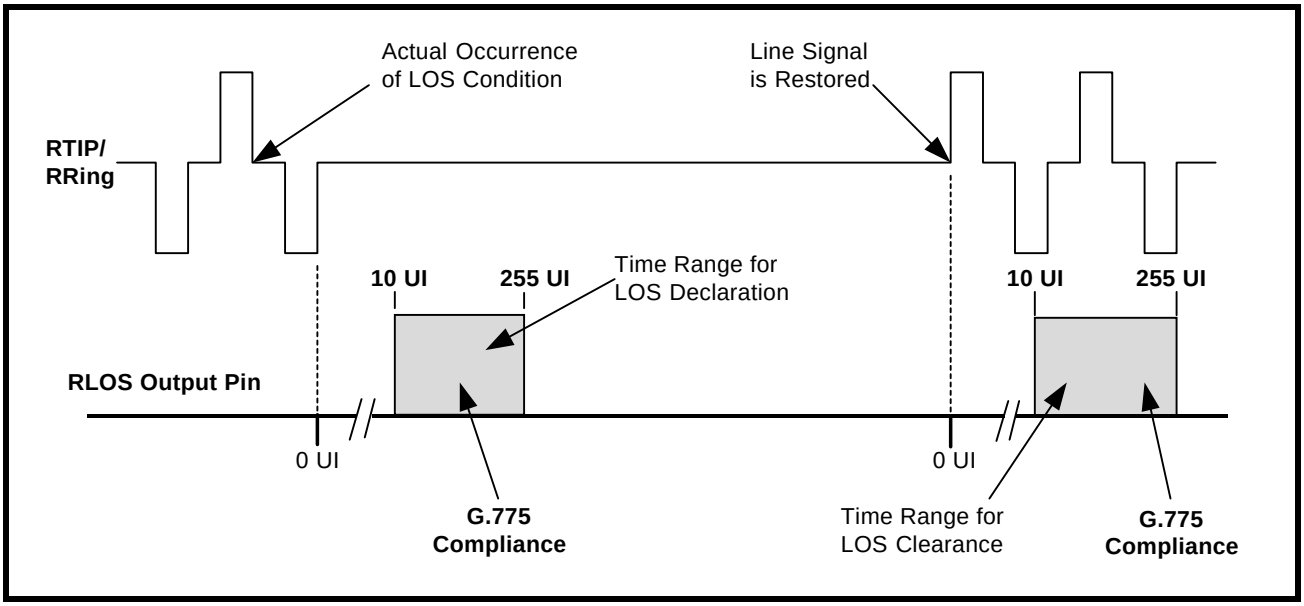
FIGURE 23. THE SIGNAL LEVELS AT WHICH THE XRT73L02A DECLARES AND CLEARS LOS



Timing Requirements associated with Declaring and Clearing the LOS Indicator

The XRT73L02A was designed to meet the ITU-T G.775 specification timing requirements for declaring and clearing the LOS indicator. In particular, a channel of the XRT73L02A declares an LOS between 10 and 255 UI (or E3 bit-periods) after the actual time the LOS condition occurred. The channel clears the LOS indicator within 10 to 255 UI after restoration of the incoming line signal. Figure 24 illustrates the LOS Declaration and Clearance behavior in response to the Loss of Signal event and then the restoration of the signal.

FIGURE 24. THE BEHAVIOR OF THE LOS OUTPUT INDICATOR IN RESPONSE TO THE LOSS OF SIGNAL AND THE RESTORATION OF SIGNAL



3.6.2 The LOS Declaration/Clearance Criteria for DS3 and STS-1 Applications

When the XRT73L02A is operating in the DS3 or STS-1 Mode, each channel in the XRT73L02A declares and clears LOS based upon the following two criteria:

- Analog LOS (ALOS) Declaration/Clearance Criteria
- Digital LOS (DLOS) Declaration/Clearance Criteria

In the DS3 Mode, the LOS output (RLOS) is simply the logical "OR" of the ALOS and DLOS states.

1. The Analog LOS (ALOS) Declaration/Clearance Criteria

A channel in the XRT73L02A declares an Analog LOS (ALOS_(n)) Condition if the amplitude of the incoming line signal drops below a specific amplitude as defined by the voltage at the LOSTHR input pin and whether the Receive Equalizer is enabled or not.

Table 5 presents the various voltage levels at the LOSTHR input pin, the state of the Receive Equalizer, and the corresponding ALOS (Analog LOS) threshold amplitudes.

TABLE 5: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN FOR DS3 AND STS-1 APPLICATIONS

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS	SIGNAL LEVEL TO CLEAR ALOS
DS3	1	1	≤22mV	≥90mV
	0	1	≤17mV	≤70mV
STS-1	1	1	≤25mV	≥115mV
	0	1	≤20mV	≤90mV

Declaring ALOS

A Channel (n) in the XRT73L02A declares ALOS_(n) whenever the amplitude of the receive line signal falls below the signal levels to declare ALOS, as specified in Table 5.

Clearing ALOS_(n)

A Channel (n) clears ALOS_(n) whenever the amplitude of the receive line signal increases above the signal levels to declare ALOS, as specified in Table 5.

There is approximately a 2dB hysteresis in the received signal level that exists between declaring and clearing ALOS_(n) in order to prevent chattering in the RLOS_(n) output signal.

Monitoring the State of ALOS_(n)

If the XRT73L02A is operating in the HOST Mode, the state of ALOS_(n) of Channel (n) can be polled or monitored by reading in the contents of Command Register CR0.

COMMAND REGISTER CR0-(n)

D4	D3	D2	D1	D0
RLOL_(n)	RLOS_(n)	ALOS_(n)	DLOS_(n)	DMO_(n)
Read Only	Read Only	Read Only	Read Only	Read Only

If the ALOS_(n) bit-field contains a "1", then the corresponding Channel (n) is currently declaring an ALOS condition. If the ALOS_(n) bit-field contains a "0", then the channel is not currently declaring an ALOS condition.

Disabling the ALOS Detector

For debugging purposes it may be useful to disable the ALOS Detector in the XRT73L02A. If the XRT73L02A is operating in the HOST Mode, the ALOS Detector can be disabled by writing a "1" into the ALOSDIS_(n) bit-field in Command Register CR2.

COMMAND REGISTER CR2-(n)

D4	D3	D2	D1	D0
Reserved	ENDECDIS_(n)	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	X	1	X	X

2. The Digital LOS (DLOS) Declaration/Clearance Criteria

A given Channel (n) in the XRT73L02A declares a Digital LOS (DLOS_(n)) condition if the XRT73L02A detects 160±32 or more consecutive "0's" in the incoming data.

The channel clears DLOS if it detects four consecutive sets of 32 bit-periods, each of which contains at least 10 "1's" (e.g., average pulse density of greater than 33%).

Monitoring the State of DLOS

If the XRT73L02A is operating in the HOST Mode the state of DLOS_(n) of Channel (n) can be polled or monitored by reading in the contents of Command Register CR0.

COMMAND REGISTER CR0-(n)

D4	D3	D2	D1	D0
RLOL_(n)	RLOS_(n)	ALOS_(n)	DLOS_(n)	DMO_(n)
Read Only	Read Only	Read Only	Read Only	Read Only

If the DLOS_(n) bit-field contains a “1”, then the corresponding Channel (n) is currently declaring a DLOS condition. If the DLOS_(n) bit-field contains a “0”, the Channel (n) is currently declaring the DLOS condition.

Disabling the DLOS Detector

For debugging purposes, it is useful to be able to disable the DLOS_(n) detector in the XRT73L02A. If the XRT73L02A is operating in the HOST Mode, the DLOS Detector can be disabled by writing a “1” into the DLOSDIS_(n) bit-field of Command Register CR2.

COMMAND REGISTER CR2-(n)

D4	D3	D2	D1	D0
Reserved	ENDECDIS_(n)	ALOSDIS_(n)	DLOSDIS_(n)	REQEN_(n)
X	X	X	1	X

NOTE: *Setting both the ALOSDIS_(n) and DLOSDIS_(n) bit-fields to "1" disables LOS Declaration by Channel (n).*

3.6.3 Muting the Recovered Data while the LOS is being Declared

In some applications it is not desirable for a channel of the XRT73L02A to recover data and route it to the Receiving Terminal while the channel is declaring an LOS condition. Consequently, the XRT73L02A includes a LOS Muting feature. This feature if enabled causes a given channel to halt transmission of the recovered data to the Receiving Terminal while the LOS condition is "true". In this case, the RPOS_(n) and RNEG_(n) output pins are forced to "0". Once the LOS condition has been cleared, the channel resumes normal transmission of the recovered data to the Receiving Terminal.

This feature is available whenever the XRT73L02A is operating in the HOST or Hardware Mode.

a. Operating in the Hardware Mode.

To enable the Muting upon LOS feature for all channels of the XRT73L02A, pull the LOSMUTEN output pin "High".

b. Operating in the HOST Mode.

The Muting upon LOS feature for each Channel can be enabled by writing a "1" into the LOSMUT_(n) bit-field in Command Register 3.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
SR/($\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF_(n)	RxClk_(n)INV	Reserved
X	1	X	X	X

NOTES:

1. *This step only enables the Muting upon LOS feature in Channel (n).*
2. *Each channel (n) automatically declares an LOS (Loss of Signal) condition anytime it has been configured to operate in either the Analog Local Loop-Back or Digital Local Loop-Back modes. To configure the chip to operate in either of these modes, disable the Muting-upon-LOS feature.*

3.7 ROUTING RECOVERED TIMING AND DATA INFORMATION TO THE RECEIVING TERMINAL EQUIPMENT

Each channel in the XRT73L02A takes the Recovered Timing and Data information, converts it into CMOS levels and routes it to the Receiving Terminal Equipment via the RPOS_(n), RNEG_(n) and RxClk_(n) output pins.

Each channel of the XRT73L02A can deliver the recovered data and clock information to the Receiving Terminal in either a Single-Rail or Dual-Rail format.

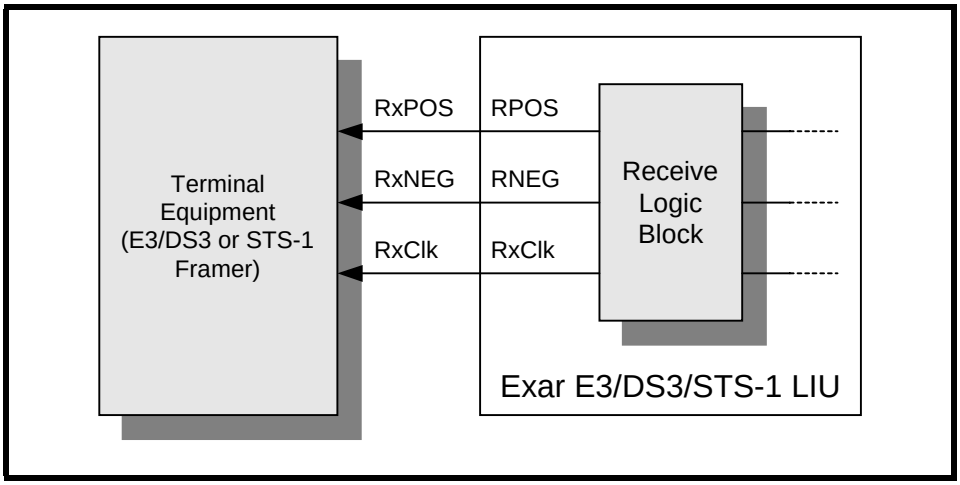
3.7.1 Routing Dual-Rail Format Data to the Receiving Terminal Equipment

Whenever a channel of the XRT73L02A delivers Dual-Rail format to the Terminal Equipment, it does so via the following signals:

- RPOS_(n)
- RNEG_(n)
- RxClk_(n)

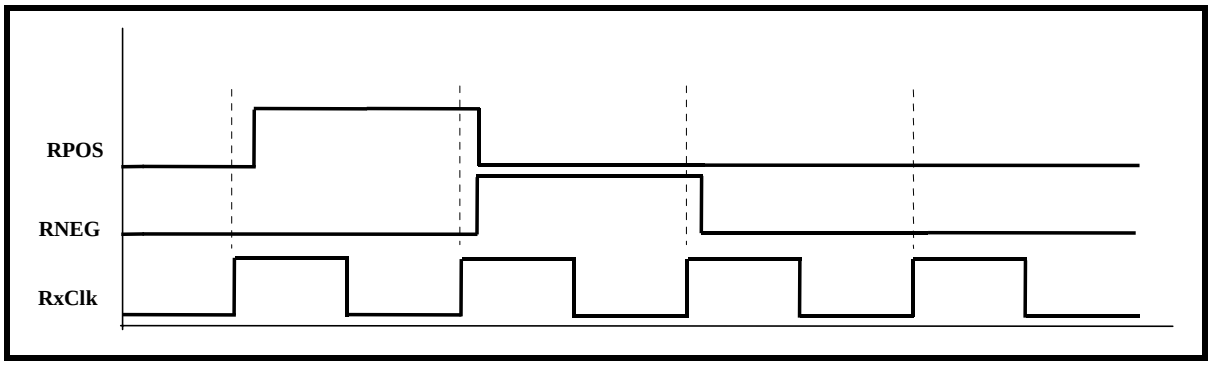
Figure 25 illustrates the typical interface for the transmission of data in a Dual-Rail Format from the Receive Section of a channel to the Receiving Terminal Equipment

FIGURE 25. THE TYPICAL INTERFACE FOR THE TRANSMISSION OF DATA IN A DUAL-RAIL FORMAT FROM THE RECEIVE SECTION OF THE XRT73L02A TO THE RECEIVING TERMINAL EQUIPMENT



The manner that a given channel transmits Dual-Rail data to the Receiving Terminal Equipment is described below and illustrated in Figure 26. Each Channel (n) of the XRT73L02A typically updates the data on the RPOS_(n) and RNEG_(n) output pins on the rising edge of RxClk_(n).

FIGURE 26. HOW THE XRT73L02A OUTPUTS DATA ON THE RPOS AND RNEG OUTPUT PINS



RxClk_(n) is the Recovered Clock signal from the incoming Received line signal. As a result, these clock signals are typically 34.368 MHz for E3 applications, 44.736 MHz for DS3 applications and 51.84 MHz for SONET STS-1 applications.

In general, if a given channel received a positive-polarity pulse in the incoming line signal via the RTIP_(n) and RRing_(n) input pins, then the channel pulses its corresponding RPOS_(n) output pin "High". If the channel received a negative-polarity pulse in the incoming line signal via the RTIP_(n) and RRing_(n) input pins, then the Channel (n) pulses its corresponding RNEG_(n) output pin "High".

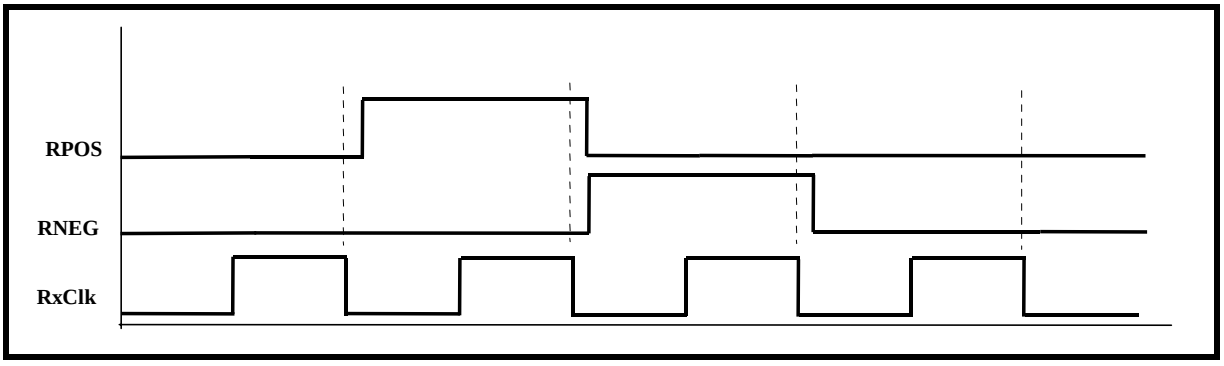
Inverting the RxClk_(n) outputs

Both channels can invert the RxClk_(n) signals with respect to the delivery of the RPOS_(n) and RNEG_(n) output data to the Receiving Terminal Equipment. This feature may be useful for those customers whose Receiving Terminal Equipment is designed such that the RPOS_(n) and RNEG_(n) data must be sampled on the rising edge of RxClk_(n). Figure 27 illustrates the behavior of the RPOS_(n), RNEG_(n) and RxClk_(n) signals when the RxClk_(n) signal has been inverted.

a. Operating in the Hardware Mode

Setting the RxClkINV pin “High” results in all channels of the XRT73L02A to output the recovered data on RPOS_(n) and RNEG_(n) on the falling edge of RxClk_(n). Setting this pin “Low” results in the recovered data on RPOS_(n) and RNEG_(n) to output on the rising edge of RxClk_(n).

FIGURE 27. THE BEHAVIOR OF THE RPOS, RNEG AND RXCLK SIGNALS WHEN RXCLK IS INVERTED



b. Operating in the HOST Mode

In order to configure a channel of the XRT73L02A to invert the RxClk_(n) output signal, the XRT73L02A must be operating in the HOST Mode.

To invert RxClk_(n) associated with Channel (n), write a "1" into the RxClk_(n)INV bit-field in Command Register CR-3 as illustrated below.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
SR/(DR)_(n)	LOSMUT_(n)	RxOFF_(n)	RxClk_(n)INV	Reserved
X	X	X	1	X

Inverting the RxClk_(n) signals via the Hardware Mode

Setting the RxClkINV input pin “High" inverts all the RxClk_(n) output signals.

3.7.2 Routing Single-Rail Format (Binary Data Stream) data to the Receive Terminal Equipment

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
SR/(DR)_(n)	LOSMUT_(n)	RxOFF_(n)	RxClk_(n)INV	Reserved
1	X	X	X	X

The configured channel outputs Single-Rail data to the Receiving Terminal Equipment via its corresponding RPOS_(n) and RxClk_(n) output pins as illustrated in Figure 28 and Figure 29.

b. Operating in the Hardware Mode

Configure the XRT73L02A to output Single-Rail data from the Receive Sections of all channels by pulling the SR/(DR) pin to VDD.

NOTE: When the XRT73L02A is operating in the Hardware Mode, the setting of the SR/(DR) input pin applies globally to both channels.

a. Operating in the HOST Mode

Configure Channel (n) to output Single-Rail data to the Terminal Equipment by writing a "1" into the SR/(DR)_(n) bit-field of Command Register CR3-(n).

FIGURE 28. THE TYPICAL INTERFACE FOR DATA TRANSMISSION IN A SINGLE-RAIL FORMAT FROM THE RECEIVE SECTION OF THE XRT73L02A TO THE RECEIVING TERMINAL EQUIPMENT

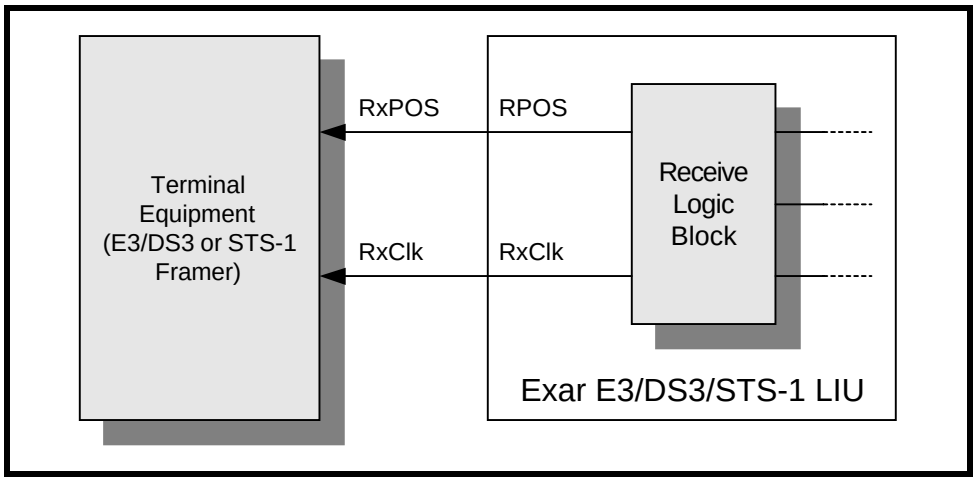
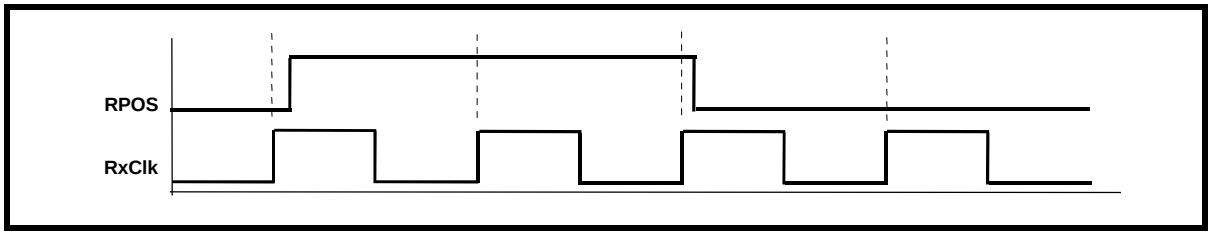


FIGURE 29. THE BEHAVIOR OF THE RPOS AND RXCLK OUTPUT SIGNALS WHILE THE XRT73L02A IS TRANSMITTING SINGLE-RAIL DATA TO THE RECEIVING TERMINAL EQUIPMENT



NOTE: The RNEG_(n) output pin is internally tied to Ground whenever this feature is implemented.

3.8 SHUTTING OFF THE RECEIVE SECTION

The Receiver Section in each channel of the XRT73L02A can be shut off. This feature may be useful in some redundant system designs. Particularly, in those designs where the Receive Termination in the Secondary LIU Line Card has been switched-out and is not receiving any traffic in parallel with the Primary Line Card. In this case, it is a waste of power if the LIU on the Secondary Line Card is consuming the normal amount of current. This feature can permit powering down the Receive Section of the LIU's on the Secondary Line Card which reduces their power consumption by approximately 80%.

a. Operating in the Hardware Mode

Shut off the Receive Section of Channel (n) by pulling the RxOFF_(n) input pin "High". Turn on the Receive Section of Channel (n) by pulling the RxOFF_(n) input pin to "Low".

b. Operating in the HOST Mode

Shut off the Receive Section of Channel (n) by writing a "1" into the RxOFF_(n) bit-field in Command Register CR3-(n). Turn on the Receive Section of Channel (n) by writing a "0" into the RxOFF_(n) bit-field in Command Register CR3-(n).

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
SR/($\overline{DR}$)_(n)	LOSMUT_(n)	RxOFF_(n)	RxClk_(n)INV	Reserved
X	X	1	X	X

4.0 DIAGNOSTIC FEATURES OF THE XRT73L02A

The XRT73L02A supports equipment diagnostic activities by supporting the following Loop-Back modes in each channel in the XRT73L02A:

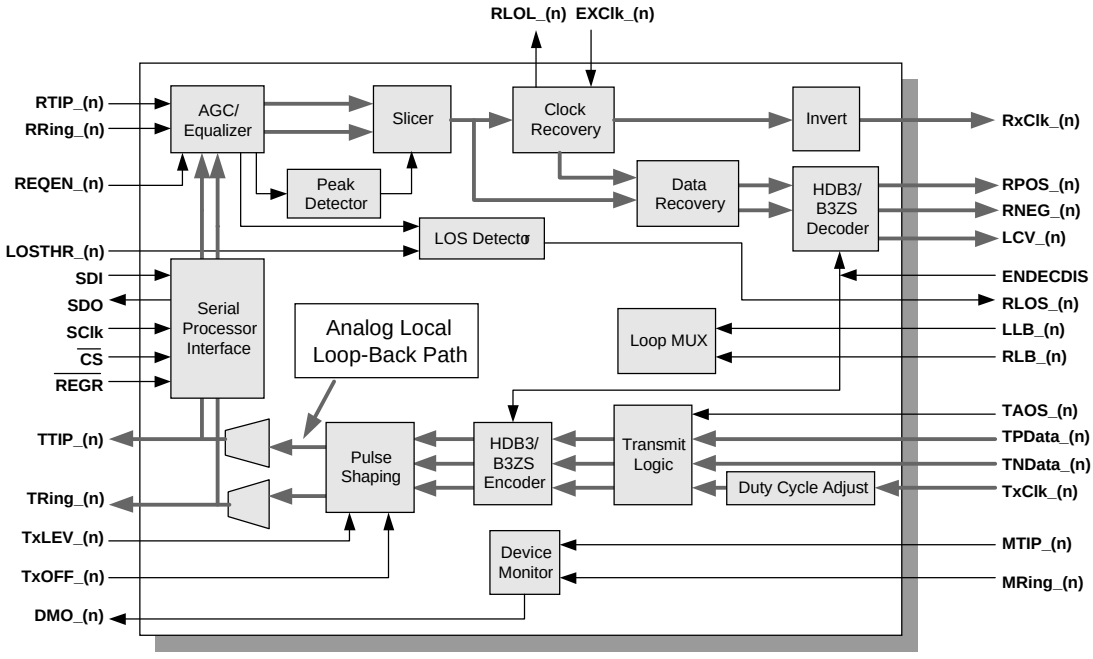
- Analog Local Loop-Back
- Digital Local Loop-Back
- Remote Loop-Back

4.1 THE ANALOG LOCAL LOOP-BACK MODE

When a given channel in the XRT73L02A is configured to operate in the Analog Local Loop-Back Mode, it ignores any signals that are input to its RTIP_(n) and RRing_(n) input pins. The Transmitting Terminal Equipment transmits clock and data into this channel via the TPData_(n), TNData_(n) and TxClk_(n) input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder. Finally, this data outputs to the line via the TTIP_(n) and TRing_(n) output pins. Additionally, this data loops back into the Attenuator/Receive Equalizer Block. This data is processed through the entire Receive Section of the channel. After this post-Loop-Back data has been processed through the Receive Section, it outputs to the Near-End Receiving Terminal Equipment via the RPOS_(n), RNEG_(n) and RxClk_(n) output pins.

Figure 30 illustrates the path the data takes in a given channel of the XRT73L02A when it is configured to operate in the Analog Local Loop-Back Mode.

FIGURE 30. A CHANNEL IN THE XRT73L02A OPERATING IN THE ANALOG LOCAL LOOP-BACK MODE



Notes:
1. (n) = 0 or 1 for respective Channels
2. Serial Processor Interface input pins are shared by the two Channels in HOST Mode and redefined in Hardware Mode.

A given channel in the XRT73L02A can be configured to operate in the Analog Local Loop-Back Mode by employing either one of the following two steps:

NOTE: *See Table 2 for a description of Command Registers and Addresses for the different channels.*

a. Operating in the HOST Mode

To configure Channel (n) to operate in the Analog Local Loop-Back Mode, write a "1" into the LLB_(n) bit-field and a "0" into the RLB_(n) bit-field in Command Register CR4.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{DS3}$_ Ch_(n)	E3_ Ch_(n)	LLB_(n)	RLB_(n)
X	X	X	1	0

b. Operating in the Hardware Mode

To configure Channel (n) to operate in the Analog Local Loop-Back Mode, set the LLB_(n) input pin “High" and the RLB_(n) input pin “Low".

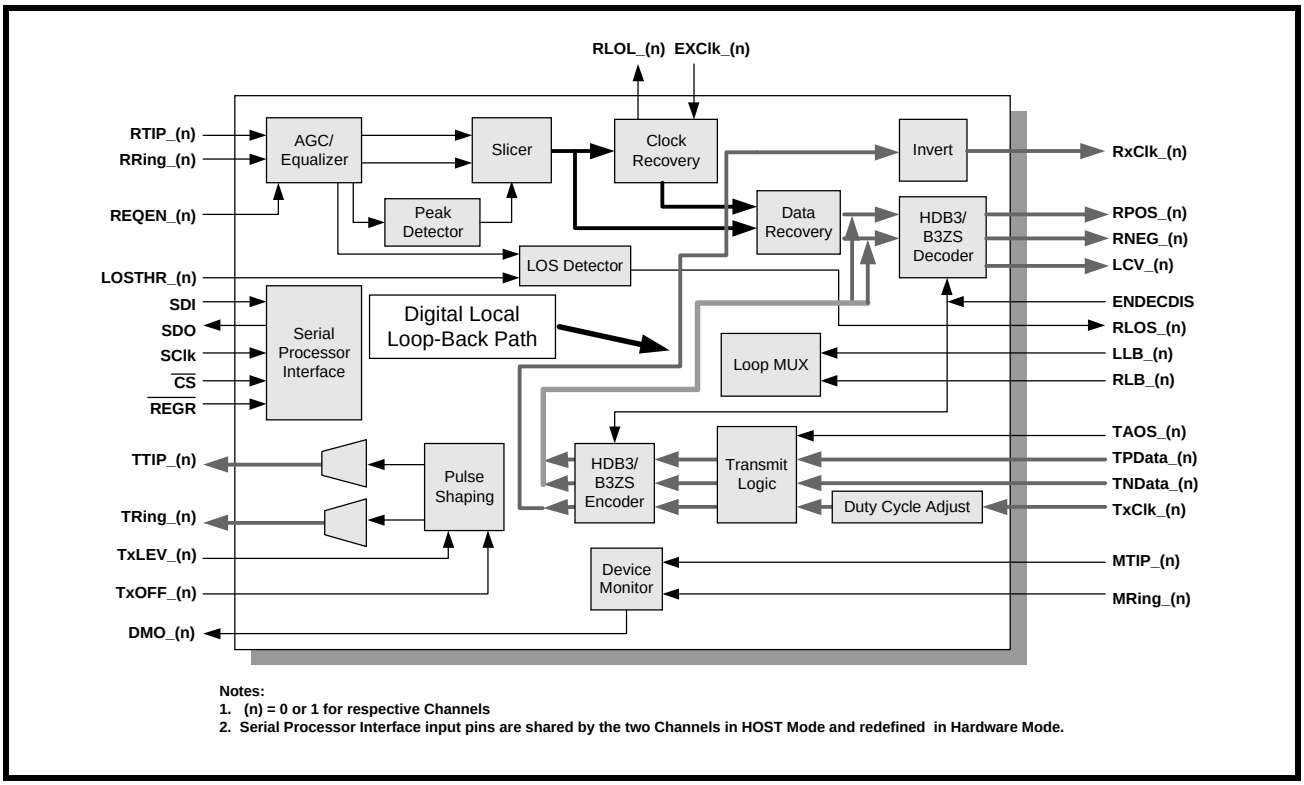
NOTE: *The Analog Local Loop-Back mode does not work if the transmitter is turned off via the TxOFF feature.*

4.2 THE DIGITAL LOCAL LOOP-BACK MODE.

When a given channel in the XRT73L02A is configured to operate in the Digital Local Loop-Back Mode, the channel ignores any signals that are input to the RTIP and RRing input pins. The Transmitting Terminal Equipment transmits clock and data into the XRT73L02A via the TPData, TNData and TxClk input pins. This data is processed through the Transmit Clock Duty Cycle Adjust PLL and the HDB3/B3ZS Encoder block. At this point, this data loops back to the HDB3/B3ZS Decoder block. After this post-Loop-Back data has been processed through the HDB3/B3ZS Decoder block, it outputs to the Near-End Receiving Terminal Equipment via the RPOS, RNEG and RxClk output pins.

Figure 31 illustrates the path the data takes in the XRT73L02A when the chip is configured to operate in the Digital Local Loop-Back Mode.

FIGURE 31. THE DIGITAL LOCAL LOOP-BACK PATH IN A GIVEN CHANNEL OF THE XRT73L02A



Notes:
1. (n) = 0 or 1 for respective Channels
2. Serial Processor Interface input pins are shared by the two Channels in HOST Mode and redefined in Hardware Mode.

To configure a channel to operate in the Digital Local Loop-Back Mode, employ either one of the following two-steps:

a. Operating in the HOST Mode

To configure Channel (n), write a “1" into both the LLB and RLB bit-fields in Command Register CR4-(n).

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{\text{DS3}}$_Ch_(n)	E3_Ch_(n)	LLB_(n)	RLB_(n)
X	X	X	1	1

b. Operating in the Hardware Mode

To configure Channel (n), pull both the LLB input pin and the RLB input pin “High".

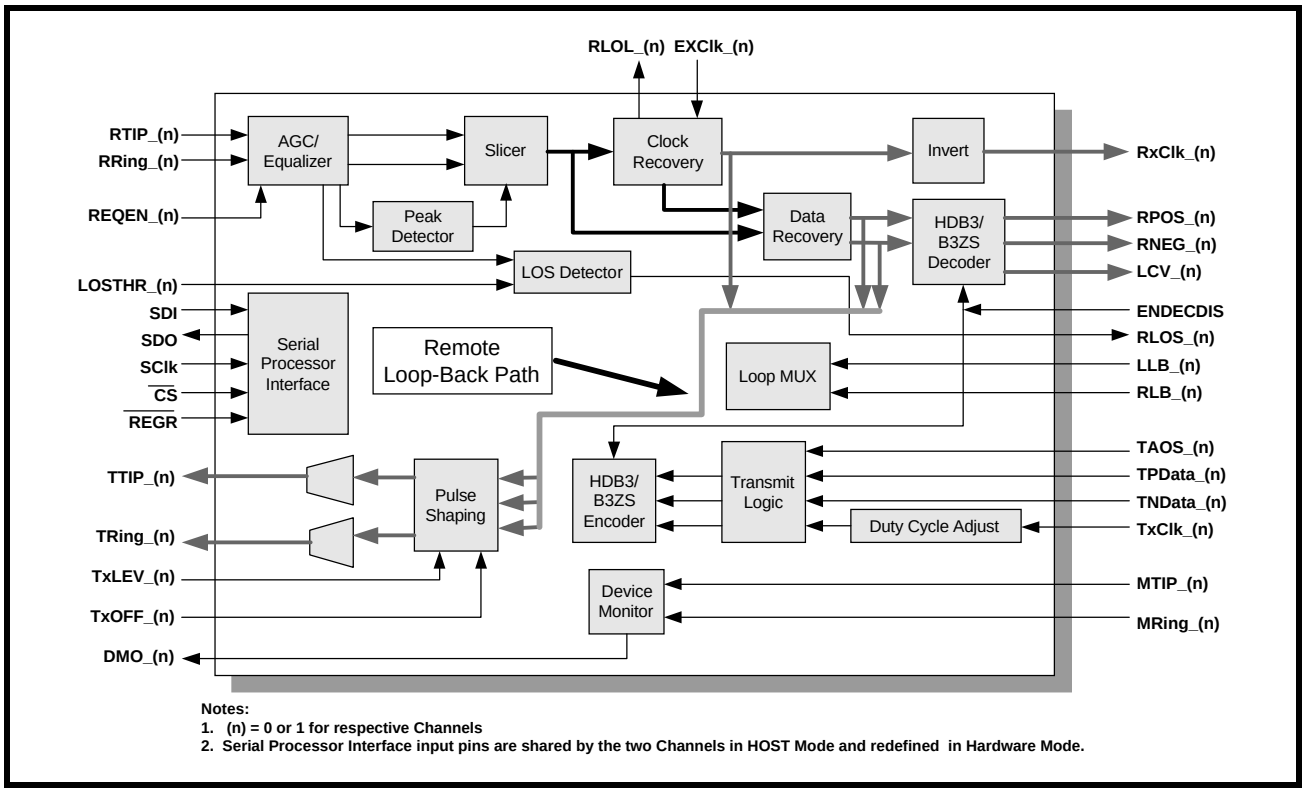
NOTE: *The Digital Local Loop-Back mode works even if the transmitter is turned off via the TxOFF feature.*

4.3 THE REMOTE LOOP-BACK MODE

When a given channel of the XRT73L02A is configured to operate in the Remote Loop-Back Mode, the channel ignores any signals that are input to the TPData and TNData input pins. The channel receives the incoming line signal via the RTIP and RRing input pins. This data is processed through the entire Receive Section of the channel and outputs to the Receive Terminal Equipment via the RPOS, RNEG and RxClk output pins. Additionally, this data is internally looped back into the Pulse-Shaping block in the Transmit Section. At this point, this data is routed through the remainder of the Transmit Section of the channel and transmitted out onto the line via the TTIP_(n) and TRing_(n) output pins.

Figure 32 illustrates the path the data takes in the XRT73L02A when the chip is configured to operate in the Remote Loop-Back Mode.

FIGURE 32. THE REMOTE LOOP-BACK PATH IN A GIVEN XRT73L02A CHANNEL



Notes:
1. (n) = 0 or 1 for respective Channels
2. Serial Processor Interface input pins are shared by the two Channels in HOST Mode and redefined in Hardware Mode.

To configure a channel to operate in the Remote Loop-Back Mode employ either one of the following two steps

a. Operating in the HOST Mode

To configure Channel (n), write a "1" into the RLB bit-field and a "0" into the LLB bit-field in Command Register CR4.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
X	STS-1/$\overline{\text{DS3}}$_Ch_(n)	E3_Ch_(n)	LLB_(n)	RLB_(n)
X	X	X	0	1

b. Operating in the Hardware Mode

To configure Channel (n), pull both the RLB input pin to “High" and the LLB input pin to "Low".

4.4 TXOFF FEATURES

The Transmit Section of each Channel in the XRT73L02A can be shut off. When this feature is invoked, the Transmit Section of the configured channel is shut-off and the Transmit Output signals TTIP_(n) and TRing_(n) are tri-stated. This feature is useful for system redundancy conditions or during diagnostic testing.

a. Operating in the Hardware Mode

Shut off the Channel (n) Transmit Driver by toggling the TxOFF_(n) input pin "High". Turn on the Transmit Driver by toggling the TxOFF_(n) input pin "Low".

b. Operating in the HOST Mode

Turn off the Channel (n) Transmit Driver by setting the TxOFF_(n) bit-field in Command Register CR1-(n) to "1".

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	TxBIN_(n)
1	X	X	X	X

Writing a "0" into this bit-field enables the Channel (n) Transmit Driver.

NOTE: *In order to permit a system designed for redundancy to quickly shut-off a defective line card and turn-on the back-up line card, the XRT73L02A was designed such that either Transmitter can quickly be turned-on or turned-off by toggling the TxOFF_(n) input pins. This approach is much quicker then setting the TxOFF_(n) bit-fields via the Microprocessor Serial Interface.*

Table 6 presents a Truth Table which relates the setting of the TxOFF external pin and bit-field for a channel to the state of the Transmitter. This table applies to both Channels of the XRT73L02A.

TABLE 6: THE RELATIONSHIP BETWEEN THE TXOFF INPUT PIN, THE TXOFF BIT FIELD AND THE STATE OF THE TRANSMITTER

STATE OF THE TXOFF INPUT PIN	STATE OF THE TXOFF BIT FIELD	STATE OF THE TRANSMITTER
LOW	0	ON (Transmitter is Active)
LOW	1	OFF (Transmitter is Tri-Stated)
HIGH	0	OFF (Transmitter is Tri-Stated)
HIGH	1	OFF (Transmitter is Tri-Stated)

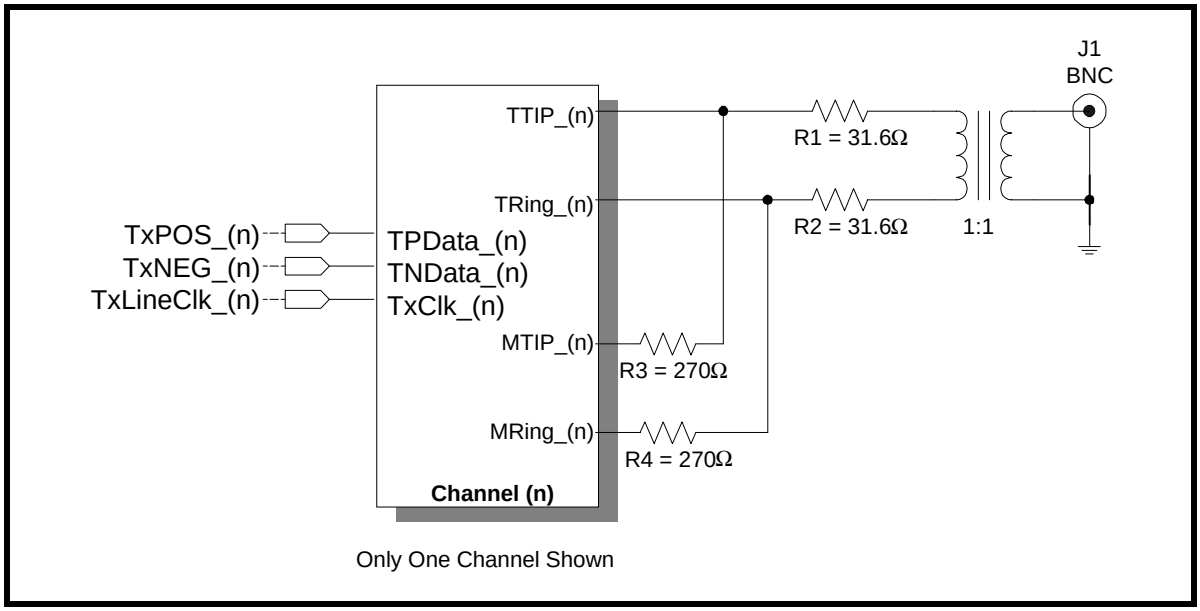
To control the state of each transmitter via the Microprocessor Serial interface, connect the TxOFF_(n) input pins to GND.

4.5 THE TRANSMIT DRIVE MONITOR FEATURES

The Transmit Drive Monitor is used to monitor the line in the Transmit Direction for the occurrence of fault conditions such as a short circuit on the line, a defective Transmit Drive in the XRT73L02A or another LIU.

Activate the Channel (n) Transmit Drive Monitor by connecting the MTIP_(n) pin to the TTIP_(n) line through a 270 Ohm resistor connected in series, and connecting the MRing_(n) pin to the TRing_(n) line through a 270 Ohm resistor connected in series. Such an approach is illustrated in Figure 33.

FIGURE 33. THE XRT73L02A EMPLOYING THE TRANSMIT DRIVE MONITOR FEATURES



When the Transmit Drive Monitor circuitry in a given line is connected to the line as illustrated in Figure 33, then it monitors the line for transitions. As long as the Transmit Drive Monitor circuitry detects transitions on the line via the MTIP_(n) and MRing_(n) pins, it keeps the DMO (Drive Monitor Output) signal "Low". However, if the Transmit Drive Monitor circuit detects no transitions on the line for 128±32 TxClk periods, the DMO (Drive Monitor Output) signal toggles "High".

NOTE: *The Transmit Drive Monitor circuit does not have to be used to operate the Transmit Section of the XRT73L02A. This is purely a diagnostic feature.*

4.6 THE TAOS (TRANSMIT ALL ONES) FEATURE

The XRT73L02A can command any channel to transmit an all “1’s” pattern onto the line by toggling a single input pin or by setting a single bit-field in one of the Command Registers to "1".

NOTE: *When this feature is activated, the Transmit Section of the configured channel in the XRT73L02A overwrites the Terminal Equipment data with an all “1’s” pattern.*

a. Operating in the Hardware Mode

Configure Channel (n) to transmit an all “1’s” pattern by toggling the TAOS_(n) input pin “High". Terminate the all “1’s” pattern by toggling the TAOS_(n) input pin "Low".

b. Operating in the HOST Mode

Configure Channel (n) to transmit an all “1’s” pattern by writing to Command Register CR1-(n) and setting the TAOS_(n) bit-field (D3) to "1".

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	TxBIN_(n)
0	1	X	X	X

Terminate the all “1’s” pattern by writing to Command Register CR1-(n) and setting the TAOS_(n) bit-field (D3) to "0".

5.0 THE MICROPROCESSOR SERIAL INTERFACE

The on-chip Command Registers of XRT73L02A DS3/E3/STS-1 Line Interface Unit IC are used to configure the XRT73L02A into a wide-variety of modes. This section discusses the following:

1. The description of the Command Registers.
2. A description on how to use the Microprocessor Serial Interface.

5.1 DESCRIPTION OF THE COMMAND REGISTERS

Table 7 lists the Command Registers, their Addresses and their bit-formats.

TABLE 7: ADDRESSES AND BIT FORMATS OF XRT73L02A COMMAND REGISTERS

			REGISTER BIT-FORMAT				
ADDRESS	COMMAND REGISTER	TYPE	D4	D3	D2	D1	D0
CHANNEL 0							
0x00	CR0-0	RO	RLOL_0	RLOS_0	ALOS_0	DLOS_0	DMO_0
0x01	CR1-0	R/W	TxOFF_0	TAOS_0	TxClkINV_0	TxLEV_0	TxBIN_0
0x02	CR2-0	R/W	Reserved	ENDECDIS_0	ALOSDIS_0	DLOSDIS_0	REQEN_0
0x03	CR3-0	R/W	SR/$\overline{DR}$_0	LOSMUT_0	RxOFF_0	RxClk_0INV	Reserved
0x04	CR4-0	R/W	Reserved	STS-1/$\overline{DS3}$_Ch_0	E3_CH_0	LLB_0	RLB_0
0x05	CR5-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7-0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
CHANNEL 1							
0x08	CR0-1	RO	RLOL_1	RLOS_1	ALOS_1	DLOS_1	DMO_1
0x09	CR1-1	R/W	TxOFF_1	TAOS_1	TxClkINV_1	TxLEV_1	TxBIN_1
0x0A	CR2-1	R/W	Reserved	ENDECDIS_1	ALOSDIS_1	DLOSDIS_1	REQEN_1
0x0B	CR3-1	R/W	SR/$\overline{DR}$_1	LOSMUT_1	RxOFF_1	RxClk_1INV	Reserved
0x0C	CR4-1	R/W	Reserved	STS-1/$\overline{DS3}$_Ch_1	E3_CH_1	LLB_1	RLB_1
0x0D	CR5-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0E	CR6-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x0F	CR7-1	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

Address

The register addresses are presented in the **Hexadecimal** format.

Type:

The Command Registers are either Read-Only (RO) or Read/Write (R/W) registers. Each channel of the XRT73L02A has eight command registers, CR0-(n) through CR7-(n) where (n) = 0 or 1. The associated addresses for each channel is presented in Table 7.

NOTE: The default value for each of the bit-fields in these registers is "0".

5.2 DESCRIPTION OF BIT-FIELDS FOR EACH COMMAND REGISTER

5.2.1 Command Register - CR0-(n)

The bit-format and default values for Command Register CR0-(n) are listed below followed by the function of these bit-fields.

COMMAND REGISTER CR0-(n)

D4	D3	D2	D1	D0
RLOL	RLOS	ALOS	DLOS	DMO
1	1	1	1	1

Bit D4 - RLOL_(n) (Receive Loss of Lock Status - Channel (n))

This Read-Only bit-field reflects the lock status of the Channel (n) Clock Recovery Phase-Locked-Loop in the XRT73L02A.

This bit-field is set to “0" if the Clock Recovery PLL is in lock with the incoming line signal. This bit-field is

set to "1" if the Clock Recovery PLL is out of lock with the incoming line signal.

Bit D3 - RLOS_(n) (Receive Loss of Signal Status - Channel (n))

This Read-Only bit-field indicates whether or not Channel (n) of the Receiver is currently declaring an LOS (Loss of Signal) Condition.

This bit-field is set to "0" if Channel (n) is NOT currently declaring the LOS Condition or, this bit-field is set to "1" if Channel (n) is declaring an LOS Condition.

Bit D2 - ALOS_(n) (Analog Loss of Signal Status - Channel (n))

This Read-Only bit-field indicates whether or not the Channel (n) Analog LOS Detector is currently declaring an LOS condition.

This bit-field is set to "0" if the Analog LOS Detector is NOT currently declaring an LOS condition. This bit-field is set to "1" if the Analog LOS Detector is currently declaring an LOS condition.

NOTE: *The purpose is to isolate the Detector (e.g., either the Analog LOS or the Digital LOS detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.*

Bit D1 - DLOS_(n) (Digital Loss of Signal Status - Channel (n))

This Read-Only bit-field indicates whether or not the Channel (n) Digital LOS Detector is currently declaring an LOS condition.

This bit-field is set to "0" if the Digital LOS Detector is NOT currently declaring an LOS condition. This bit-field is set to "1" if the Digital LOS Detector is currently declaring an LOS condition.

NOTE: *The purpose is to isolate the Detector (e.g., either the Analog LOS or the Digital LOS detector) that is declaring the LOS condition. This feature may be useful for troubleshooting/debugging purposes.*

Bit D0 - DMO_(n) (Drive Monitor Output Status - Channel (n))

This Read-Only bit-field reflects the status of the DMO output pin.

5.2.2 Command Register CR1

The bit-format and default values for Command Register CR1-(n) are listed below followed by the function of these bit-fields.

COMMAND REGISTER CR1-(n)

D4	D3	D2	D1	D0
TxOFF_(n)	TAOS_(n)	TxClkINV_(n)	TxLEV_(n)	TxBIN_(n)
0	0	0	0	0

Bit D4 - TxOFF_(n) (Transmitter OFF - Channel (n))

This Read/Write bit-field is used to turn off the Channel (n) Transmitter.

Writing a "1" to this bit field turns off the Transmitter and tri-state the Transmit Output. Writing a "0" to this bit-field turns on the Transmitter.

Bit D3 - TAOS_(n) (Transmit All OneS - Channel (n))

This Read/Write bit-field is used to command the Channel (n) Transmitter to generate and transmit an all “1’s” pattern onto the line.

Writing a "1" to this bit-field commands the Transmitter to transmit an all “1’s” pattern onto the line. Writing a "0" to this bit-field commands normal operation.

Bit D2 - TxClkINV_(n) (Transmit Clock Invert - Channel (n))

This Read/Write bit-field is used to configure the Transmitter in the XRT73L02A to sample the signal at the TPData and TNData pins on the rising edge or falling edge of TxClk (the Transmit Line Clock signal).

Writing a "1" to this bit-field configures the Transmitter to sample the TPData and TNData input pins on the rising edge of TxClk. Writing a "0" to this bit-field configures the Transmitter to sample the TPData and TNData input pins on the falling edge of TxClk.

Bit D1 - TxLEV_(n) (Transmit Line Build-Out Enable/Disable Select - Channel (n))

This Read/Write bit-field is used to enable or disable the Channel (n) Transmit Line Build-Out circuit in the XRT73L02A.

Setting this bit-field "High” disables the Channel (n) Line Build-Out circuit. In this mode, Channel (n) outputs partially-shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

Setting this bit-field "Low" enables the Channel (n) Line Build-Out circuit. In this mode, Channel (n) outputs shaped pulses onto the line via the TTIP_(n) and TRing_(n) output pins.

In order to comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements (per Bellcore GR-499-CORE or GR-253-CORE):

a. Set this bit-field to "1" if the cable length between the Cross-Connect and the transmit output of Channel (n) is greater than 225 feet.

b. Set this bit-field to "0" if the cable length between the Cross-Connect and the transmit output of Channel (n) is less than 225 feet.

NOTE: *This bit-field is active only if the XRT73L02A is configured to operate in the DS3 or SONET STS-1 Modes.*

If the cable length is greater than 225 feet, set this bit-field to "1" in order to increase the amplitude of the Transmit Output Signal. If the cable length is less than 225 feet, set this bit-field to "0".

NOTE: *This option is only available when the XRT73L02A is operating in the DS3 or STS-1 Mode.*

Bit D0 - TxBIN_(n) (Transmit Binary Data - Channel (n))

This Read/Write bit-field is used to configure the Channel (n) Transmitter to accept an un-encoded binary data stream via the TPData input and convert this data into the appropriate bipolar signal for the line.

Writing a "1" configures the Transmitter to accept a binary data stream via the TPData input. The TNData input is ignored.

This form of data acceptance is sometimes referred to as Single-Rail mode operation. The Transmitter then encodes this data into the appropriate line code (e.g., B3ZS or HDB3) prior to its transmission over the line.

Writing a "0" configures the Transmitter to accept data in a Dual-Rail manner via TPData and TNData inputs.

5.2.3 Command Register CR2-(n)

The bit-format and default values for Command Register CR2-(n) are listed below followed by the function of each of these bit-fields.

COMMAND REGISTER CR2-(n)

D4	D3	D2	D1	D0
Reserved	ENDECDIS	ALOSDIS	DLOSDIS	REQEN
X	0	0	0	0

Bit D4 - Reserved

Bit D3 - ENDECDIS (B3ZS/HDB3 Encoder/Decoder-Disable - Channel (n))

This Read/Write bit-field is used to enable or disable the Channel (n) B3ZS/HDB3 Encoder and Decoder blocks.

Writing a "1" to this bit-field disables the B3ZS/HDB3 Encoder and Decoder blocks. Writing a "0" to this bit-field enables the B3ZS/HDB3 Encoder and Decoder blocks.

NOTE: *This Encoder/Decoder performs HDB3 Encoding/Decoding if the XRT73L02A is operating in the E3 Mode. Otherwise, it performs B3ZS Encoding/Decoding.*

Bit D2 - ALOSDIS (Analog LOS Disable - Channel (n))

This Read/Write bit-field is used to enable or disable the Channel (n) Analog LOS Detector.

Writing a "0" to this bit-field enables the Analog LOS Detector. Writing a "1" to this bit-field disables the Analog LOS Detector.

NOTE: *If the Analog LOS Detector is disabled, then the RLOS input pin is only asserted by the DLOS (Digital LOS Detector).*

Bit D1 - DLOSDIS (Digital LOS Disable - Channel (n))

This Read/Write bit-field to used to enable or disable the Channel (n) Digital LOS Detector .

Writing a "0" to this bit-field enables the Digital LOS Detector. Writing a "1" to this bit-field disables the Digital LOS Detector.

NOTE: *If the Digital LOS Detector is disabled, then the RLOS input pin is only asserted by the ALOS (Analog LOS Detector).*

Bit D0 - REQEN (Receive Equalization Enable - Channel (n))

This Read/Write bit-field is used to either enable or disable the Channel (n) internal Receive Equalizer of the XRT73L02A.

Writing a "1" to this bit-field enables the Internal Equalizer. Writing a "0" to this bit-field disables the Internal Equalizer.

5.2.4 Command Register CR3-(n)

The bit-format and default values for Command Register CR3 are listed below followed by the function of these bit-fields.

COMMAND REGISTER CR3-(n)

D4	D3	D2	D1	D0
SR/$\overline{DR}$_(n)	LOSMUT_(n)	RxOFF_(n)	RxClk_(n)INV	Reserved
0	1	0	0	0

Bit D4 - SR/$\overline{DR}$_(n) (Single-Rail/Dual-Rail Data Output - Channel (n))

This Read/Write bit-field is used to configure Channel (n) in the XRT73L02A to output the received data from the Remote Terminal in a binary or Dual-Rail format.

Writing a "1" to this bit-field configures Channel (n) to output data to the Terminal Equipment in a binary Single-Rail format via the RPOS_(n) output pin. RNEG_(n) is grounded. Writing a "0" to this bit-field configures Channel (n) to output data to the Terminal Equipment in a Dual-Rail format via both the RPOS_(n) and RNEG_(n) output pins.

Bit D3 - LOSMUT_(n) (Recovered Data Muting during LOS Condition - Channel (n))

This Read/Write bit-field is used to configure Channel (n) in the XRT73L02A to NOT output any recovered data from the line while it is declaring an LOS condition.

Writing a "0" to this bit-field configures the chip to output recovered data even while the XRT73L02A is declaring an LOS condition. Writing a "1" to this bit-field configures the chip to NOT output the recovered data while an LOS condition is being declared.

NOTE: *In this mode, RPOS_(n) and RNEG_(n) is set to "0" asynchronously.*

Bit D2 - RxOFF_(n) (Receive Section - Shut OFF Select)

This Read/Write bit-field is used to shut-off the Receive Section of Channel (n) in the XRT73L02A. The purpose of this feature is to permit conservation of power consumption when this is the back-up device in a Redundancy System.

Writing a "1" into this bit-field shuts off the Receive Section of Channel (n). Writing a "0" into this bit-field turns on the Receive Section of Channel (n).

Bit D1 - RxClk_(n)INV (Invert RxClk_(n))

This Read/Write bit-field is used to configure the Receiver of Channel (n) of the XRT73L02A) to output the recovered data on either the rising edge or the falling edge of the RxClk_(n) clock signal.

Writing a "0" to this bit-field configures the Receiver to output the recovered data on the rising edge of the RxClk_(n) output signal. Writing a "1" to this bit-field configures the Receiver to output the recovered data on the falling edge of the RxClk_(n) output signal.

Bit D0 - Reserved

This bit-field has no defined functionality.

Command Register CR4-(n)

The bit-format and default values for Command Register CR4 are listed below followed by the function of each of these bit fields.

COMMAND REGISTER CR4-(n)

D4	D3	D2	D1	D0
Reserved	STS-1/$\overline{\text{DS3}}$_ Ch_(n)	E3_Ch_(n)	LLB_(n)	RLB_(n)
0	0	0	0	0

Bit D4 - Reserved

This bit-field has no defined functionality.

Bit D3 - STS-1/($\overline{DS3}$_(n)) - Channel (n) - Mode Select

This Read/Write bit field is used to configure Channel (n) to operate in either the SONET STS-1 Mode or the DS3 Mode.

Writing a "0" into this bit-field configures Channel (n) to operate in the DS3 Mode. Writing a "1" into this bit-field configures Channel (n) to operate in the SONET STS-1 Mode.

NOTE: *This bit-field is ignored if the E3_Ch_(n) bit-field (e.g., D2 in this Command Register) is set to "1".*

Bit D2 - E3 Mode Select - Channel (n)

This Read/Write bit-field is used to configure Channel (n) to operate in the E3 Mode.

Writing a "0" into this bit-field configures Channel (n) to operate in either the DS3 or SONET STS-1 Mode as specified by the setting of the DS3 bit-field in this Command Register. Writing a "1" into this bit-field configures Channel (n) to operate in the E3 Mode.

Bit D1 - LLB_(n) (Local Loop-Back - Channel (n))

This Read/Write bit-field along with RLB_(n) is used to configure Channel (n) to operate in any one of a variety of Loop-Back modes.

Table 8 relates the contents of LLB_(n) and RLB_(n) and the corresponding Loop-Back mode for Channel (n).

Bit D0 - RLB_(n) (Remote Loop-Back - Channel (n))

This Read/Write bit-field along with LLB_(n) is used to configure Channel (n) to operate in any one of a variety of Loop-Back modes.

Table 8 relates the contents of LLB_(n) and RLB_(n) and the corresponding Loop-Back mode for Channel (n).

TABLE 8: CONTENTS OF LLB_(n) AND RLB_(n) AND THE CORRESPONDING LOOP-BACK MODE FOR CHANNEL (n)

LLB_(n)	RLB_(n)	LOOP-BACK MODE (FOR CHANNEL (n))
0	0	None
1	0	Analog Loop-Back Mode (See Section 4.1 for Details)
1	1	Digital Loop-Back Mode (See Section 4.2 for Details)
0	1	Remote Loop-Back Mode (See Section 4.3 for Details)

5.3 OPERATING THE MICROPROCESSOR SERIAL INTERFACE.

The XRT73L02A Serial Interface is a simple four wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

- $\overline{CS}$ - Chip Select (Active Low)
- SClk - Serial Clock
- SDI - Serial Data Input
- SDO - Serial Data Output

Using the Microprocessor Serial Interface

The following instructions for using the Microprocessor Serial Interface are best understood by referring to the diagram in Figure 34 and the timing diagram in Figure 35.

In order to use the Microprocessor Serial Interface, a clock signal must be first applied to the SClk input pin. Then, initiate a Read or Write operation by asserting the active-low Chip Select input pin $\overline{CS}$. It is important to assert the $\overline{CS}$ pin (e.g., toggle it “Low") at least 50ns prior to the very first rising edge of the clock signal.

Once the $\overline{CS}$ input pin has been asserted, the type of operation and the target register address must now be specified. Provide this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input.

NOTE: *Each of these bits is clocked into the SDI input on the rising edge of SClk.*

Bit 1- R/W (Read/Write) Bit

This bit is clocked into the SDI input on the first rising edge of SClk after $\overline{CS}$ has been asserted. This bit indicates whether the current operation is a Read or Write operation. A "1" in this bit specifies a Read operation, a "0" in this bit specifies a Write operation.

Bits 2 through 5: The four (4) bit Address Values (labeled A0, A1, A2 and A3)

The next four rising edges of the SClk signal clocks in the 4-bit address value for this particular Read or Write operation. The address selects the Command Register in the XRT73L02A that the user either be reading data from or writing data to. The address bits must be applied to the SDI input pin in ascending order with the LSB (least significant bit) first.

Bit 6 and 7:

A4 and A5 must be set to "0" as shown in Figure 34.

Bit 8 - A6:

The value of "A6" is a don't care.

Once these first 8 bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a Read or Write operation.

Read Operation

Once the last address bit (A3) has been clocked into the SDI input, the Read operation proceeds through an idle period lasting three SClk periods. On the falling edge of SClk Cycle #8 (see Figure 34) the serial data output signal (SDO) becomes active. At this point, reading the data contents of the addressed Command Register at Address [A3, A2, A1, A0] via the SDO output pin can begin. The Microprocessor Serial Interface outputs this five bit data word (D0 through D4) in ascending order with the LSB first, on the falling edges of the SClk pin. Consequently, the data on the SDO output pin is sufficiently stable for reading by the Microprocessor on the very next rising edge of the SClk pin.

Write Operation

Once the last address bit (A3) has been clocked into the SDI input, the Write operation proceeds through an idle period lasting three SClk periods. Prior to the rising edge of SClk Cycle # 9 (see Figure 34). Apply the desired eight bit data word to the SDI input pin via the Microprocessor Serial Interface. The Microprocessor Serial Interface latches the value on the SDI input pin on the rising edge of SClk. Apply this word (D0 through D7) serially, in ascending order with the LSB first.

Simplified Interface Option

The design of the circuitry connecting to the Microprocessor Serial Interface can be simplified by tying both the SDO and SDI pins together and reading data from and/or writing data to this combined signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal is tri-stated.

NOTES:

1. *A4 and A5 is always "0"*
2. *R/W = "1" for "Read" Operations*
3. *R/W = "0" for "Write" Operations*
4. *Shaded blocks denotes a "don't care" value*

FIGURE 34. MICROPROCESSOR SERIAL INTERFACE DATA STRUCTURE

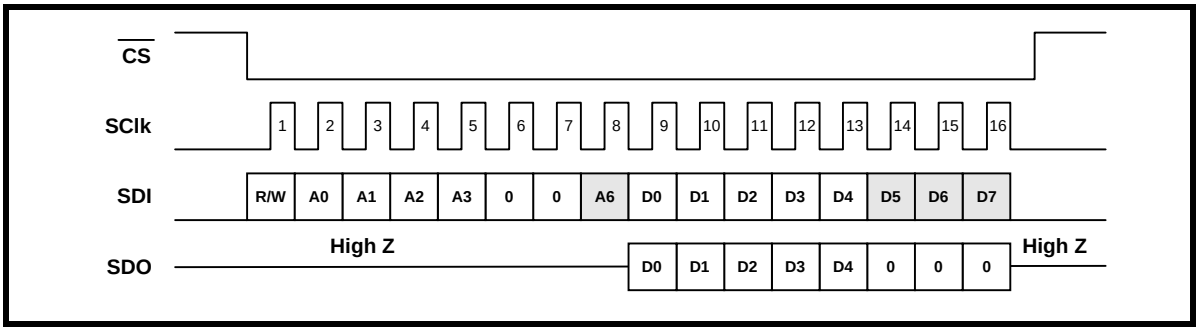
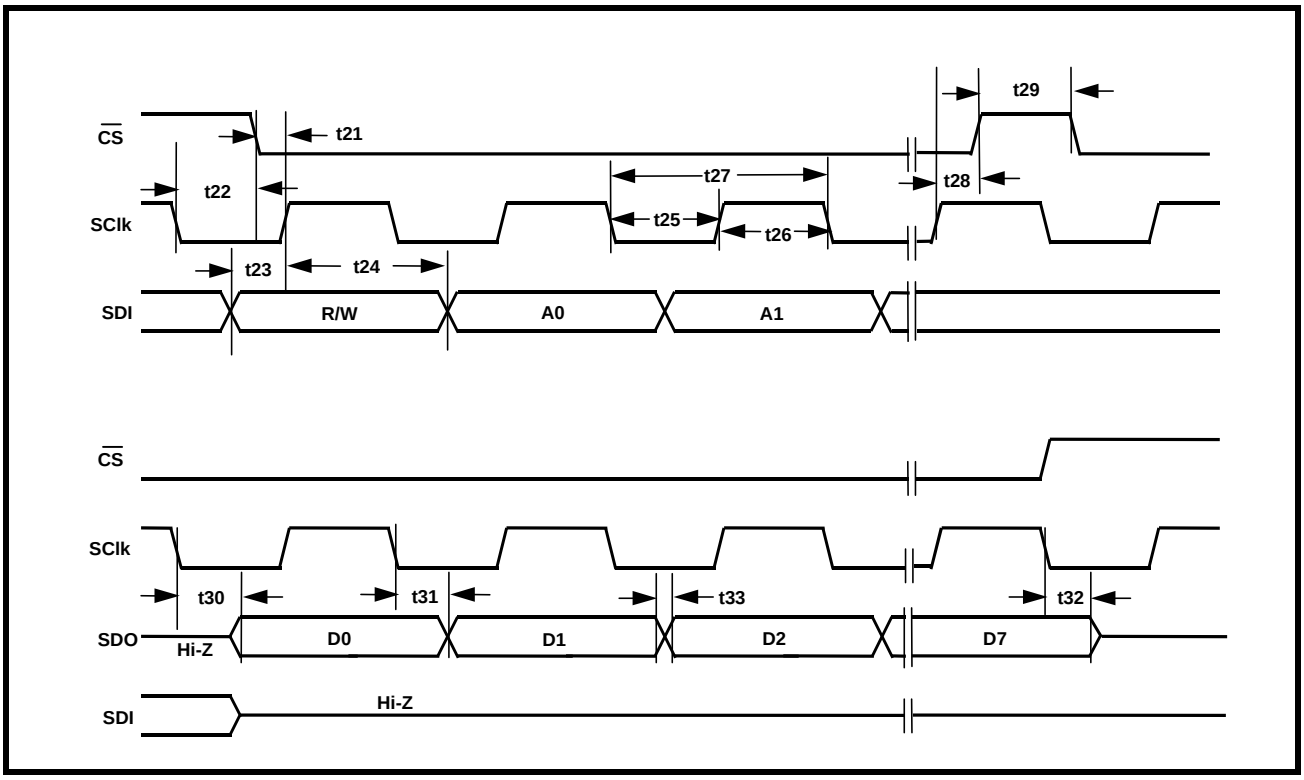


FIGURE 35. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

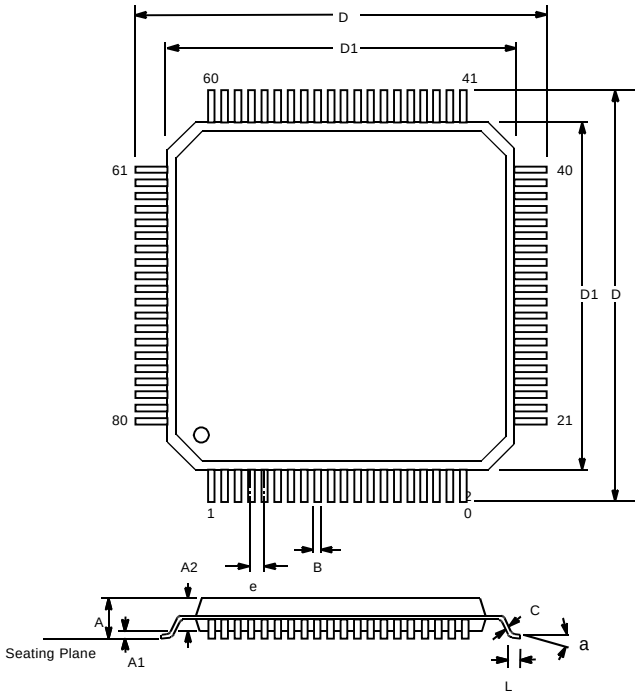


ORDERING INFORMATION

PART #	PACKAGE	OPERATING TEMPERATURE RANGE
XRT73L02AIV	80 Pin TQFP	-40°C to +85°C
Thermal Information	Theta - J_A = 23° C/W	Theta J_C = 5.32° C/W

PACKAGE DIMENSIONS

80 LEAD THIN QUAD FLAT PACK
(14 x 14 x 1.4 mm) TQFP



NOTE: *The control dimension is the millimeter column*

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.009	0.015	0.22	0.38
C	0.004	0.008	0.09	0.20
D	0.622	0.638	15.80	16.20
D_1	0.547	0.555	13.90	14.10
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
a	0°	7°	0°	7°

REVISION HISTORY

P1.1.1 Removed heat slug from package drawing.

P1.1.2 Removed note referencing heat slug in the electrical characteristics (page 14).

2.0.0 Redesigned 73L02 with improved performance and added timing recovery circuit. Added typical Jitter tolerance @800kHz. Receiver Sensitivity (cable length) increased. Part Number changed to XRT73L02A, ordering information changed to XRT73L02AIV. Updated “Transformer Recommendations”. Removed preliminary designation.

NOTICE