

## DS92LX1621/DS92LX1622 10 - 50 MHz DC-Balanced Channel Link III Serializer and Deserializer with Bi-Directional Control Channel

Check for Samples: [DS92LX1621](#), [DS92LX1622](#)

### FEATURES

- Configurable Data Throughput
  - 12-bit (min) up to 600 Mbits/sec
  - 16-bit (def) up to 800 Mbits/sec
  - 18-bit (max) up to 900 Mbits/sec
- 10 MHz to 50 MHz Input Clock Support
- Embedded Clock with DC Balanced Coding to Support AC-Coupled Interconnects
- Capable to Drive up to 10 Meters Shielded Twisted-Pair
- Bi-Directional Control Interface Channel with I<sup>2</sup>C Support
- I<sup>2</sup>C Interface for Device Configuration. Single-pin ID Addressing
- 16-bit Data Payload with CRC (Cyclic Redundancy Check) for Checking Data Integrity with Programmable Data Transmission Error Detection and Interrupt Control
- Up to 6 Programmable GPIO's
- AT-SPEED BIST Diagnosis Feature to Validate Link Integrity
- Individual Power-Down Controls for Both SER and DES
- User-Selectable Clock Edge for Parallel Data on Both SER and DES
- Integrated Termination Resistors
- 1.8V- or 3.3V-Compatible Parallel Bus Interface
- Single Power Supply at 1.8V
- IEC 61000-4-2 ESD Compliant
- No Reference Clock Required on Deserializer
- Programmable Receive Equalization
- LOCK Output Reporting Pin to Ensure Link Status
- EMI/EMC Mitigation
  - DES Programmable Spread Spectrum (SSCG) Outputs
  - DES Receiver Staggered Outputs
- Temperature Range –40°C to +85°C

- SER Package: 32 Pin WQFN (5mm x 5mm)
- DES Package: 40 Pin WQFN (6mm x 6mm)

### APPLICATIONS

- Industrial Displays, Touch Screens
- Medical Imaging

### DESCRIPTION

The DS92LX1621 / DS92LX1622 chipset offers a Channel Link III interface with a high-speed forward channel and a full-duplex back channel for data transmission over a single differential pair. The Serializer/Deserializer pair is targeted for direct connections between automotive camera systems and Host Controller/Electronic Control Unit (ECU). The primary transport sends 16 bits of image data over a single high-speed serial stream together with a low latency bi-directional control channel transport that supports I<sup>2</sup>C. Included with the 16-bit payload is a selectable data integrity option for CRC (Cyclic Redundancy Check) or parity bit to monitor transmission link errors. Using TI's embedded clock technology allows transparent full-duplex communication over a single differential pair, carrying asymmetrical bi-directional control information without the dependency of video blanking intervals. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating the skew problems between parallel data and clock paths. This significantly saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

In addition, the Deserializer inputs provide equalization control to compensate for loss from the media over longer distances. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects.

The sleep function provides a power-savings mode and a remote wake up interrupt for signaling of a remote device.

The Serializer is offered in a 32-pin WQFN package, and Deserializer is offered in a 40-pin WQFN package.



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## Typical Application Diagram

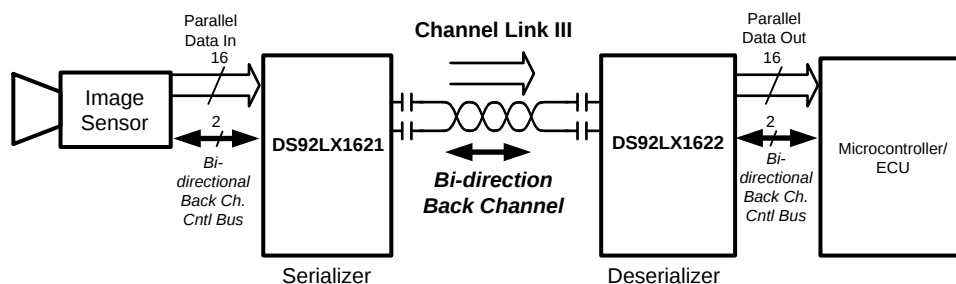


Figure 1. Typical Application Circuit

## Block Diagrams

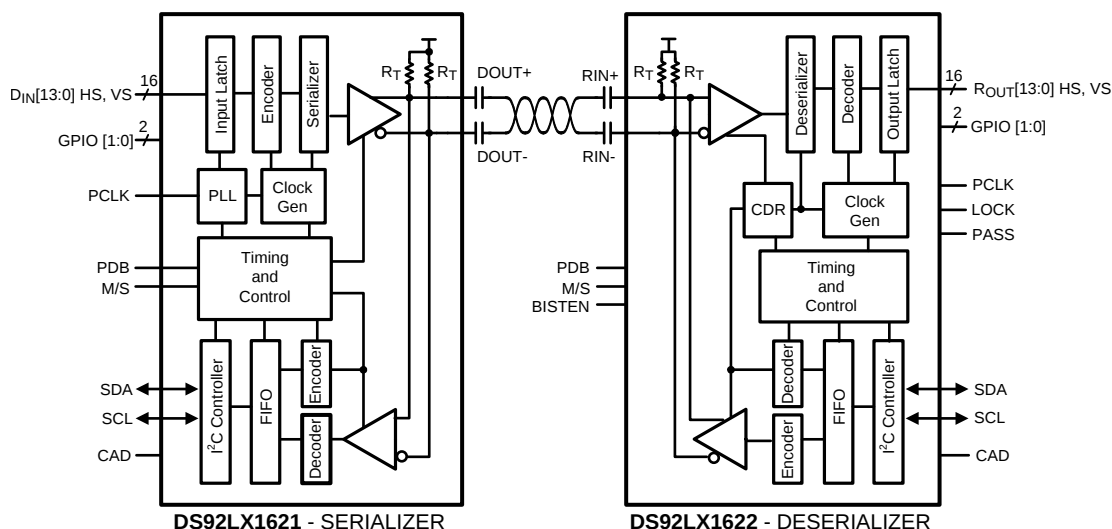


Figure 2. Block Diagram

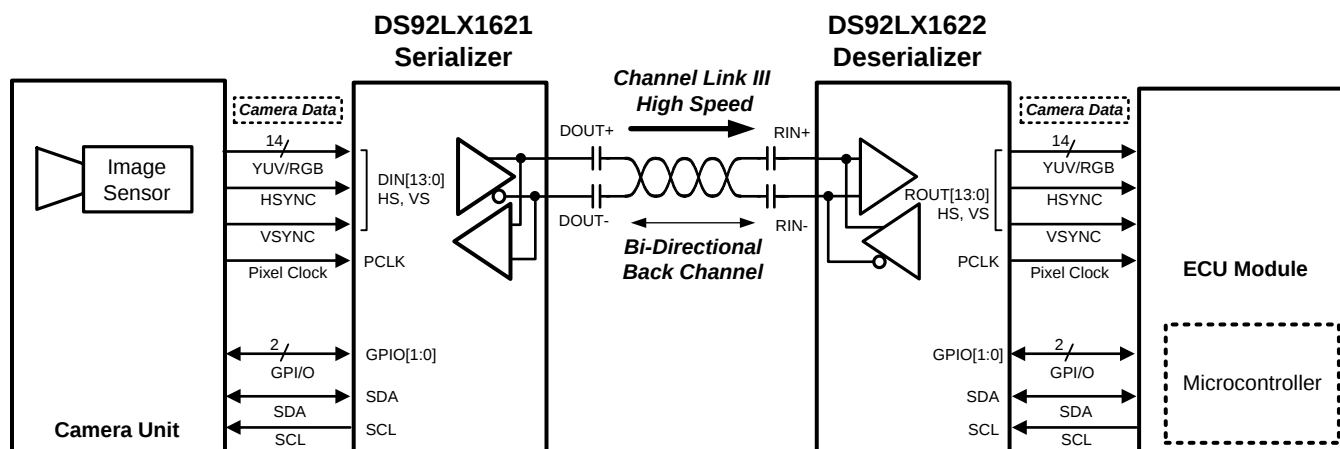
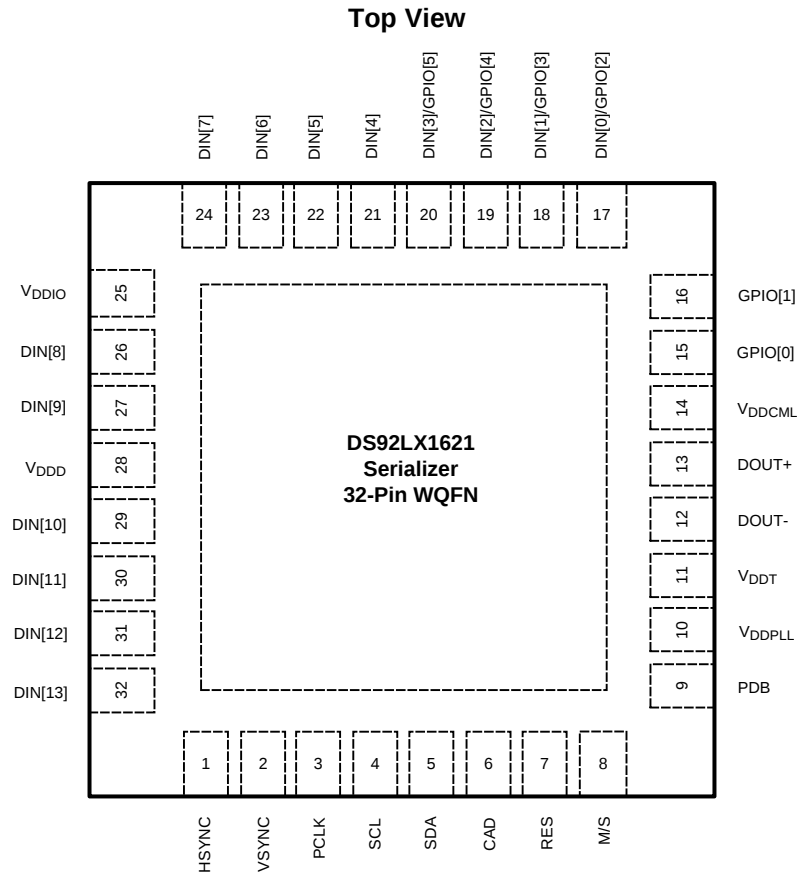


Figure 3. Application Block Diagram

## DS92LX1621 Pin Diagram



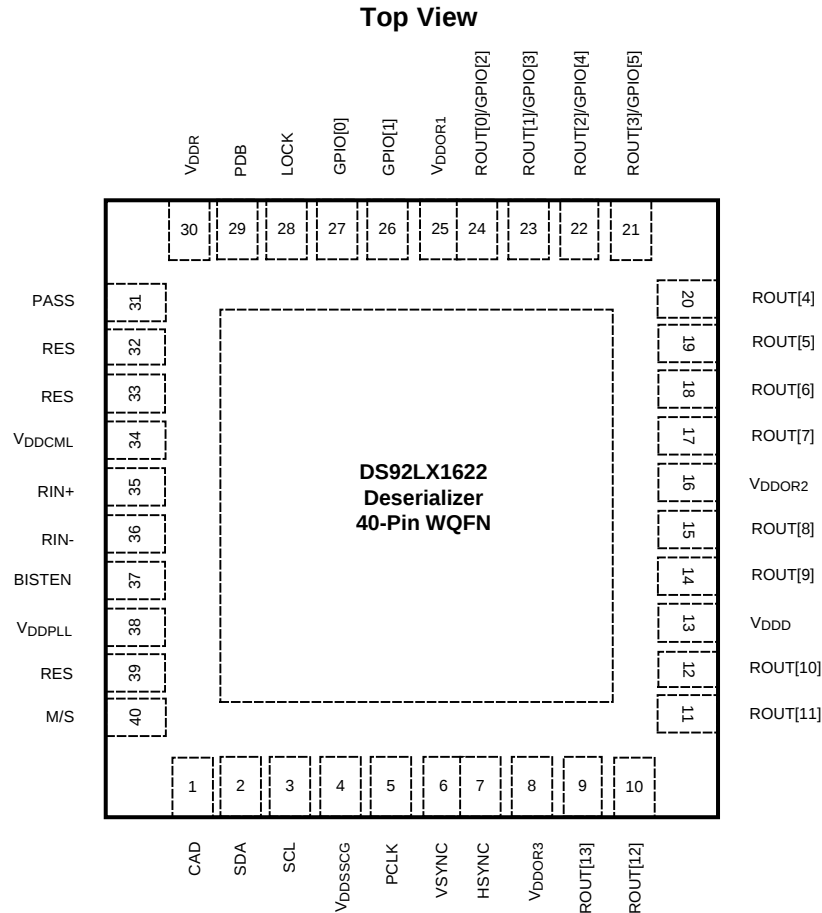
**Figure 4. Serializer - DS92LX1621  
32-Pin WQFN (RTV Package)**

### DS92LX1621 Serializer PIN DESCRIPTIONS

| Pin Name                                   | Pin No.                                                | I/O, Type                    | Description                                                                                                                                |
|--------------------------------------------|--------------------------------------------------------|------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|
| <b>LVC MOS PARALLEL INTERFACE</b>          |                                                        |                              |                                                                                                                                            |
| DIN[13:0]                                  | 32, 31, 30, 29, 27, 26, 24, 23, 22, 21, 20, 19, 18, 17 | Inputs, LVC MOS w/ pull down | Parallel data inputs.                                                                                                                      |
| HSYNC                                      | 1                                                      | Inputs, LVC MOS w/ pull down | Parallel data input 14, typically used as Horizontal SYNC Input                                                                            |
| VSYNC                                      | 2                                                      | Inputs, LVC MOS w/ pull down | Parallel data input 15, typically used as Vertical SYNC Input                                                                              |
| PCLK                                       | 3                                                      | Input, LVC MOS w/ pull down  | Pixel Clock Input Pin. Strobe edge set by TRFB control register.                                                                           |
| <b>GENERAL PURPOSE INPUT OUTPUT (GPIO)</b> |                                                        |                              |                                                                                                                                            |
| DIN[3:0]/GPIO[5:2]                         | 20, 19, 18, 17                                         | Input/Output, Digital        | DIN[3:0] general-purpose pins can be individually configured as either inputs or outputs; used to control and respond to various commands. |
| GPIO[1:0]                                  | 16, 15                                                 | Input/Output, Digital        | General-purpose pins can be individually configured as either inputs or outputs; used to control and respond to various commands.          |

**DS92LX1621 Serializer PIN DESCRIPTIONS (continued)**

| Pin Name                                              | Pin No. | I/O, Type                  | Description                                                                                                                                                                                                       |
|-------------------------------------------------------|---------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>SERIAL CONTROL BUS - I<sup>2</sup>C COMPATIBLE</b> |         |                            |                                                                                                                                                                                                                   |
| SCL                                                   | 4       | Input/Output, Digital      | Clock line for the serial control bus communication<br>SCL requires an external pull-up resistor to V <sub>DDIO</sub> .                                                                                           |
| SDA                                                   | 5       | Input/Output, Open Drain   | Data line for the serial control bus communication<br>SDA requires an external pull-up resistor to V <sub>DDIO</sub> .                                                                                            |
| M/S                                                   | 8       | Input, LVCMOS w/ pull down | I <sup>2</sup> C Mode Select<br>M/S = L, Master (default); device generates and drives the SCL clock line<br>M/S = H, Slave; device accepts SCL clock input                                                       |
| CAD                                                   | 6       | Input, analog              | Continuous Address Decoder<br>Input pin to select the Slave Device Address.<br>Input is connect to external resistor divider to programmable Device ID address (See <a href="#">Figure 29</a> ).                  |
| <b>CONTROL AND CONFIGURATION</b>                      |         |                            |                                                                                                                                                                                                                   |
| PDB                                                   | 9       | Input, LVCMOS w/ pull down | Power down Mode Input Pin.<br>PDB = H, Transmitter is enabled and is ON.<br>PDB = L, Transmitter is in Sleep (Power Down). When the transmitter is in the SLEEP state, the PLL is shutdown, and IDD is minimized. |
| RES                                                   | 7       | Input, LVCMOS w/ pull down | Reserved. This pin MUST be tied LOW.                                                                                                                                                                              |
| <b>Channel Link III INTERFACE</b>                     |         |                            |                                                                                                                                                                                                                   |
| DOUT+                                                 | 13      | Input/Output, CML          | Non-inverting differential output, back-channel input.                                                                                                                                                            |
| DOUT-                                                 | 12      | Input/Output, CML          | Inverting differential output, back-channel input.                                                                                                                                                                |
| <b>Power and Ground</b>                               |         |                            |                                                                                                                                                                                                                   |
| VDDPLL                                                | 10      | Power, Analog              | PLL Power, 1.8V ±5%                                                                                                                                                                                               |
| VDDT                                                  | 11      | Power, Analog              | Tx Analog Power, 1.8V ±5%                                                                                                                                                                                         |
| VDDCML                                                | 14      | Power, Analog              | LVDS & BC Dr Power, 1.8V ±5%                                                                                                                                                                                      |
| VDDD                                                  | 28      | Power, Digital             | Digital Power, 1.8V ±5%                                                                                                                                                                                           |
| VDDIO                                                 | 25      | Power, Digital             | Power for input stage, The single-ended inputs are powered from V <sub>DDIO</sub> .                                                                                                                               |
| VSS                                                   | DAP     | Ground, DAP                | DAP must be grounded. Connect to ground plane with at least 9 vias.                                                                                                                                               |

**DS92LX1622 PIN DIAGRAM**


**Figure 5. Deserializer - DS92LX1622  
40-Pin WQFN (RTA Package)**

**DS92LX1622 Deserializer PIN DESCRIPTIONS**

| Pin Name                                              | Pin No.                                               | I/O, Type             | Description                                                                                                                                 |
|-------------------------------------------------------|-------------------------------------------------------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| <b>LVC MOS PARALLEL INTERFACE</b>                     |                                                       |                       |                                                                                                                                             |
| ROUT[13:0]                                            | 9, 10, 11, 12, 14, 15, 17, 18, 19, 20, 21, 22, 23, 24 | Outputs, LVC MOS      | Parallel data outputs.                                                                                                                      |
| HSYNC                                                 | 7                                                     | Output, LVC MOS       | Parallel data output 14, typically used as Horizontal SYNC output                                                                           |
| VSYNC                                                 | 6                                                     | Output, LVC MOS       | Parallel data output 14, typically used as Vertical SYNC output                                                                             |
| PCLK                                                  | 5                                                     | Output, LVC MOS       | Pixel Clock Output Pin.<br>Strobe edge set by RRFB control register                                                                         |
| General Purpose Input Output (GPIO)                   |                                                       |                       |                                                                                                                                             |
| ROUT[3:0] / GPIO[5:2]                                 | 21, 22, 23, 24                                        | Input/Output, Digital | ROUT[3:0] general-purpose pins can be individually configured as either inputs or outputs; used to control and respond to various commands. |
| GPIO[1:0]                                             | 26, 27                                                | Input/Output, Digital | General-purpose pins can be individually configured as either inputs or outputs; used to control and respond to various commands.           |
| <b>SERIAL CONTROL BUS - I<sup>2</sup>C COMPATIBLE</b> |                                                       |                       |                                                                                                                                             |
| SCL                                                   | 3                                                     | Input/Output, Digital | Clock line for the serial control bus communication<br>SCL requires an external pull-up resistor to V <sub>DDIO</sub> .                     |

**DS92LX1622 Deserializer PIN DESCRIPTIONS (continued)**

| Pin Name                   | Pin No.    | I/O, Type                     | Description                                                                                                                                                              |
|----------------------------|------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDA                        | 2          | Input/Output, Open Drain      | Data line for serial control bus communication<br>SDA requires an external pull-up resistor to V <sub>DDIO</sub> .                                                       |
| M/S                        | 40         | Input, LVCMOS w/<br>pull up   | I <sup>2</sup> C Mode Select                                                                                                                                             |
|                            |            |                               | M/S = L, Master; device generates and drives the SCL clock line                                                                                                          |
|                            |            |                               | M/S = H, Slave (default); device accepts SCL clock input                                                                                                                 |
| CAD                        | 1          | Input, analog                 | Continuous Address Decoder                                                                                                                                               |
|                            |            |                               | Input pin to select the Slave Device Address.                                                                                                                            |
|                            |            |                               | Input is connect to external resistor divider to programmable Device ID address<br>(See <a href="#">Figure 29</a> )                                                      |
| CONTROL AND CONFIGURATION  |            |                               |                                                                                                                                                                          |
| PDB                        | 29         | Input, LVCMOS w/<br>pull down | Power down Mode Input Pin.                                                                                                                                               |
|                            |            |                               | PDB = H, Receiver is enabled and is ON.                                                                                                                                  |
|                            |            |                               | PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVCMOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized. |
| LOCK                       | 28         | Output, LVCMOS                | LOCK Status Output Pin.                                                                                                                                                  |
|                            |            |                               | LOCK = H, PLL is Locked, outputs are active                                                                                                                              |
|                            |            |                               | LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status.                                                            |
| PASS                       | 31         | Output, LVCMOS                | When BISTEN = L; Normal operation<br>PASS is high to indicate no errors are detected. The PASS pin asserts low to indicate a CRC error was detected on the link.         |
| RES                        | 32, 33, 39 | -                             | Reserved.                                                                                                                                                                |
|                            |            |                               | Pin 39: This pin MUST be tied LOW.                                                                                                                                       |
|                            |            |                               | Pins 32, 33: Leave pin open.                                                                                                                                             |
| BIST MODE                  |            |                               |                                                                                                                                                                          |
| BISTEN                     | 37         | Input, LVCMOS w/<br>pull down | BIST Enable Pin.                                                                                                                                                         |
|                            |            |                               | BISTEN = H, BIST Mode is enabled.                                                                                                                                        |
|                            |            |                               | BISTEN = L, BIST Mode is disabled.                                                                                                                                       |
| PASS                       | 31         | Output, LVCMOS                | PASS Output Pin for BIST mode.                                                                                                                                           |
|                            |            |                               | PASS = H, ERROR FREE Transmission                                                                                                                                        |
|                            |            |                               | PASS = L, one or more errors were detected in the received payload.                                                                                                      |
|                            |            |                               | Leave Open if unused. Route to test point (pad) recommended.                                                                                                             |
| Channel Link III INTERFACE |            |                               |                                                                                                                                                                          |
| RIN+                       | 35         | Input/Output, CML             | Noninverting differential input, back channel output.                                                                                                                    |
| RIN-                       | 36         | Input/Output, CML             | Inverting differential input, back channel output.                                                                                                                       |
| POWER AND GROUND           |            |                               |                                                                                                                                                                          |
| VDDSSCG                    | 4          | Digital Power                 | SSCG Power, 1.8V ±5%<br>Power supply must be connect regardless if SSCG function is in operation                                                                         |
| VDDOR1/2/3                 | 25, 16, 8  | Digital Power                 | TTL Output Buffer Power, The single-ended outputs and control input are powered from V <sub>DDIO</sub> . V <sub>DDIO</sub> can be connected to a 1.8V ±5% or 3.3V ±10%   |
| VDDD                       | 13         | Digital Power                 | Digital Core Power, 1.8V ±5%                                                                                                                                             |
| VDDR                       | 30         | Analog Power                  | Rx Analog Power, 1.8V ±5%                                                                                                                                                |
| VDDCML                     | 34         | Analog Power                  | Bi-Directional Control Channel Driver Power, 1.8V ±5%                                                                                                                    |
| VDDPLL                     | 38         | Analog Power                  | PLL Power, 1.8V ±5%                                                                                                                                                      |
| VSS                        | DAP        | Ground                        | DAP must be grounded. Connect to the ground plane with at least 16 vias.                                                                                                 |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)(2)</sup>**

|                                                    |                                |
|----------------------------------------------------|--------------------------------|
| Supply Voltage ( $V_{DD1V8}$ )                     | –0.3V to +2.5V                 |
| Supply Voltage ( $V_{DD3V3}$ )                     | –0.3V to +4.0V                 |
| LVC MOS Input Voltage ( $V_{DD1V8}$ )              | –0.3V to $+(V_{DD1V8} + 0.3V)$ |
| LVC MOS Input Voltage ( $V_{DD3V3}$ )              | –0.3V to $+(V_{DD3V3} + 0.3V)$ |
| LVC MOS Output Voltage ( $V_{DD}$ )                | –0.3V to $+(V_{DD} + 0.3V)$    |
| CML Driver I/O Voltage ( $V_{DD1V8}$ )             | –0.3V to $(V_{DD1V8} + 0.3V)$  |
| CML Receiver I/O Voltage ( $V_{DD1V8}$ )           | –0.3V to $(V_{DD1V8} + 0.3V)$  |
| Junction Temperature                               | +150°C                         |
| Storage Temperature                                | –65°C to +150°C                |
| Maximum Package Power Dissipation Capacity         | 1/θJA °C/W above +25°          |
| Package Derating:<br>DS92LX1621 32L WQFN           |                                |
| θJA(based on 9 thermal vias)                       | 34.3 °C/W                      |
| θJC(based on 9 thermal vias)                       | 6.9 °C/W                       |
| Maximum Package Power Dissipation Capacity Package | 1/θJA °C/W above +25°          |
| Package Derating:<br>DS92LX1622 40L WQFN           |                                |
| θJA(based on 16 thermal vias)                      | 28.0 °C/W                      |
| θJC(based on 16 thermal vias)                      | 4.4 °C/W                       |
| ESD Rating (IEC 61000–4–2)                         | RD = 330Ω, CS = 150pF          |
| Air Discharge<br>(DOUT+, DOUT–, RIN+, RIN–)        | ≥±25 kV                        |
| Contact Discharge<br>(DOUT+, DOUT–, RIN+, RIN–)    | ≥±10 kV                        |
| ESD Rating (HBM)                                   | ≥±8 kV                         |

- (1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional; the device should not be operated beyond such conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

**Recommended Operating Conditions**

|                                     | Min  | Nom | Max  | Units |
|-------------------------------------|------|-----|------|-------|
| $V_{DD}$ (1.8V)                     | 1.71 | 1.8 | 1.89 | V     |
| $V_{DDIO}$ (1.8V Mode)              | 1.71 | 1.8 | 1.89 | V     |
| $V_{DDIO}$ (3.3V Mode)              | 3    | 3.3 | 3.6  | V     |
| Supply Noise                        |      |     |      |       |
| $V_{DDn}$ (1.8V)                    |      |     | 25   | mVp-p |
| $V_{DDIO}$ (1.8V)                   |      |     | 25   | mVp-p |
| $V_{DD3V3}$                         |      |     | 50   | mVp-p |
| Operating Free Air Temperature (TA) | –40  | +25 | +85  | °C    |
| Input Clock Rate                    | 10   |     | 50   | MHz   |

**Serializer Electrical Characteristics**<sup>(1)(2)(3)</sup>

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol                                                                                        | Parameter                                    | Conditions                                                        |                             | Min                                           | Typ                               | Max                                           | Unit<br>s |
|-----------------------------------------------------------------------------------------------|----------------------------------------------|-------------------------------------------------------------------|-----------------------------|-----------------------------------------------|-----------------------------------|-----------------------------------------------|-----------|
| LVCMOS DC SPECIFICATIONS 3.3V I/O (SER INPUTS, DES OUTPUTS, GPIO, CONTROL INPUTS AND OUTPUTS) |                                              |                                                                   |                             |                                               |                                   |                                               |           |
| V <sub>IH</sub>                                                                               | High Level Input Voltage                     | V <sub>IN</sub> = 3.0V to 3.6V                                    |                             | 2.0                                           |                                   | V <sub>IN</sub>                               | V         |
| V <sub>IL</sub>                                                                               | Low Level Input Voltage                      | V <sub>IN</sub> = 3.0V to 3.6V                                    |                             | GND                                           |                                   | 0.8                                           | V         |
| I <sub>IN</sub>                                                                               | Input Current                                | V <sub>IN</sub> = 0V or 3.6V<br>V <sub>IN</sub> = 3.0V to 3.6V    |                             | -20                                           | ±1                                | +20                                           | µA        |
| V <sub>OH</sub>                                                                               | High Level Output Voltage                    | V <sub>DDIO</sub> = 3.0V to 3.6V                                  |                             | 2.4                                           |                                   | V <sub>DDIO</sub>                             | V         |
| V <sub>OL</sub>                                                                               | Low Level Output Voltage                     | V <sub>DDIO</sub> = 3.0V to 3.6V<br>I <sub>OH</sub> = +4mA        |                             | GND                                           |                                   | 0.4                                           | V         |
| I <sub>OS</sub>                                                                               | Output Short Circuit Current                 | V <sub>OUT</sub> = 0V                                             | Serializer GPIO Outputs     |                                               | -24                               |                                               | mA        |
|                                                                                               |                                              |                                                                   | Deserializer LVCMOS Outputs |                                               | -39                               |                                               |           |
| I <sub>OZ</sub>                                                                               | TRI-STATE Output Current                     | PDB = 0V,<br>V <sub>OUT</sub> = 0V or V <sub>DD</sub>             | LVCMOS Outputs              | -20                                           | ±1                                | +20                                           | µA        |
| LVCMOS DC SPECIFICATIONS 1.8V I/O (TX INPUTS, RX OUTPUTS, GPIO, CONTROL INPUTS AND OUTPUTS)   |                                              |                                                                   |                             |                                               |                                   |                                               |           |
| V <sub>IH</sub>                                                                               | High Level Input Voltage                     | V <sub>IN</sub> = 1.71V to 1.89V                                  |                             | 0.65 V <sub>IN</sub>                          |                                   | V <sub>IN</sub> +0.3                          | V         |
| V <sub>IL</sub>                                                                               | Low Level Input Voltage                      | V <sub>IN</sub> = 1.71V to 1.89V                                  |                             | GND                                           |                                   | 0.35 V <sub>IN</sub>                          |           |
| I <sub>IN</sub>                                                                               | Input Current                                | V <sub>IN</sub> = 0V or 1.89V<br>V <sub>IN</sub> = 1.71V to 1.89V |                             | -20                                           | ±1                                | +20                                           | µA        |
| V <sub>OH</sub>                                                                               | High Level Output Voltage                    | V <sub>DDIO</sub> = 1.71V to 1.89V<br>I <sub>OH</sub> = -4mA      |                             | V <sub>DDIO</sub> - 0.45                      |                                   | V <sub>DDIO</sub>                             | V         |
| V <sub>OL</sub>                                                                               | Low Level Output Voltage                     | V <sub>DDIO</sub> = 1.71V to 1.89V<br>I <sub>OL</sub> = +4 mA     |                             | GND                                           |                                   | 0.45                                          | V         |
| I <sub>OS</sub>                                                                               | Output Short Circuit Current                 | V <sub>OUT</sub> = 0V <sup>(4)</sup>                              | Serializer GPIO Outputs     |                                               | -11                               |                                               | mA        |
|                                                                                               |                                              |                                                                   | Deserializer LVCMOS Outputs |                                               | -20                               |                                               |           |
| I <sub>OZ</sub>                                                                               | TRI-STATE Output Current                     | PDB = 0V,<br>V <sub>OUT</sub> = 0V or V <sub>DD</sub>             | LVCMOS Outputs              | -20                                           | ±1                                | +20                                           | µA        |
| CML DRIVER DC SPECIFICATIONS (DOUT+, DOUT-)                                                   |                                              |                                                                   |                             |                                               |                                   |                                               |           |
| V <sub>OD</sub>                                                                               | Output Differential Voltage                  | R <sub>T</sub> = 100Ω                                             |                             | 268                                           | 340                               | 412                                           | mV        |
| ΔV <sub>OD</sub>                                                                              | Output Differential Voltage Unbalance        | R <sub>L</sub> = 100Ω                                             |                             |                                               | 1                                 | 50                                            | mV        |
| V <sub>OS</sub>                                                                               | Output Differential Offset Voltage           | R <sub>L</sub> = 100Ω (See <a href="#">Figure 10</a> )            |                             | V <sub>DD</sub> (MIN) - V <sub>OD</sub> (MAX) | V <sub>DD</sub> - V <sub>OD</sub> | V <sub>DD</sub> (MAX) - V <sub>OD</sub> (MIN) | V         |
| ΔV <sub>OS</sub>                                                                              | Offset Voltage Unbalance                     | R <sub>L</sub> = 100Ω                                             |                             |                                               | 1                                 | 50                                            | mV        |
| I <sub>OS</sub>                                                                               | Output Short Circuit Current                 | DOUT+/- = 0V,<br>PDB = L or H <sup>(4)</sup>                      |                             |                                               | -27                               |                                               | mA        |
| R <sub>T</sub>                                                                                | Differential Internal Termination Resistance | Differential across DOUT+ and DOUT-                               |                             | 80                                            | 100                               | 120                                           | Ω         |
| CML RECEIVER DC SPECIFICATIONS (RIN+, RIN-)                                                   |                                              |                                                                   |                             |                                               |                                   |                                               |           |
| V <sub>TH</sub>                                                                               | Differential Threshold High Voltage          | See <a href="#">Figure 12</a>                                     |                             |                                               |                                   | +90                                           | mV        |
| V <sub>TL</sub>                                                                               | Differential Threshold Low Voltage           |                                                                   |                             | -90                                           |                                   |                                               |           |

- (1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
- (2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except  $V_{OD}$ ,  $\Delta V_{OD}$ ,  $V_{TH}$  and  $V_{TL}$  which are differential voltages.
- (3) Typical values represent most likely parametric norms at 1.8V or 3.3V,  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
- (4) Specification is guaranteed by characterization and is not tested in production.

**Serializer Electrical Characteristics<sup>(1)(2)(3)</sup> (continued)**

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol                                                       | Parameter                                                         | Conditions                                                               | Min                                                     | Typ     | Max | Units    |
|--------------------------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------------|---------------------------------------------------------|---------|-----|----------|
| $V_{IN}$                                                     | Differential Input Voltage Range                                  | $R_{IN+} - R_{IN-}$                                                      | 180                                                     |         |     | mV       |
| $I_{IN}$                                                     | Input Current                                                     | $V_{IN} = V_{DD}$ or 0V,<br>$V_{DD} = 1.89V$                             | -20                                                     | $\pm 1$ | +20 | $\mu A$  |
| $R_T$                                                        | Differential Internal Termination Resistance                      | Differential across $R_{IN+}$ and $R_{IN-}$                              | 80                                                      | 100     | 120 | $\Omega$ |
| <b>SER/DES SUPPLY CURRENT *DIGITAL, PLL, AND ANALOG VDDS</b> |                                                                   |                                                                          |                                                         |         |     |          |
| $I_{DDT}$                                                    | Serializer (Tx) Total Supply Current Mode (includes load current) | $R_T = 100\Omega$<br>WORST CASE pattern<br>(See Figure 7)                | $V_{DDn} = 1.89V$ ,<br>$f = 50MHz$<br>Default Registers | 62      | 90  | mA       |
|                                                              |                                                                   | $R_T = 100\Omega$<br>RANDOM PRBS-7 pattern                               |                                                         | 55      |     |          |
| $I_{DDIOT}$                                                  | Serializer (Tx) VDDIO Supply Current (includes load current)      | $R_T = 100\Omega$<br>WORST CASE pattern<br>(See Figure 7)                | $V_{DDn} = 1.89V$ ,<br>$f = 50MHz$<br>Default Registers | 2       | 5   | mA       |
|                                                              |                                                                   |                                                                          | $V_{DDn} = 3.6V$ ,<br>$f = 50MHz$<br>Default Registers  | 7       | 15  |          |
| $I_{DDTZ}$                                                   | Serializer (Tx) Supply Current Power-down                         | $PDB = 0V$ ; All other<br>LVCMOS Inputs = 0V                             | $V_{DD} = 1.89V$                                        | 370     | 775 | $\mu A$  |
|                                                              |                                                                   |                                                                          | $V_{DDIO} = 1.89V$                                      | 55      | 125 |          |
| $I_{DDIOTZ}$                                                 |                                                                   |                                                                          | $V_{DDIO} = 3.6V$                                       | 65      | 135 |          |
| $I_{DDR}$                                                    | Deserializer (Rx) Supply Current (includes load current)          | $V_{DDn} = 1.89V$<br>$CL = 8pF$<br>WORST CASE Pattern<br>(See Figure 7)  | $f = 50 MHz$<br>SSCG[3:0] = ON<br>Default Registers     | 60      | 96  | mA       |
|                                                              |                                                                   | $V_{DDn} = 3.6V$<br>$CL = 8pF$<br>WORST CASE Pattern                     | $f = 50 MHz$<br>Default Registers                       | 53      |     |          |
| $I_{DDIOR}$                                                  | Deserializer (Rx) VDDIO Supply Current (includes load current)    | $V_{DDIO} = 1.89V$<br>$CL = 8pF$<br>WORST CASE Pattern<br>(See Figure 7) | $f = 50 MHz$<br>Default Registers                       | 16      | 25  |          |
|                                                              |                                                                   | $V_{DDIO} = 3.6V$<br>$CL = 8pF$<br>Worst Case Pattern                    | $f = 50 MHz$<br>Default Registers                       | 38      | 64  |          |
| $I_{DDRZ}$                                                   | Deserializer (Rx) Supply Current Power-down                       | $PDB = 0V$ ; All other<br>LVCMOS Inputs = 0V                             | $V_{DDn} = 1.89V$                                       | 42      | 400 | $\mu A$  |
|                                                              |                                                                   |                                                                          | $V_{DDIO} = 1.89V$                                      | 8       | 40  |          |
| $I_{DDIORZ}$                                                 |                                                                   |                                                                          | $V_{DDIO} = 3.6V$                                       | 350     | 800 |          |

## Recommended Serializer Timing for PCLK<sup>(1)(2)</sup>

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol            | Parameter                        | Conditions      | Min  | Typ  | Max  | Units |
|-------------------|----------------------------------|-----------------|------|------|------|-------|
| t <sub>TCP</sub>  | Transmit Clock Period            | 10 MHz — 50 MHz | 20   | T    | 100  | ns    |
| t <sub>TCIH</sub> | Transmit Clock Input High Time   |                 | 0.4T | 0.5T | 0.6T | ns    |
| t <sub>TCIL</sub> | Transmit Clock Input Low Time    |                 | 0.4T | 0.5T | 0.6T | ns    |
| t <sub>CLKT</sub> | PCLK Input Transition Time       |                 | 0.5  |      | 3    | ns    |
| f <sub>osc</sub>  | Internal oscillator clock source |                 |      | 25   |      | MHz   |

- (1) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
- (2) Typical values represent most likely parametric norms at 1.8V or 3.3V, T<sub>A</sub> = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

## Serializer Switching Characteristics<sup>(1)(2)(3)</sup>

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol             | Parameter                                             | Conditions                                                                                                                                                       | Min        | Typ         | Max           | Units             |
|--------------------|-------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-------------|---------------|-------------------|
| t <sub>LHT</sub>   | CML Low-to-High Transition Time                       | RL = 100Ω (See <a href="#">Figure 8</a> )                                                                                                                        |            | 150         | 330           | ps                |
| t <sub>HLT</sub>   | CML High-to-Low Transition Time                       | RL = 100Ω (See <a href="#">Figure 8</a> )                                                                                                                        |            | 150         | 330           | ps                |
| t <sub>DIS</sub>   | Data Input Setup to PCLK                              | Serializer Data Inputs (See <a href="#">Figure 14</a> )                                                                                                          | 2.0        |             |               | ns                |
| t <sub>DIH</sub>   | Data Input Hold from PCLK                             |                                                                                                                                                                  | 2.0        |             |               | ns                |
| t <sub>PLD</sub>   | Serializer PLL Lock Time <sup>(4)(5)</sup>            | RL = 100Ω                                                                                                                                                        |            | 1           | 2             | ms                |
| t <sub>SD</sub>    | Serializer Delay                                      | R <sub>T</sub> = 100Ω<br>f = 10-50 MHz<br>Reg Address 0x03h b[0] (TRFB = 1) (See <a href="#">Figure 16</a> )                                                     | 6.386T + 5 | 6.386T + 12 | 6.386T + 19.7 | ns                |
| t <sub>JIND</sub>  | Serializer Output Deterministic Jitter                | Serializer output intrinsic deterministic jitter. Measure with PRBS-7 test pattern. PCLK = 50 MHz                                                                |            | 0.13        |               | UI <sup>(6)</sup> |
| t <sub>JINR</sub>  | Serializer Output Random Jitter                       | Serializer output intrinsic random jitter (cycle-cycle). Alternating – 1,0 pattern.                                                                              |            | 0.04        |               | UI <sup>(6)</sup> |
| t <sub>JINT</sub>  | Peak-to-peak Serializer Output Jitter                 | Serializer output peak-to-peak jitter includes deterministic jitter, random jitter, and jitter transfer from serializer input. Measure with PRBS-7 test pattern. |            | 0.396       |               | UI <sup>(6)</sup> |
| λ <sub>STXBW</sub> | Serializer Jitter Transfer Function -3 dB Bandwidth   | PCLK = 50 MHz<br>Default Registers                                                                                                                               |            | 1.9         |               | MHz               |
| δ <sub>STX</sub>   | Serializer Jitter Transfer Function                   | PCLK = 50 MHz<br>Default Registers                                                                                                                               |            | 0.944       |               | dB                |
| δ <sub>STXf</sub>  | Serializer Jitter Transfer Function Peaking Frequency | PCLK = 50 MHz<br>Default Registers                                                                                                                               |            | 500         |               | kHz               |

- (1) Typical values represent most likely parametric norms at 1.8V or 3.3V, T<sub>A</sub> = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
- (2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD, ΔVOD, VTH and VTL which are differential voltages.
- (3) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
- (4) t<sub>PLD</sub> and t<sub>DDL</sub> is the time required by the serializer and deserializer to obtain data lock when exiting power-down state with an active PCLK.
- (5) Specification is guaranteed by design and is not tested in production.
- (6) UI – Unit Interval is equivalent to one ideal serialized data bit width. The UI scales with PCLK frequency.

## Deserializer Switching Characteristics<sup>(1)(2)(3)(4)</sup>

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol      | Parameter                                               | Conditions                                                                                                                | Pin/Freq.                 | Min          | Typ                         | Max           | Units |
|-------------|---------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|---------------------------|--------------|-----------------------------|---------------|-------|
| $t_{RCP}$   | Receiver Output Clock Period                            | $t_{RCP} = t_{TCP}$                                                                                                       | PCLK                      | 20           | T                           | 100           | ns    |
| $t_{PDC}$   | PCLK Duty Cycle                                         | Default Registers<br>SSCG[3:0] = OFF                                                                                      | PCLK                      | 45           | 50                          | 55            | %     |
| $t_{CLH}$   | LVC MOS Low-to-High Transition Time                     | $V_{DDIO}$ : 1.71V to 1.89V or 3.0V to 3.6V, $C_L = 8$ pF (lumped load)<br>Default Registers (See Table 1) <sup>(5)</sup> | PCLK                      | 1.3          | 2.0                         | 2.8           | ns    |
| $t_{CHL}$   | LVC MOS High-to-Low Transition Time                     |                                                                                                                           |                           | 1.3          | 2.0                         | 2.8           |       |
| $t_{CLH}$   | LVC MOS Low-to-High Transition Time                     | $V_{DDIO}$ : 1.71V to 1.89V or 3.0V to 3.6V, $C_L = 8$ pF (lumped load)<br>Default Registers (See Table 1) <sup>(6)</sup> | Deserializer Data Outputs | 1.6          | 2.4                         | 3.3           | ns    |
| $t_{CHL}$   | LVC MOS High-to-Low Transition Time                     |                                                                                                                           |                           | 1.6          | 2.4                         | 3.3           |       |
| $t_{ROS}$   | ROUT Setup Data to PCLK                                 | $V_{DDIO}$ : 1.71V to 1.89V or 3.0V to 3.6V, $C_L = 8$ pF (lumped load)<br>Default Registers ( See Table 1)               | Deserializer Data Outputs | 0.38T        | 0.5T                        |               | ns    |
| $t_{ROH}$   | ROUT Hold Data to PCLK                                  |                                                                                                                           |                           | 0.38T        | 0.5T                        |               |       |
| $t_{DD}$    | Deserializer Delay                                      | Default Registers<br>Register 0x03h b[0] (RRFB = 1)                                                                       | 10 MHz-50 MHz             | $4.571T + 8$ | $4.571T + 12$               | $4.571T + 16$ | ns    |
| $t_{DDL T}$ | Deserializer Data Lock Time                             |                                                                                                                           | 10 MHz-50 MHz             |              |                             | 10            | ms    |
| $t_{RJIT}$  | Receiver Input Jitter Tolerance <sup>(7)</sup>          |                                                                                                                           | 50 MHz                    |              | 0.53                        |               | UI    |
| $t_{RDJ}$   | Receiver Clock Jitter                                   | PCLK<br>SSCG[3:0] = OFF                                                                                                   | 10 MHz                    |              | 300                         | 550           | ps    |
|             |                                                         |                                                                                                                           | 50 MHz                    |              | 120                         | 250           |       |
| $t_{DPJ}$   | Deserializer Period Jitter <sup>(8)</sup>               | PCLK<br>SSCG[3:0] = OFF                                                                                                   | 10 MHz                    |              | 425                         | 600           | ps    |
|             |                                                         |                                                                                                                           | 50 MHz                    |              | 320                         | 480           |       |
| $t_{DCCJ}$  | Deserializer Cycle-to-Cycle Clock Jitter <sup>(9)</sup> | PCLK<br>SSCG[3:0] = OFF                                                                                                   | 10 MHz                    |              | 320                         | 500           | ps    |
|             |                                                         |                                                                                                                           | 50 MHz                    |              | 300                         | 500           |       |
| $f_{dev}$   | Spread Spectrum Clocking Deviation Frequency            | LVC MOS Output Bus<br>(See Figure 21)                                                                                     | 20 MHz-50 MHz             |              | $\pm 0.5\%$ to $\pm 2.0\%$  |               | %     |
| $f_{mod}$   | Spread Spectrum Clocking Modulation Frequency           |                                                                                                                           | 20 MHz-50 MHz             |              | $\pm 9$ kHz to $\pm 66$ kHz |               | kHz   |

- (1) The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.
- (2) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except VOD,  $\Delta VOD$ , VTH and VTL which are differential voltages.
- (3) Typical values represent most likely parametric norms at 1.8V or 3.3V,  $T_A = +25^\circ\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.
- (4)  $t_{DCJ}$  is the maximum amount of jitter measured over 30,000 samples based on Time Interval Error (TIE).
- (5) Specification is guaranteed by characterization and is not tested in production.
- (6) Specification is guaranteed by design and is not tested in production.
- (7)  $t_{RJIT}$  max (0.61 UI) is limited by instrumentation and actual  $t_{RJIT}$  of in-band jitter at low frequency (<2MHz) is greater than 1 UI.
- (8)  $t_{DPJ}$  is the maximum amount the period is allowed to deviate measured over 30,000 samples.
- (9)  $t_{DCCJ}$  is the maximum amount of jitter between adjacent clock cycles measured over 30,000 samples.

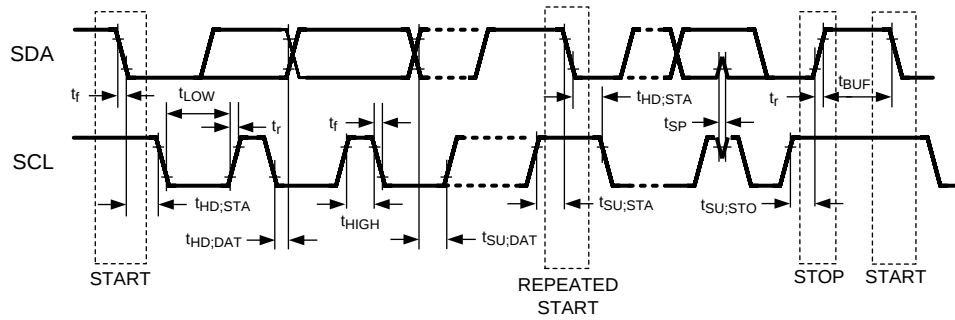
## Bi-Directional Control Bus Timing Specifications (SCL, SDA) - (See Figure 6)

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol                                               | Parameter                                             | Conditions                                                | Min | Typ | Max  | Units |
|------------------------------------------------------|-------------------------------------------------------|-----------------------------------------------------------|-----|-----|------|-------|
| RECOMMENDED INPUT TIMING REQUIREMENTS <sup>(1)</sup> |                                                       |                                                           |     |     |      |       |
| f <sub>SCL</sub>                                     | SCL Clock Frequency                                   | f <sub>SCL</sub> = 100 kHz                                | >0  |     | 100  | kHz   |
| f <sub>LOW</sub>                                     | SCL Low Period                                        |                                                           | 4.7 |     |      | μs    |
| f <sub>HIGH</sub>                                    | SCL High Period                                       |                                                           | 4.0 |     |      | μs    |
| t <sub>HD:STA</sub>                                  | Hold time for a start or a repeated start condition   |                                                           | 4.0 |     |      | μs    |
| t <sub>SU:STA</sub>                                  | Set Up time for a start or a repeated start condition |                                                           | 4.7 |     |      | μs    |
| t <sub>HD:DAT</sub>                                  | Data Hold Time                                        |                                                           | 0   |     | 3.45 | μs    |
| t <sub>SU:DAT</sub>                                  | Data Set Up Time                                      |                                                           | 250 |     |      | ns    |
| t <sub>SU:STO</sub>                                  | Set Up Time for STOP Condition,                       |                                                           | 4.0 |     |      | μs    |
| t <sub>r</sub>                                       | SCL & SDA Rise Time                                   |                                                           |     |     | 1000 | ns    |
| t <sub>f</sub>                                       | SCL & SDA Fall Time                                   |                                                           |     |     | 300  | ns    |
| C <sub>b</sub>                                       | Capacitive load for bus                               |                                                           |     | 400 | pF   |       |
| SWITCHING CHARACTERISTICS <sup>(2)</sup>             |                                                       |                                                           |     |     |      |       |
| f <sub>SCL</sub>                                     | SCL Clock Frequency                                   | Serializer M/S = 0 – R/W Register 0x05 = 0x40'h           |     | 100 |      | kHz   |
|                                                      |                                                       | Deserializer M/S = 0 – READ Register 0x06 b[6:4] = 0x00'h |     | 100 |      |       |
| f <sub>LOW</sub>                                     | SCL Low Period                                        | Serializer M/S = 0 – R/W Register 0x05 = 0x40'h           | 4.7 |     |      | μs    |
|                                                      |                                                       | Deserializer M/S = 0 – READ Register 0x06 b[6:4] = 0x00'h |     |     |      |       |
| f <sub>HIGH</sub>                                    | SCL High Period                                       | Serializer M/S = 0 – R/W Register 0x05 = 0x40'h           | 4.0 |     |      | μs    |
|                                                      |                                                       | Deserializer M/S = 0 – READ Register 0x06 b[6:4] = 0x00'h |     |     |      |       |
| t <sub>HD:STA</sub>                                  | Hold time for a start or a repeated start condition   | Serializer M/S = 0 Register 0x05 = 0x40'h                 | 4.0 |     |      | μs    |
| t <sub>SU:STA</sub>                                  | Set Up time for a start or a repeated start condition | Serializer M/S = 0 Register 0x05 = 0x40'h                 | 4.7 |     |      | μs    |
| t <sub>HD:DAT</sub>                                  | Data Hold Time                                        |                                                           | 0   |     | 3.45 | μs    |
| t <sub>SU:DAT</sub>                                  | Data Set Up Time                                      |                                                           | 250 |     |      | ns    |
| t <sub>SU:STO</sub>                                  | Set Up Time for STOP Condition                        | Serializer M/S = 0                                        | 4.0 |     |      | μs    |
| t <sub>f</sub>                                       | SCL & SDA Fall Time                                   |                                                           |     |     | 300  | ns    |
| t <sub>BUF</sub>                                     | Bus free time between a stop and start condition      | Serializer M/S = 0                                        | 4.7 |     |      | μs    |
| t <sub>TIMEOUT</sub>                                 | NACK Time out                                         | Serializer M/S = 1                                        |     | 1   |      | ms    |
|                                                      |                                                       | Deserializer MODE = 1 Register 0x06 b[2:0]=111'b          |     | 25  |      |       |

(1) Recommended Input Timing Requirements are input specifications and not tested in production.

(2) Specification is guaranteed by design and is not tested in production.

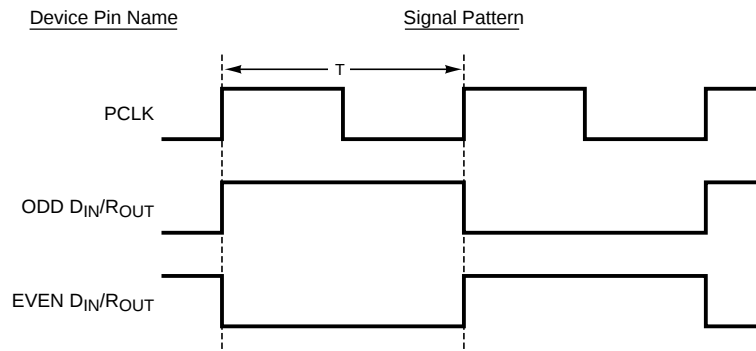


**Figure 6. Bi-Directional Control Bus Timing**

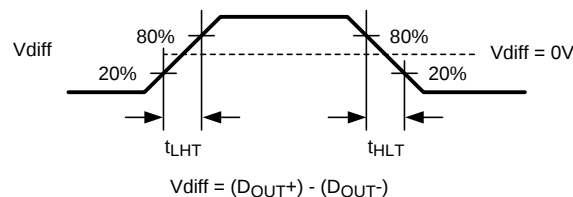
### Bi-Directional Control Bus DC Characteristics (SCL, SDA) - I<sup>2</sup>C Compliant

| Symbol          | Parameter                | Conditions                                                    | Min                     | Typ | Max                     | Units |
|-----------------|--------------------------|---------------------------------------------------------------|-------------------------|-----|-------------------------|-------|
| V <sub>IH</sub> | Input High Level         | SDA and SCL                                                   | 0.7 x V <sub>DDIO</sub> |     | V <sub>DDIO</sub>       | V     |
| V <sub>IL</sub> | Input Low Level Voltage  | SDA and SCL                                                   | GND                     |     | 0.3 x V <sub>DDIO</sub> | V     |
| V <sub>HY</sub> | Input Hysteresis         |                                                               |                         | >50 |                         | mV    |
| I <sub>OZ</sub> | TRI-STATE Output Current | PDB = 0V V <sub>OUT</sub> = 0V or V <sub>DD</sub>             | -20                     | ±1  | +20                     | μA    |
| I <sub>IN</sub> | Input Current            | SDA or SCL, V <sub>in</sub> = V <sub>DDIO</sub> or GND        | -20                     | ±1  | +20                     | μA    |
| C <sub>IN</sub> | Input Pin Capacitance    |                                                               |                         | <5  |                         | pF    |
| V <sub>OL</sub> | Low Level Output Voltage | SCL and SDA V <sub>DDIO</sub> = 3.0V I <sub>OL</sub> = 1.5 mA |                         |     | 0.36                    | V     |
|                 |                          | SCL and SDA V <sub>DDIO</sub> = 1.71V I <sub>OL</sub> = 1 mA  |                         |     | 0.36                    |       |

### AC Timing Diagrams and Test Circuits



**Figure 7. "Worst Case" Test Pattern**



**Figure 8. Serializer CML Output Load and Transition Times**

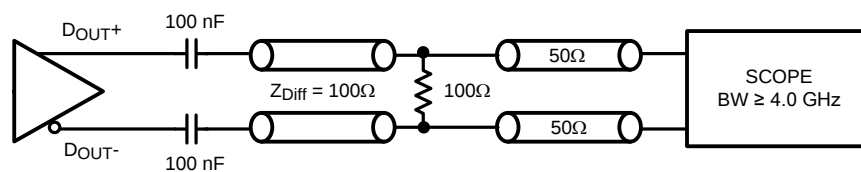


Figure 9. Serializer CML Output Load and Transition Times

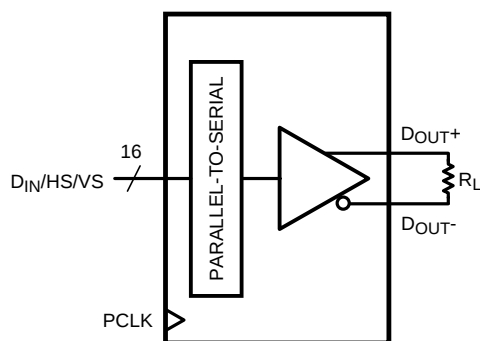


Figure 10. Serializer VOD DC Diagram

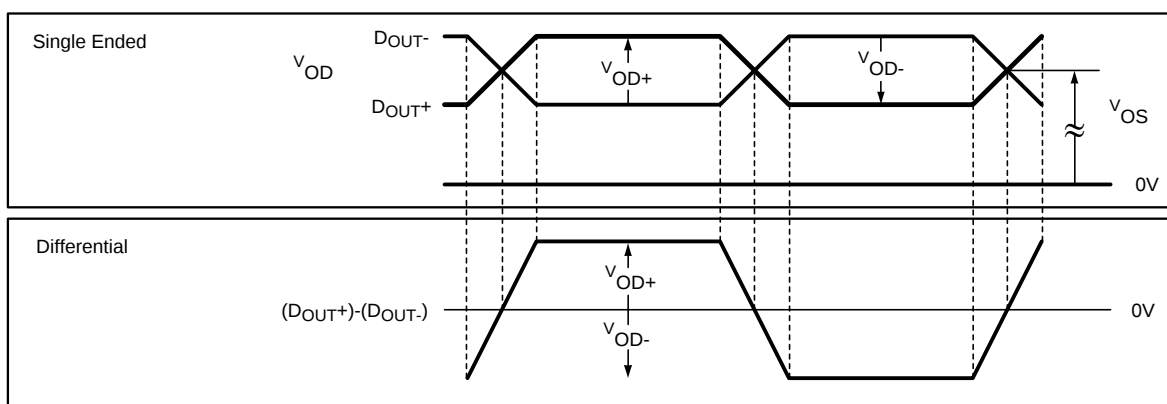


Figure 11. Serializer VOD DC Diagram

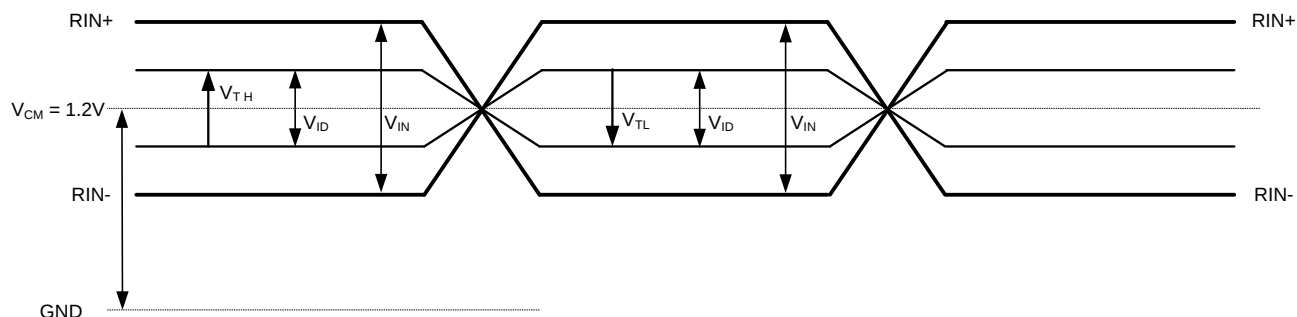
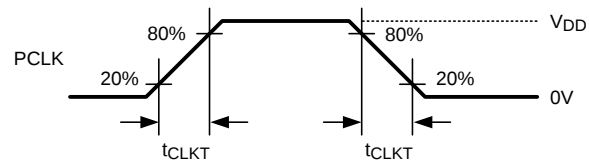
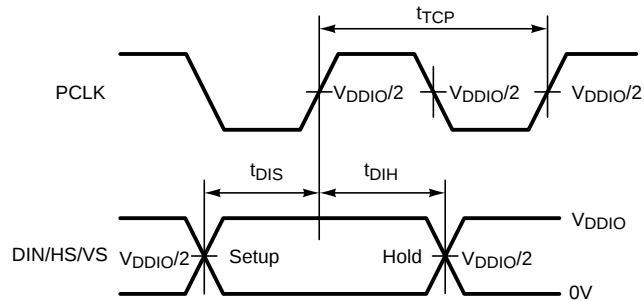


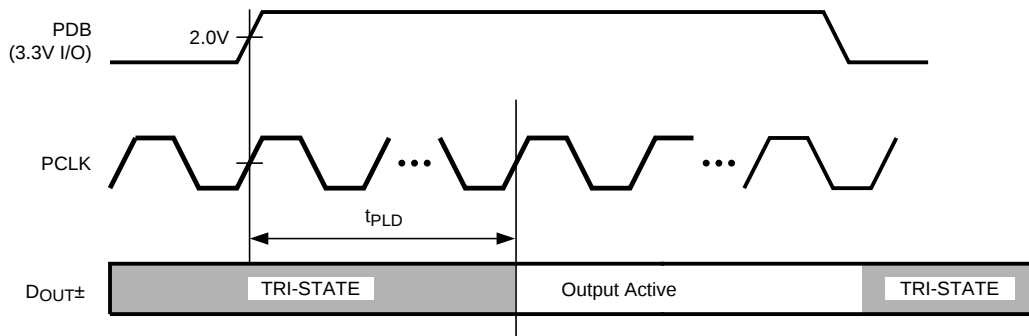
Figure 12. Differential VTH/VTL Definition Diagram



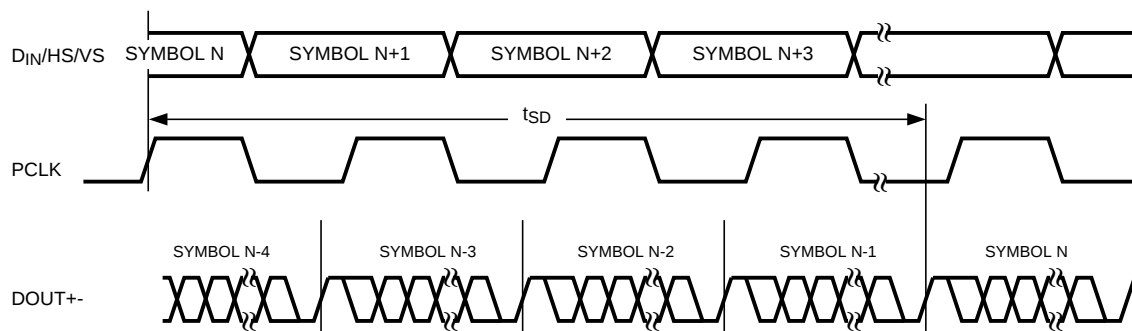
**Figure 13. Serializer Input Clock Transition Times**



**Figure 14. Serializer Setup/Hold Times**



**Figure 15. Serializer Data Lock Time**



**Figure 16. Serializer Delay**

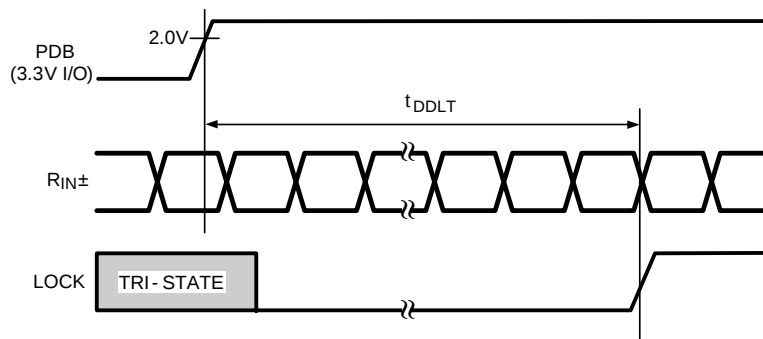


Figure 17. Deserializer Data Lock Time

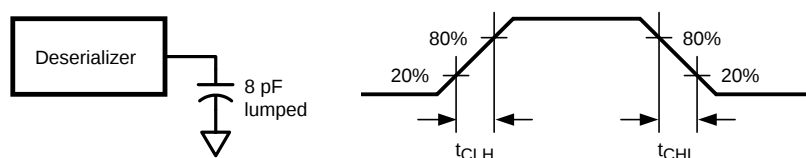


Figure 18. Deserializer LVCMOS Output Load and Transition Times

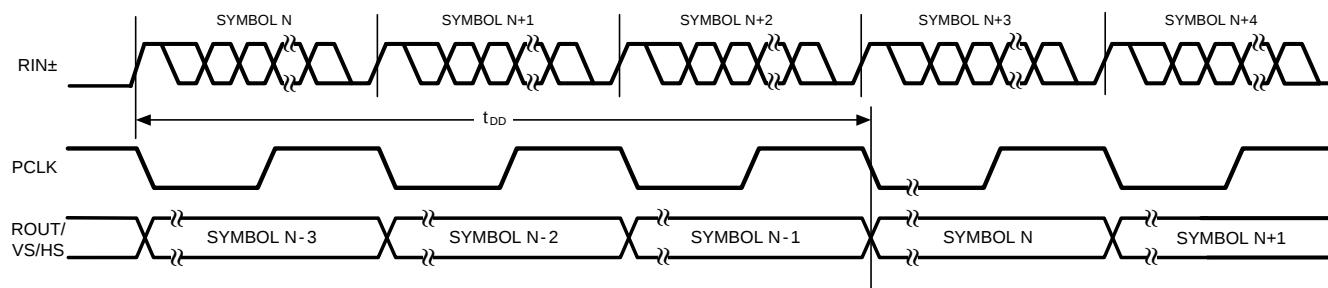


Figure 19. Deserializer Delay

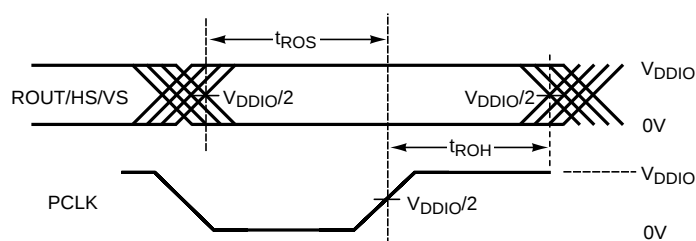
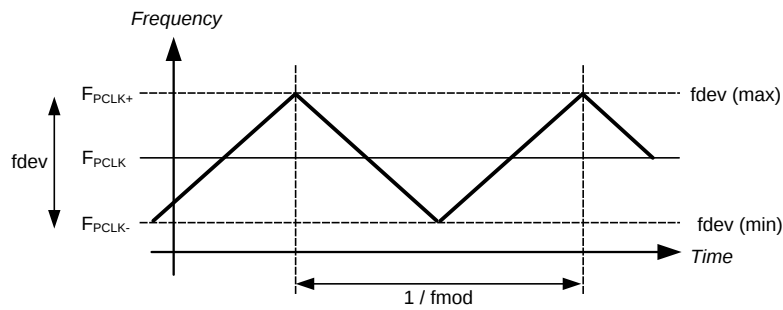
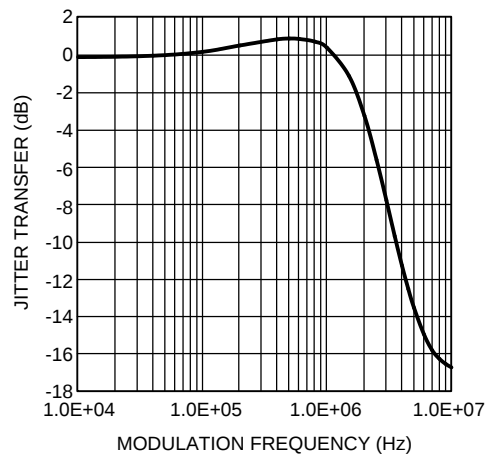


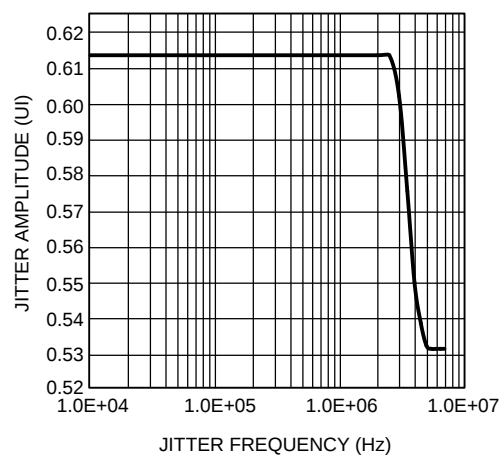
Figure 20. Deserializer Output Setup/Hold Times



**Figure 21. Spread Spectrum Clock Output Profile**



**Figure 22. Typical Serializer Jitter Transfer Function at 43 MHz**



**Figure 23. Typical Deserializer Input Jitter Tolerance Curve at 43 MHz**

**Table 1. DS92LX1621 Control Registers**

| Addr (Hex) | Name                            | Bits | Field                         | R/W | Default      | Description                                                                                                                                                                                                                       |
|------------|---------------------------------|------|-------------------------------|-----|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0          | I <sup>2</sup> C Device ID      | 7:1  | DEVICE ID                     | RW  | 0x58         | 7-bit address of Serializer; 0x58h (1011_000X) default                                                                                                                                                                            |
|            |                                 | 0    | SER ID                        | RW  | 0            | 0: Device ID is from CAD<br>1: Register I <sup>2</sup> C Device ID overrides CAD                                                                                                                                                  |
| 1          | Reset                           | 7:3  | RESERVED                      |     | 0            | Reserved                                                                                                                                                                                                                          |
|            |                                 | 2    | STANDBY                       | RW  | 0            | Standby mode control. Retains control register data. Supported only when M/S = 0<br>0: Enabled. Low-current Standby mode with wake-up capability. Suspends all clocks and functions.<br>1: Disabled. Standby and wake-up disabled |
|            |                                 | 1    | DIGITAL RESET0                | RW  | 0 self clear | 1: Resets the device to default register values. Does not affect device I <sup>2</sup> C Bus or Device ID                                                                                                                         |
|            |                                 | 0    | DIGITAL RESET1                | RW  | 0 self clear | 1: Digital Reset, retains all register values                                                                                                                                                                                     |
| 2          | Reserved                        | 7:0  | RESERVED                      |     | 0x20'h       | Reserved                                                                                                                                                                                                                          |
| 3          | CRC Fault Tolerant Transmission | 7    | RX CRC CHECKER ENABLE         | RW  | 1            | Back Channel CRC Enable<br>0: Disable<br>1: Enable<br>For proper CRC operation, control register 0x03h b[6] of the Deserializer must be enabled.                                                                                  |
|            | CRC Fault Tolerant Transmission | 6    | TX CRC GEN ENABLE             | RW  | 1            | Forward Channel CRC Enable<br>0: Disable<br>1: Enable<br>For proper CRC operation, control register 0x03h b[7] of the Deserializer must be enabled.                                                                               |
|            | VDDIO Control                   | 5    | VDDIO CONTROL                 | RW  | 1            | Auto V <sub>DDIO</sub> detect<br>0: Disable<br>1: Enable (auto detect mode)                                                                                                                                                       |
|            | VDDIO Mode                      | 4    | VDDIO MODE                    | RW  | 1            | VDDIO voltage set<br>Only used when VDDIOCONTROL = 0<br>0: 1.8V<br>1: 3.3V                                                                                                                                                        |
|            | I <sup>2</sup> C Pass-Through   | 3    | I <sup>2</sup> C PASS-THROUGH | RW  | 1            | I <sup>2</sup> C Pass-Through Mode<br>0: Disabled<br>1: Enabled                                                                                                                                                                   |
|            | Reserved                        | 2    | RESERVED                      |     | 0            | Reserved                                                                                                                                                                                                                          |
|            | PCLK_AUTO                       | 1    | PCLK_AUTO                     | RW  | 1            | Switch over to internal 25 MHz oscillator clock in the absence of PCLK<br>0: Disable<br>1: Enable                                                                                                                                 |
|            | TRFB                            | 0    | TRFB                          | RW  | 1            | Pixel Clock Edge Select:<br>0: Parallel Interface Data is strobed on the Falling Clock Edge.<br>1: Parallel Interface Data is strobed on the Rising Clock Edge.                                                                   |
| 4          | CRC Transmission                | 7:6  | RESERVED                      |     | 01'b         | Reserved                                                                                                                                                                                                                          |
|            |                                 | 5    | CRC RESET                     | RW  | 0            | 1: CRC Reset.<br>Clears CRC Error counter.                                                                                                                                                                                        |
|            |                                 | 4:0  | RESERVED                      |     | 0            | Reserved                                                                                                                                                                                                                          |

**Table 1. DS92LX1621 Control Registers (continued)**

| Addr (Hex) | Name                      | Bits | Field                     | R/W | Default | Description                                                                                                                                                                                                        |
|------------|---------------------------|------|---------------------------|-----|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5          | I <sup>2</sup> C Bus Rate | 7:0  | I <sup>2</sup> C BUS RATE | RW  | 0x40    | I <sup>2</sup> C ratio is determined by the following:<br>$f_{SCL} = 6.25 \text{ MHz} / \text{register value (in decimal)}$<br>0x40'h = ~100 kHz SCL (default)<br>Note: Register values <0x32'h are NOT supported. |
| 6          | DES ID                    | 7:1  | DES DEV ID                | RW  | 0x60    | Deserializer Device ID = 0x60 (1100_000X) default                                                                                                                                                                  |
|            |                           | 0    | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
| 7          | Slave ID                  | 7:1  | SLAVE DEV ID              | RW  | 0       | Slave Device ID. Must be programmed to communicate with remote slave device                                                                                                                                        |
|            |                           | 0    | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
| 8          | Reserved                  | 7:0  | RESERVED                  | RW  | 0       | Reserved                                                                                                                                                                                                           |
| 9          | Reserved                  | 7:0  | RESERVED                  | RW  | 1       | Reserved                                                                                                                                                                                                           |
| A          | CRC Errors                | 7:0  | CRC ERROR B0              | R   | 0       | Number of CRC errors - 8 LSBs                                                                                                                                                                                      |
| B          | CRC Errors                | 7:0  | CRC ERROR B1              | R   | 0       | Number of CRC errors - 8 MSBs                                                                                                                                                                                      |
| C          | Reserved                  | 7:3  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            | PCLK Detect               | 2    | PCLK DETECT               | R   | 0       | 1: Valid PCLK detected<br>0: Valid PCLK not detected                                                                                                                                                               |
|            | CRC Check                 | 1    | DES ERROR                 | R   | 0       | 1: CRC error during communication with Deserializer                                                                                                                                                                |
|            | Cable Link Detect Status  | 0    | LINK DETECT               | R   | 0       | 1: Cable link detected<br>0: Cable link not detected                                                                                                                                                               |
| D          | GPIO[0] Config            | 7:4  | RESERVED                  |     | 1       | Reserved                                                                                                                                                                                                           |
|            |                           | 3:2  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 1    | GPIO0 DIR                 | RW  | 0       | 0: Output<br>1: Input                                                                                                                                                                                              |
|            |                           | 0    | GPIO0 EN                  | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                                                                                                                                                         |
| E          | GPIO[1] Config            | 7:4  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 3:2  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 1    | GPIO1 DIR                 | RW  | 0       | 0: Output<br>1: Input                                                                                                                                                                                              |
|            |                           | 0    | GPIO1 EN                  | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                                                                                                                                                         |
| F          | GPIO[2] Config            | 7:4  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 3:2  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 1    | GPIO2 DIR                 | RW  | 1       | 0: Output<br>1: Input                                                                                                                                                                                              |
|            |                           | 0    | GPIO2 EN                  | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                                                                                                                                                         |
| 10         | GPIO[3] Config            | 7:4  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 3:2  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 1    | GPIO3 DIR                 | RW  | 1       | 0: Output<br>1: Input                                                                                                                                                                                              |
|            |                           | 0    | GPIO3 EN                  | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                                                                                                                                                         |
| 11         | GPIO[4] Config            | 7:4  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 3:2  | RESERVED                  |     | 0       | Reserved                                                                                                                                                                                                           |
|            |                           | 1    | GPIO4 DIR                 | RW  | 1       | 0: Output<br>1: Input                                                                                                                                                                                              |
|            |                           | 0    | GPIO4 EN                  | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                                                                                                                                                         |

**Table 1. DS92LX1621 Control Registers (continued)**

| Addr (Hex) | Name                        | Bits | Field                                                                                | R/W | Default | Description                |
|------------|-----------------------------|------|--------------------------------------------------------------------------------------|-----|---------|----------------------------|
| 12         | GPIO[5] Config              | 7:4  | RESERVED                                                                             |     | 0       | Reserved                   |
|            |                             | 3:2  | RESERVED                                                                             |     | 0       | Reserved                   |
|            |                             | 1    | GPIO5 DIR                                                                            | RW  | 1       | 0: Output<br>1: Input      |
|            |                             | 0    | GPIO5 EN                                                                             | RW  | 1       | 0: TRI-STATE<br>1: Enabled |
| 13         | General Purpose Control Reg | 7:0  | GPCR[7]<br>GPCR[6]<br>GPCR[5]<br>GPCR[4]<br>GPCR[3]<br>GPCR[2]<br>GPCR[1]<br>GPCR[0] | RW  | 0       | 0: LOW<br>1: HIGH          |

**Table 2. DS92LX1622 Control Registers**

| Addr (Hex) | Name                       | Bits | Field         | R/W | Default      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|----------------------------|------|---------------|-----|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0          | I <sup>2</sup> C Device ID | 7:1  | DEVICE ID     | RW  | 0x60h        | 7-bit address of Deserializer;<br>0x60h<br>(1100_000X) default                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|            |                            | 0    | DES ID        | RW  | 0            | 0: Device ID is from CAD<br>1: Register I <sup>2</sup> C Device ID overrides CAD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1          | Reset                      | 7:3  | RESERVED      |     | 0            | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|            |                            | 2    | REM_WAKEUP    | RW  | 0            | Remote Wake-up Select<br>1: Enable. Generate remote wakeup signal automatically wake-up the Serializer in Standby mode<br>0: Disable. Puts the Serializer (M/S = 0) in Standby mode when Deserializer M/S = 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|            |                            | 1    | DIGITALRESET0 | RW  | 0 self clear | 1: Resets the device to default register values. Does not affect device I <sup>2</sup> C Bus or Device ID                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|            |                            | 0    | DIGITALRESET1 | RW  | 0 self clear | 1: Digital Reset, retains all register values                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2          | Reserved                   | 7:6  |               |     | 0            | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|            | Auto Clock                 | 5    | AUTO_CLOCK    | RW  | 0            | 1: Output PCLK or Internal 25 MHz Oscillator clock<br>0: Only PCLK when valid PCLK present                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|            | OSS Select                 | 4    | OSS_SEL       | RW  | 0            | Output Sleep State Select<br>0: Outputs = TRI-STATE, when LOCK = L<br>1: Outputs = LOW, when LOCK = L                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|            | SSCG                       | 3:0  | SSCG          |     | 0            | SSCG Select<br>0000: Normal Operation, SSCG OFF<br>0001: fmod (KHz) PCLK/2168, fdev ±0.50%<br>0010: fmod (KHz) PCLK/2168, fdev ±1.00%<br>0011: fmod (KHz) PCLK/2168, fdev ±1.50%<br>0100: fmod (KHz) PCLK/2168, fdev ±2.00%<br>0101: fmod (KHz) PCLK/1300, fdev ±0.50%<br>0110: fmod (KHz) PCLK/1300, fdev ±1.00%<br>0111: fmod (KHz) PCLK/1300, fdev ±1.50%<br>1000: fmod (KHz) PCLK/1300, fdev ±2.00%<br>1001: fmod (KHz) PCLK/868, fdev ±0.50%<br>1010: fmod (KHz) PCLK/868, fdev ±1.00%<br>1011: fmod (KHz) PCLK/868, fdev ±1.50%<br>1100: fmod (KHz) PCLK/868, fdev ±2.00%<br>1101: fmod (KHz) PCLK/650, fdev ±0.50%<br>1110: fmod (KHz) PCLK/650, fdev ±1.00%<br>1111: fmod (KHz) PCLK/650, fdev ±1.50% |

**Table 2. DS92LX1622 Control Registers (continued)**

| Addr (Hex) | Name                            | Bits | Field                         | R/W | Default | Description                                                                                                                                                                                                                               |
|------------|---------------------------------|------|-------------------------------|-----|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3          | CRC Fault Tolerant Transmission | 7    | Tx CRC CHECK ENABLE           | RW  | 1       | Back Channel CRC Enable<br>0: Disable<br>1: Enable<br>For proper CRC operation, on Serailizer 0x03h b[6] control register must be Enabled.                                                                                                |
|            |                                 | 6    | Rx CRC GEN ENABLE             | RW  | 1       | Foward Channel CRC Enable<br>0: Disable<br>1: Enable For proper CRC operation, on Serailizer 0x03h b[7] control register must be Enabled.                                                                                                 |
|            | VDDIO Control                   | 5    | VDDIO CONTROL                 | RW  | 1       | Auto voltage control<br>0: Disable<br>1: Enable (auto detect mode)                                                                                                                                                                        |
|            | VDDIO Mode                      | 4    | VDDIO MODE                    | RW  | 0       | VDDIO voltage set<br>Only used when VDDIOCONTROL = 0<br>0: 1.8V<br>1: 3.3V                                                                                                                                                                |
|            | I <sup>2</sup> C Pass-Through   | 3    | I <sup>2</sup> C PASS-THROUGH | RW  | 1       | I <sup>2</sup> C Pass-Through Mode<br>0: Disabled<br>1: Enabled                                                                                                                                                                           |
|            | Auto ACK                        | 2    | AUTO ACK                      | RW  | 0       | 0: Disable<br>1: Enable                                                                                                                                                                                                                   |
|            | CRC Reset                       | 1    | CRC RESET                     | RW  | 0       | 1: CRC reset                                                                                                                                                                                                                              |
| 4          | RRFB                            | 0    | RRFB                          | RW  | 1       | Pixel Clock Edge Select<br>0: Parallel Interface Data is strobed on the Falling Clock Edge<br>1: Parallel Interface Data is strobed on the Rising Clock Edge.                                                                             |
|            |                                 |      |                               |     |         |                                                                                                                                                                                                                                           |
| 4          | EQ Feature Control1             | 7:0  | EQ                            | RW  | 0       | 00'h: ~0.0 dB<br>01'h: ~4.5 dB<br>03'h: ~6.5 dB<br>07'h: ~7.5 dB<br>0F'h: ~8.0 dB<br>1F'h: ~11.0 dB<br>3F'h: ~12.5 dB<br>FF'h: ~14.0 dB                                                                                                   |
| 5          | Reserved                        | 7:0  | RESERVED                      |     | 0       | Reserved                                                                                                                                                                                                                                  |
| 6          | Reserved                        | 7    | RESERVED                      |     | 0       | Reserved                                                                                                                                                                                                                                  |
|            | SCL Prescale                    | 6:4  | SCL_PRESCALE                  |     | 0       | Prescales the SCL clock line when reading data byte from a slave device (M/S = 0)<br>000 : ~100 kHz SCL (default)<br>001 : ~125 kHz SCL<br>101 : ~11 kHz SCL<br>110 : ~33 kHz SCL<br>111 : ~50 kHz SCL<br>Other values are NOT supported. |
|            | Remote NACK                     | 3    | REM_NACK_TIME R               | RW  | 1       | Remote NACK Timer Enable In slave mode (MODE = 1) if bit is set the I2C core will automatically timeout when no acknowledge condition was detected.<br>1: Enable<br>0: Disable                                                            |
|            | Remote NACK                     | 2:0  | NACK_TIMEOUT                  | RW  | 111'b   | Remote NACK Timeout.<br>000: 2.0 ms<br>001: 5.2 ms<br>010: 8.6 ms<br>011: 11.8 ms<br>100: 14.4 ms<br>101: 18.4 ms<br>110: 21.6 ms<br>111: 25.0 ms                                                                                         |

**Table 2. DS92LX1622 Control Registers (continued)**

| Addr (Hex) | Name                 | Bits | Field        | R/W | Default | Description                                                       |
|------------|----------------------|------|--------------|-----|---------|-------------------------------------------------------------------|
| 7          | SER ID               | 7:1  | SER DEV ID   | RW  | 0x58h   | Serializer Device ID = 0x58 (1011_000X) default                   |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 8          | ID[0] Index          | 7:1  | ID[0] INDEX  | RW  | 0       | Target slave Device ID slv_id1 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 9          | ID[1] Index          | 7:1  | ID[1] INDEX  | RW  | 0       | Target slave Device ID slv_id1 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| A          | ID[2] Index          | 7:1  | ID[2] INDEX  | RW  | 0       | Target slave Device ID slv_id2 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| B          | ID[3] Index          | 7:1  | ID[3] INDEX  | RW  | 0       | Target slave Device ID slv_id3 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| C          | ID[4] Index          | 7:1  | ID[4] INDEX  | RW  | 0       | Target slave Device ID slv_id4 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| D          | ID[5] Index          | 7:1  | ID[5] INDEX  | RW  | 0       | Target slave Device ID slv_id5 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| E          | ID[6] Index          | 7:1  | ID[6] INDEX  | RW  | 0       | Target slave Device ID slv_id6 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| F          | ID[7] Index          | 7:1  | ID[7] INDEX  | RW  | 0       | Target slave Device ID slv_id7 [7:1]                              |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 10         | ID[0] Match          | 7:1  | ID[0] MATCH  | RW  | 0       | Alias to match Device ID slv_id0 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 11         | ID[1] Match          | 7:1  | ID[1] MATCH  | RW  | 0       | Alias to match Device ID slv_id1 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 12         | ID[2] Match          | 7:1  | ID[2] MATCH  | RW  | 0       | Alias to match Device ID slv_id2 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 13         | ID[3] Match          | 7:1  | ID[3] MATCH  | RW  | 0       | Alias to match Device ID slv_id3 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved.                                                         |
| 14         | ID[4] Match          | 7:1  | ID[4] MATCH  | RW  | 0       | Alias to match Device ID slv_id4 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 15         | ID[5] Match          | 7:1  | ID[5] MATCH  | RW  | 0       | Alias to match Device ID slv_id5 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 16         | ID[6] Match          | 7:1  | ID[6] MATCH  | RW  | 0       | Alias to match Device ID slv_id6 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 17         | ID[7] Match          | 7:1  | ID[7] MATCH  | RW  | 0       | Alias to match Device ID slv_id7 [7:1]                            |
|            |                      | 0    | RESERVED     |     | 0       | Reserved                                                          |
| 18         | Reserved             | 7:0  | RESERVED     |     | 0       | Reserved                                                          |
| 19         | Reserved             | 7:0  | RESERVED     |     | 1       | Reserved                                                          |
| 1A         | CRC Errors           | 7:0  | CRC ERROR B0 | R   | 0       | Number of CRC errors 8 LSBs                                       |
| 1B         | CRC Errors           | 7:0  | CRC ERROR B1 | R   | 0       | Number of CRC errors 8 MSBs                                       |
| 1C         | Reserved             | 7:3  | RESERVED     |     | 0       | Reserved                                                          |
|            | CRC Check            | 2    | SER ERROR    | R   | 0       | CRC error during communication with Serializer on Forward Channel |
|            | Signal Detect Status | 1    |              | R   | 0       | 0: Active signal not detected<br>1: Active signal detected        |
|            | LOCK Pin Status      | 0    |              | R   | 0       | 0: CDR/PLL Unlocked<br>1: CDR/PLL Locked                          |

**Table 2. DS92LX1622 Control Registers (continued)**

| Addr (Hex) | Name                        | Bits | Field                                                                                | R/W | Default | Description                                                               |
|------------|-----------------------------|------|--------------------------------------------------------------------------------------|-----|---------|---------------------------------------------------------------------------|
| 1D         | GPIO[0] Config              | 7:3  | RESERVED                                                                             | RW  | 00010'b | Reserved                                                                  |
|            |                             | 2    | GPIO0 SET                                                                            | RW  | 1       | 1: Configured as GPIO<br>0: Configured as ROUT data (OSS_SEL controlled)  |
|            |                             | 1    | GPIO0 DIR                                                                            | RW  | 1       | 0: Output<br>1: Input                                                     |
|            |                             | 0    | GPIO0 EN                                                                             | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                |
| 1E         | GPIO[1] Config              | 7:3  | RESERVED                                                                             | RW  | 0       | Reserved                                                                  |
|            |                             | 2    | GPIO1 SET                                                                            | RW  | 1       | 1: Configured as GPIO<br>0: Configured as ROUT data (OSS_SEL controlled)  |
|            |                             | 1    | GPIO1 DIR                                                                            | RW  | 1       | 0: Output<br>1: Input                                                     |
|            |                             | 0    | GPIO1 EN                                                                             | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                |
| 1F         | GPIO[2] Config              | 7:3  | RESERVED                                                                             | RW  | 0       | Reserved                                                                  |
|            |                             | 2    | GPIO2 SET                                                                            | RW  | 0       | 1: Configured as GPIO<br>0: Configured as ROUT0 data (OSS_SEL controlled) |
|            |                             | 1    | GPIO2 DIR                                                                            | RW  | 0       | 0: Output<br>1: Input                                                     |
|            |                             | 0    | GPIO2 EN                                                                             | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                |
| 20         | GPIO[3] Config              | 7:3  | RESERVED                                                                             | RW  | 0       | Reserved                                                                  |
|            |                             | 2    | GPIO3 SET                                                                            | RW  | 0       | 1: Configured as GPIO<br>0: Configured as ROUT1 data (OSS_SEL controlled) |
|            |                             | 1    | GPIO3 DIR                                                                            | RW  | 0       | 0: Output<br>1: Input                                                     |
|            |                             | 0    | GPIO3 EN                                                                             | RW  | 1       | 0: Tri-state<br>1: Enabled                                                |
| 21         | GPIO[4] Config              | 7:3  | RESERVED                                                                             | RW  | 0       | Reserved                                                                  |
|            |                             | 2    | GPIO4 SET                                                                            | RW  | 0       | 1: Configured as GPIO<br>0: Configured as ROUT2 data (OSS_SEL controlled) |
|            |                             | 1    | GPIO4 DIR                                                                            | RW  | 0       | 0: Output<br>1: Input                                                     |
|            |                             | 0    | GPIO4 EN                                                                             | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                |
| 22         | GPIO[5] Config              | 7:3  | RESERVED                                                                             | RW  | 0       | Reserved                                                                  |
|            |                             | 2    | GPIO5 SET                                                                            | RW  | 0       | 1: Configured as GPIO<br>0: Configured as ROUT3 data (OSS_SEL controlled) |
|            |                             | 1    | GPIO5 DIR                                                                            | RW  | 0       | 0: Output<br>1: Input                                                     |
|            |                             | 0    | GPIO5 EN                                                                             | RW  | 1       | 0: TRI-STATE<br>1: Enabled                                                |
| 23         | General Purpose Control Reg | 7:0  | GPCR[7]<br>GPCR[6]<br>GPCR[5]<br>GPCR[4]<br>GPCR[3]<br>GPCR[2]<br>GPCR[1]<br>GPCR[0] | RW  | 0       | 0: LOW<br>1: HIGH                                                         |
| 24         | BIST                        | 0    | BIST_EN                                                                              | RW  | 0       | BIST Enable<br>0: Normal operation<br>1: Bist Enable                      |
| 25         | BIST_ERR                    | 7:0  | BIST_ERR                                                                             | R   | 0       | Bist Error Counter                                                        |

**Table 2. DS92LX1622 Control Registers (continued)**

| Addr (Hex) | Name               | Bits | Field         | R/W | Default | Description                                                                                    |
|------------|--------------------|------|---------------|-----|---------|------------------------------------------------------------------------------------------------|
| 26         | Remote Wake Enable | 7:6  | REM_WAKEUP_EN | RW  | 0       | 11: Enable remote wake up mode<br>00: Normal operation mode<br>Other values are NOT supported. |
|            |                    | 5:0  | RESERVED      | RW  | 0       | Reserved                                                                                       |
| 27         | BCC                | 7:0  | BCC           | RW  | 0       | 0xE0: Normal Operation Mode. Users MUST program this value.                                    |

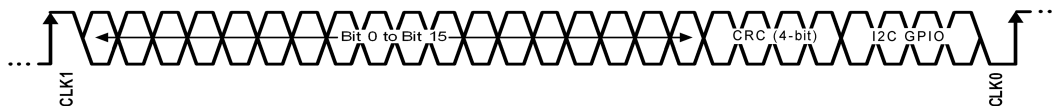
## FUNCTIONAL DESCRIPTION

The DS92LX1621 / DS92LX1622 Channel Link III chipset is intended for camera applications. The Serializer/Deserializer chipset operates from a 10 MHz to 50 MHz pixel clock frequency. The DS92LX1621 transforms a 16-bit wide parallel LVCMOS data bus along with a bi-directional control bus into a single high-speed differential pair. The high speed serial bit stream contains an embedded clock and DC-balance information which enhances signal quality to support AC coupling. The DS92LX1622 receives the single serial data stream and converts it back into a 16-bit wide parallel data bus together with the bi-directional control bus.

The bi-directional channel function of the DS92LX1621 / DS92LX1622 provides bi-directional communication between the image sensor and the host device (FPGA, frame grabber, display, etc.). The integrated back channel transfers data bi-directionally over the same differential pair used for video data interface. This interface offers advantages over other chipsets by eliminating the need for additional wires for programming and control. The bi-directional control channel is controlled via an I<sup>2</sup>C port. The bi-directional control channel offers asynchronous communication and is not dependent on video blanking intervals.

## SERIAL FRAME FORMAT

The DS92LX1621 / DS92LX1622 chipset will transmit and receive a pixel of data in the following format:



**Figure 24. Serial Bitstream for 28-bit Symbol**

The High Speed Forward Channel (HS\_FC) is a 28-bit symbol composed of 16 bits of data containing camera data & control information transmitted from Serializer to Deserializer. CLK1 and CLK0 represent the embedded clock in the serial stream. CLK1 is always HIGH and CLK0 is always LOW. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled. The data payload may be checked using a 4-bit CRC function. The CRC monitors the link integrity of the serialized data and reports when an error condition is detected.

The bi-directional control data is transferred over the single serial link along with the high-speed forward data. This architecture provides a full duplex low speed forward and backward path across the serial link together with a high speed forward channel without the dependence of the video blanking phase.

## DESCRIPTION OF BI-DIRECTIONAL CONTROL BUS AND I<sup>2</sup>C MODES

The I<sup>2</sup>C compatible interface allows programming of the DS92LX1621, DS92LX1622, or an external remote device (such as a camera) through the bi-directional control channel. Register programming transactions to/from the DS92LX1621 / DS92LX1622 chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and both lines must be pulled-up to VDDIO by external resistor. [Figure 6](#) shows the timing relationships of the clock (SCL) and data (SDA) signals. Pull-up resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS92LX1621 / DS92LX1622 I<sup>2</sup>C bus data rate supports up to 100 kbps according to I<sup>2</sup>C specification.

To start any data transfer, the DS92LX1621 / DS92LX1622 must be configured in the proper I<sup>2</sup>C mode. Each device can function as an I<sup>2</sup>C slave proxy or master proxy depending on the mode determined by M/S pin. The Ser/Des interface acts as a virtual bridge between Master controller (MCU) and the remote device. When the M/S pin is set to HIGH, the device is treated as a slave proxy; acts as a slave on behalf of the remote slave. When addressing a remote peripheral or Serializer/Deserializer (not wired directly to the MCU), the slave proxy will forward any byte transactions sent by the Master controller to the target device. When M/S pin is set to LOW, the device will function as a master proxy device; acts as a master on behalf of the I<sup>2</sup>C master controller. Note that the devices must have complementary settings for the M/S configuration. For example, if the Serializer M/S pin is set to HIGH then the Deserializer M/S pin must be set to LOW and vice-versa.

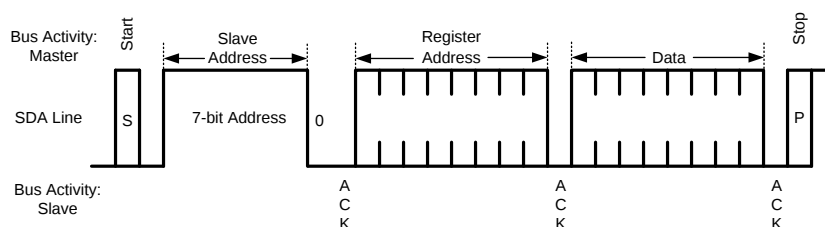


Figure 25. Write Byte

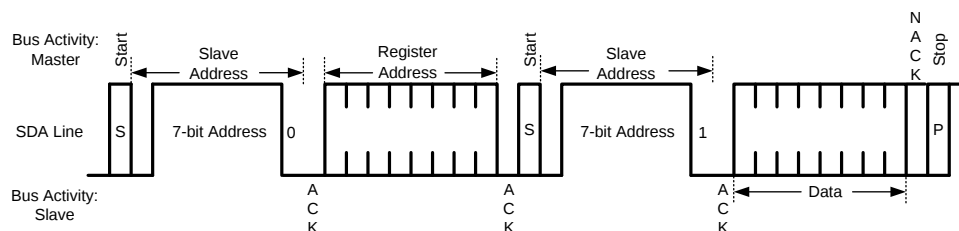


Figure 26. Read Byte

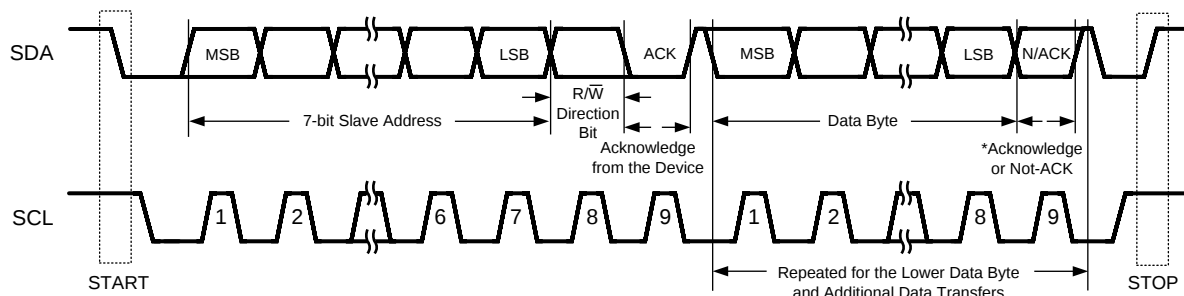


Figure 27. Basic Operation

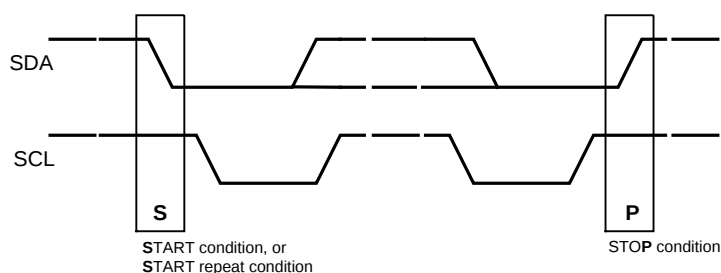


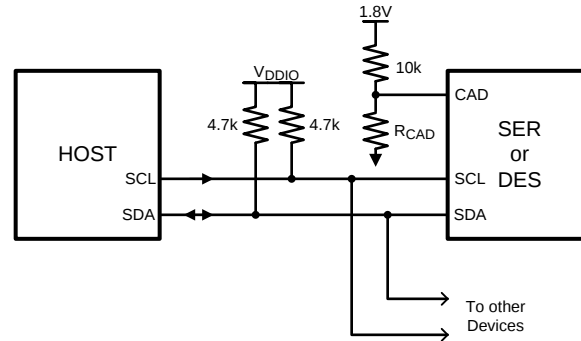
Figure 28. START and STOP Conditions

## SLAVE CLOCK STRETCHING

In order to communicate and synchronize with remote devices on the I<sup>2</sup>C bus through the bi-directional control channel, slave clock stretching must be supported by the I<sup>2</sup>C master controller/MCU. The chipset utilizes bus clock stretching (holding the SCL line low) during data transmission; where the I<sup>2</sup>C slave pulls the SCL line low prior to the 9th clock of every I<sup>2</sup>C data transfer (before the ACK signal). The slave device will not control the clock and only stretches it until the remote peripheral has responded; which is typically in the order of 12  $\mu$ s (typical).

## CAD PIN ADDRESS DECODER

The CAD pin is used to decode and set the physical slave address of the Serializer/Deserializer (I<sup>2</sup>C only) to allow up to six devices on the bus using only a single pin. The pin sets one of six possible addresses for each Serializer/Deserializer device. The pin must be pulled to VDD (1.8V, NOT VDDIO)) with a 10 kΩ resistor and a pull down resistor (RID) of the recommended value to set the physical device address. The recommended maximum resistor tolerance is 0.1% worst case (0.2% total tolerance).



**Figure 29. Serial Control Bus Connection**

**Table 3. CAD Resistor Value - DS92LX1621 Ser**

| Resistor RID Ω<br>(±0.1%) | Address 7'b         | Address 8'b 0 appended (WRITE) |
|---------------------------|---------------------|--------------------------------|
| 0<br>GND                  | 7b' 101 1000 (h'58) | 8b' 1011 0000 (h'B0)           |
| 2.0k                      | 7b' 101 1001 (h'59) | 8b' 1011 0010 (h'B2)           |
| 4.7k                      | 7b' 101 1010 (h'5A) | 8b' 1011 0100 (h'B4)           |
| 8.2k                      | 7b' 101 1011 (h'5B) | 8b' 1011 0110 (h'B6)           |
| 12.1k                     | 7b' 101 1100 (h'5C) | 8b' 1011 1000 (h'B8)           |
| 39.0k                     | 7b' 101 1110 (h'5E) | 8b' 1011 1100 (h'BC)           |

**Table 4. CAD Resistor Value - DS92LX1622 Des**

| Resistor RID Ω<br>(±0.1%) | Address 7'b         | Address 8'b 0 appended (WRITE) |
|---------------------------|---------------------|--------------------------------|
| 0<br>GND                  | 7b' 110 0000 (h'60) | 8b' 1100 0000 (h'C0)           |
| 2.0k                      | 7b' 110 0001 (h'61) | 8b' 1100 0010 (h'C2)           |
| 4.7k                      | 7b' 110 0010 (h'62) | 8b' 1100 0100 (h'C4)           |
| 8.2k                      | 7b' 110 0011 (h'63) | 8b' 1101 0110 (h'C6)           |
| 12.1k                     | 7b' 110 0100 (h'64) | 8b' 1101 1000 (h'C8)           |
| 39.0k                     | 7b' 110 0110 (h'66) | 8b' 1100 1100 (h'CC)           |

## CAMERA MODE OPERATION

In Camera mode, I<sup>2</sup>C transactions originate from the Master controller at the Deserializer side. The I<sup>2</sup>C slave core in the Deserializer will detect if a transaction is intended for the Serializer or a slave at the Serializer. Commands are sent over the bi-directional control channel to initiate the transactions. The Serializer will receive the command and generate an I<sup>2</sup>C transaction on its local I<sup>2</sup>C bus. At the same time, the Serializer will capture the response on the I<sup>2</sup>C bus and return the response on the forward channel link. The Deserializer parses the response and passes the appropriate response to the Deserializer I<sup>2</sup>C bus.

To configure the devices for camera mode operation, set the Serializer M/S pin to LOW and the Deserializer M/S pin to HIGH. Before initiating any I<sup>2</sup>C commands, the Deserializer needs to be programmed with the target slave device addresses and Serializer device address. SER\_DEV\_ID Register 0x07h sets the Serializer device address and SLAVE\_x\_MATCH/SLAVE\_x\_INDEX registers 0x08h–0x17h set the remote target slave addresses. In slave mode the address register is compared with the address byte sent by the I<sup>2</sup>C master. If the addresses are equal to any of registers values, the I<sup>2</sup>C slave will acknowledge and hold the bus to propagate the transaction to the target device otherwise it returns no acknowledge.

## DISPLAY MODE OPERATION

In Display mode, I<sup>2</sup>C transactions originate from the controller attached to the Serializer. The I2C slave core in the Serializer will detect if a transaction targets (local) registers within the Serializer or the (remote) registers within the Deserializer or a remote slave connected to the I<sup>2</sup>C master interface of the Deserializer. Commands are sent over the forward channel link to initiate the transactions. The Deserializer will receive the command and generate an I<sup>2</sup>C transaction on its local I2C bus. At the same time, the Deserializer will capture the response on the I<sup>2</sup>C bus and return the response as a command on the bi-directional control channel. The Serializer parses the response and passes the appropriate response to the Serializer I<sup>2</sup>C bus.

The physical device ID of the I<sup>2</sup>C slave in the Serializer is determined by the analog voltage on the ID[x] input. It can be reprogrammed by using the DEVICE\_ID register and setting the bit . The device ID of the logical I2C slave in the Deserializer is determined by programming the DES ID in the Serializer. The state of the CAD] input on the Deserializer is used to set the device ID. The I<sup>2</sup>C transactions between Ser/Des will be bridged between the host controller to the remote slave.

To configure the devices for display mode operation, set the Serializer M/S pin to HIGH and the Deserializer M/S pin to LOW. Before initiating any I<sup>2</sup>C commands, the Serializer needs to be programmed with the target slave device address and Serializer device address. DES\_DEV\_ID Register 0x06h sets the Deserializer device address and SLAVE\_DEV\_ID register 0x7h sets the remote target slave address. If the I<sup>2</sup>C slave address matches any of registers values, the I<sup>2</sup>C slave will hold the transaction allowing read or write to target device. Note: In Display mode operation, registers 0x08h–0x17h on Deserializer must be reset to 0x00.

## CRC (CYCLIC REDUNDANCY CHECK)

A 4-bit CRC per symbol is reserved for checking the link integrity during transmission. The reporting status pin (PASS) is provided on the Deserializer side, which flags any mismatch of data transmitted to and from the remote device. The Deserializer's PLL must first be locked (LOCK pin is HIGH) to ensure the PASS status is valid. This error detection handling generates an interrupt signal onto the PASS output pin; notifying the host controller as soon as any errors are identified. When an error occurs, the PASS will asserts LOW. An adjustable interrupt threshold register is also available for managing the data flow.

## ERROR DETECTION

The DS92LX1621 / DS92LX1622 chipset provides several error detection operations for ensuring data integrity in long distance transmission and reception. The data error detection function offers user flexibility and usability of performing bit-by-bit and data transmission error checking. The error detection operating modes support data validation of the following signals:

- Bi-directional Control Channel control data detection across serial link
- Control VSYNC and HSYNC signals across serial link
- Parallel video/pixel data across serial link

## PROGRAMMABLE CONTROLLER

An integrated I<sup>2</sup>C slave controller is embedded in each of the DS92LX1621 Serializer and DS92LX1622 Deserializer. It must be used to access and program the extra features embedded within the configuration registers. Refer to [Table 1](#) and [Table 2](#) for details of control registers.

## MULTIPLE DEVICE ADDRESSING

Some applications require multiple camera devices with the same fixed address to be accessed on the same I<sup>2</sup>C bus. The DS92LX1621 / DS92LX1622 provide slave ID matching/aliasing to generate different target slave addresses when connecting more than two identical devices together on the same bus. This allows the slave devices to be independently addressed. Each device connected to the bus is addressable through a unique ID by programming of the SLAVE\_ID\_MATCH register on Deserializer. This will remap the SLAVE\_ID\_MATCH address to the target SLAVE\_ID\_INDEX address; up to 8 ID indexes are supported. The host controller must keep track of the list of I<sup>2</sup>C peripherals in order to properly address the target device. In a camera application, the microcontroller is located on the Deserializer side. In this case, the microcontroller programs the slave address matching registers and handles all data transfers to and from all slave I<sup>2</sup>C devices. This is useful in the event where camera modules are removed or replaced. For example in the configuration shown in Figure 30:

- Host device (FPGA, frame grabber, etc.) is the I<sup>2</sup>C master and has an I<sup>2</sup>C master interface
- The I<sup>2</sup>C protocol is bridged from DES A to SER A and from DES B to SER B
- The I<sup>2</sup>C interfaces in SER A and SER B are both master interfaces

If the master controller transmits I<sup>2</sup>C slave 0xA0, the DES A address 0xE0 will forward the transaction to remote Camera A. If the controller transmits slave address 0xA2, the DES B 0xE2 will recognize that 0xA2 is mapped to 0xA0 and will be transmitted to the remote Camera B. If controller sends command to address 0xB2, the DES B 0xE2 will forward transaction to slave device 0xB0.

The Slave ID index/match is supported only in the camera mode (SER: M/S pin = L; DES: M/S pin = H). For Multiple device addressing in display mode (SER: M/S pin = H; DES: M/S pin = L), use the I<sup>2</sup>C pass through function.

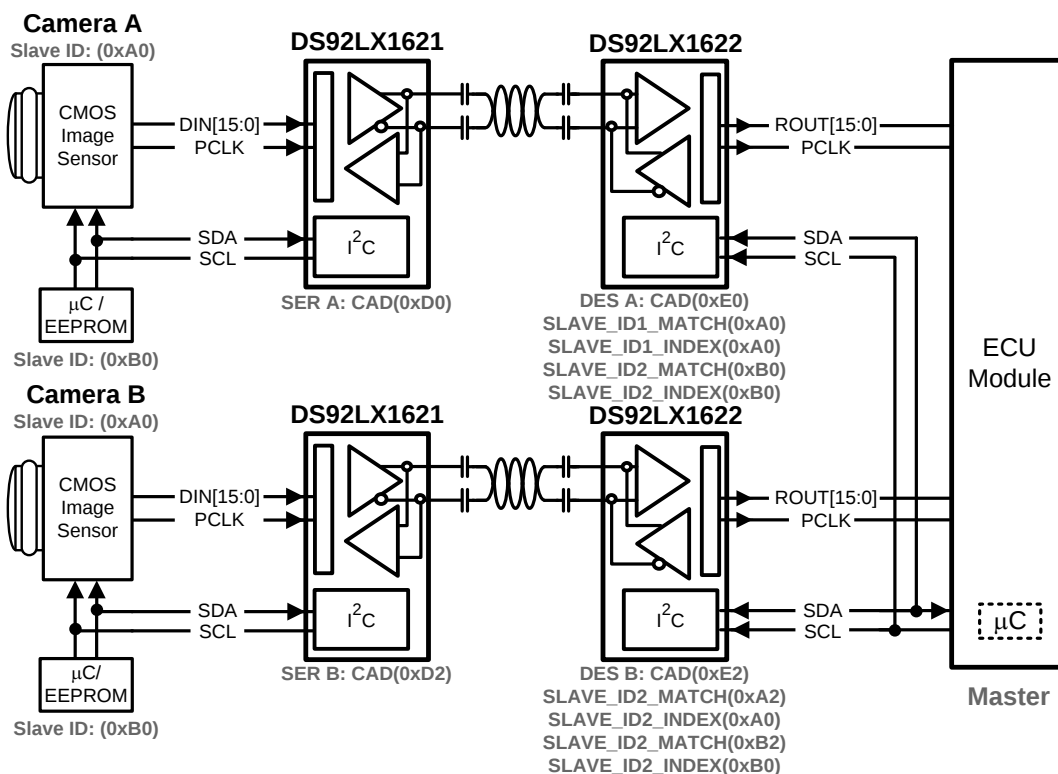


Figure 30. Multiple Device Addressing

## I<sup>2</sup>C PASS THROUGH

I<sup>2</sup>C pass-through provides an alternative means to independently address slave devices. The mode enables or disables I<sup>2</sup>C bidirectional control channel communication to the remote I<sup>2</sup>C bus. This option is used to determine whether or not an I<sup>2</sup>C instruction is to be transferred over to the remote I<sup>2</sup>C device. When enabled, the I<sup>2</sup>C bus traffic will continue to pass through and will be received by I<sup>2</sup>C devices downstream. If disabled, I<sup>2</sup>C commands will be blocked to the remote I<sup>2</sup>C device. The pass through function also provides access and communication to only specific devices on the remote bus. The feature is effective for both Camera mode and Display mode.

For example in the configuration shown in [Figure 31](#):

If master controller transmits I<sup>2</sup>C transaction for address 0xA0, the SER A with I<sup>2</sup>C pass through enabled will transfer I<sup>2</sup>C commands to remote Camera A. The SER B with I<sup>2</sup>C pass through disabled, any I<sup>2</sup>C commands will be bypassed on the I<sup>2</sup>C bus to Camera B.

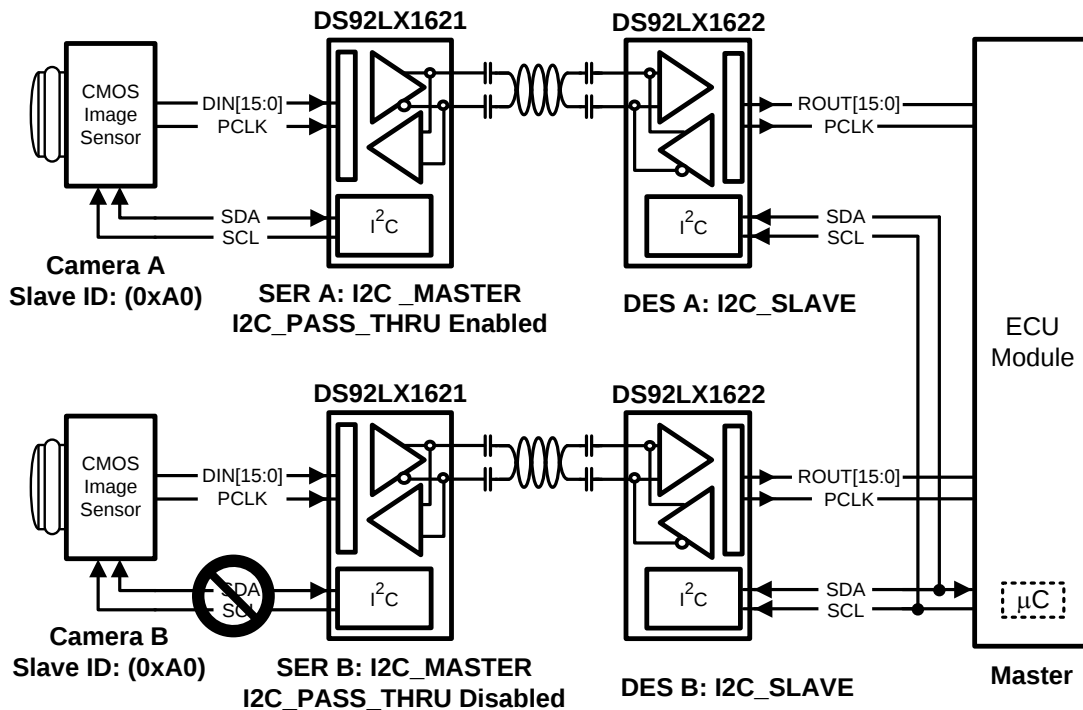


Figure 31. I<sup>2</sup>C Pass Through

## SYNCHRONIZING MULTIPLE CAMERAS

For applications requiring multiple cameras for frame-synchronization, it is recommended to utilize the General Purpose Input/Output (GPIO) pins to transmit control signals to synchronize multiple cameras together. To synchronize the cameras properly, the system controller needs to provide a field sync output (such as a vertical or frame sync signal) and the cameras must be set to accept an auxiliary sync input. The vertical synchronize signal corresponds to the start and end of a frame and the start and end of a field. Note this form of synchronization timing relationship has a non-deterministic latency. After the control data is reconstructed from the bi-directional control channel, there will be a time variation of the GPIO signals arriving at the different target devices (between the parallel links). The maximum latency delta ( $t_1$ ) of the GPIO data transmitted across multiple links is 25  $\mu$ s.

Note: The user must verify that the timing variations between the different links are within their system and timing specifications.

For example in the configuration shown in [Figure 32](#):

The maximum time ( $t_1$ ) between the rising edge of GPIO (i.e. sync signal) arriving at Camera A and Camera B is 25  $\mu$ s.

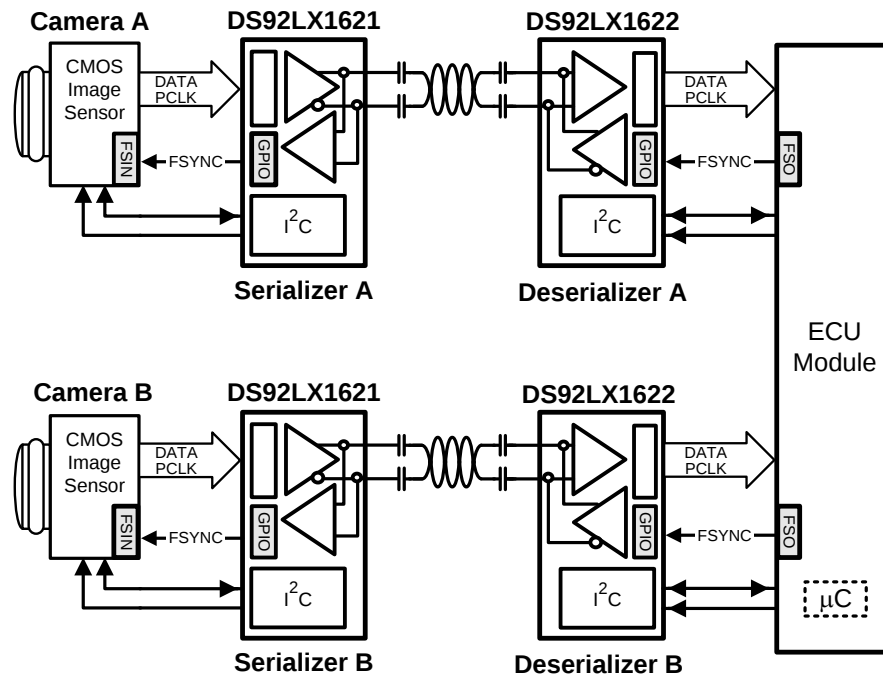


Figure 32. Synchronizing Multiple Cameras

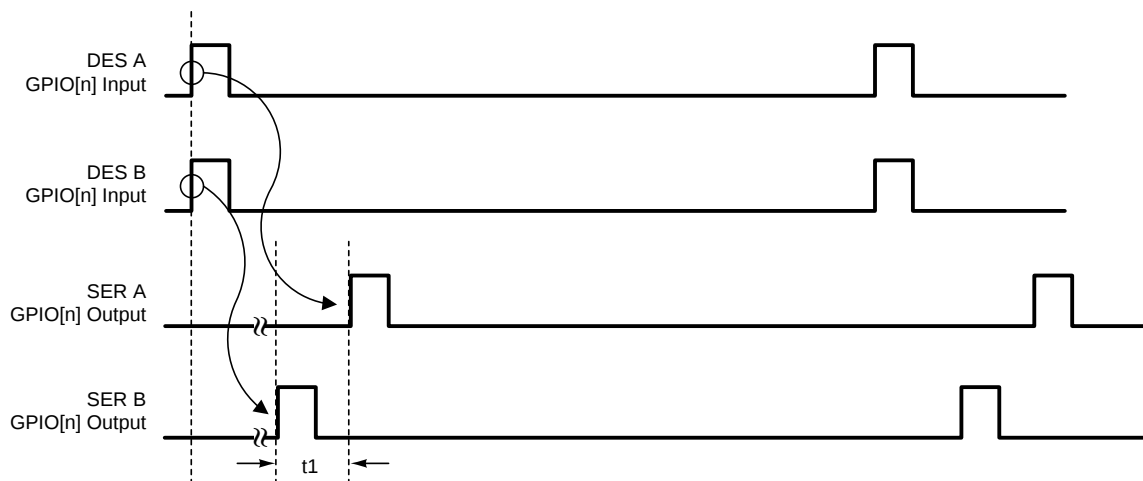


Figure 33. GPIO Delta Latency

### GENERAL PURPOSE I/O (GPIO)

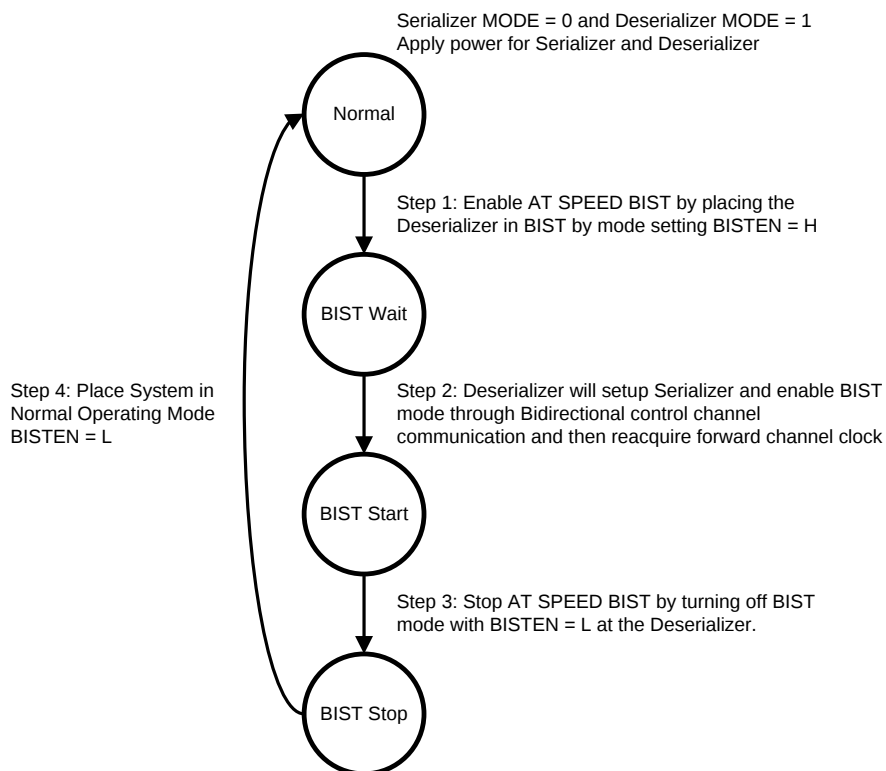
The DS92LX1621 / DS92LX1622 has up to 6 GPIO (2 dedicated and 4 programmable). GPIO[0] and GPIO[1] are always available and GPIO[2:5] are available depending on the parallel data bus size. DIN/ROUT[0:3] can be programmed into GPIOs (GPIO[2:5]) when the parallel data bus is less than 12 bits wide (10-bit data + HS,VS). Each GPIO can be configured as either an input or output port. The GPIO maximum switching rate is up to 66 kHz when configured for communication between Deserializer GPI to Serializer GPO. Whereas data flow configured for communication between Serializer GPI to Deserializer GPO is limited by the maximum data rate of the PCLK.

## AT-SPEED BIST (BISTEN, PASS)

An optional AT SPEED Built in Self Test (BIST) feature supports at speed testing of the high-speed serial and the bidirectional control channel link. Control pins at the Deserializer are used to enable the BIST test mode and allow the system to initiate the test and set the duration. A HIGH on PASS pin indicates that all payloads received during the test were error free during the BIST duration test. A LOW on this pin at the conclusion of the test indicates that one or more payloads were detected with errors.

The BIST duration is defined by the width of BISTEN. BIST starts when Deserializer LOCK goes HIGH and BISTEN is set HIGH. BIST ends when BISTEN goes LOW. Any errors detected after the BIST Duration are not included in PASS logic. Note: AT-SPEED BIST is only available in the Camera mode and not the Display mode.

The following diagram shows how to perform system AT SPEED BIST:



**Figure 34. AT-SPEED BIST System Flow Diagram**

*Step 1: Place the Deserializer in BIST Mode.*

Serializer and Deserializer power supply must be supplied. Enable the AT SPEED BIST mode on the Deserializer by setting the BISTEN pin High. The DS92LX1622 GPIO[1:0] pins are used to select the PCLK frequency of the on-chip oscillator for the BIST test on high speed data path.

**Table 5. BIST Oscillator Frequency Select**

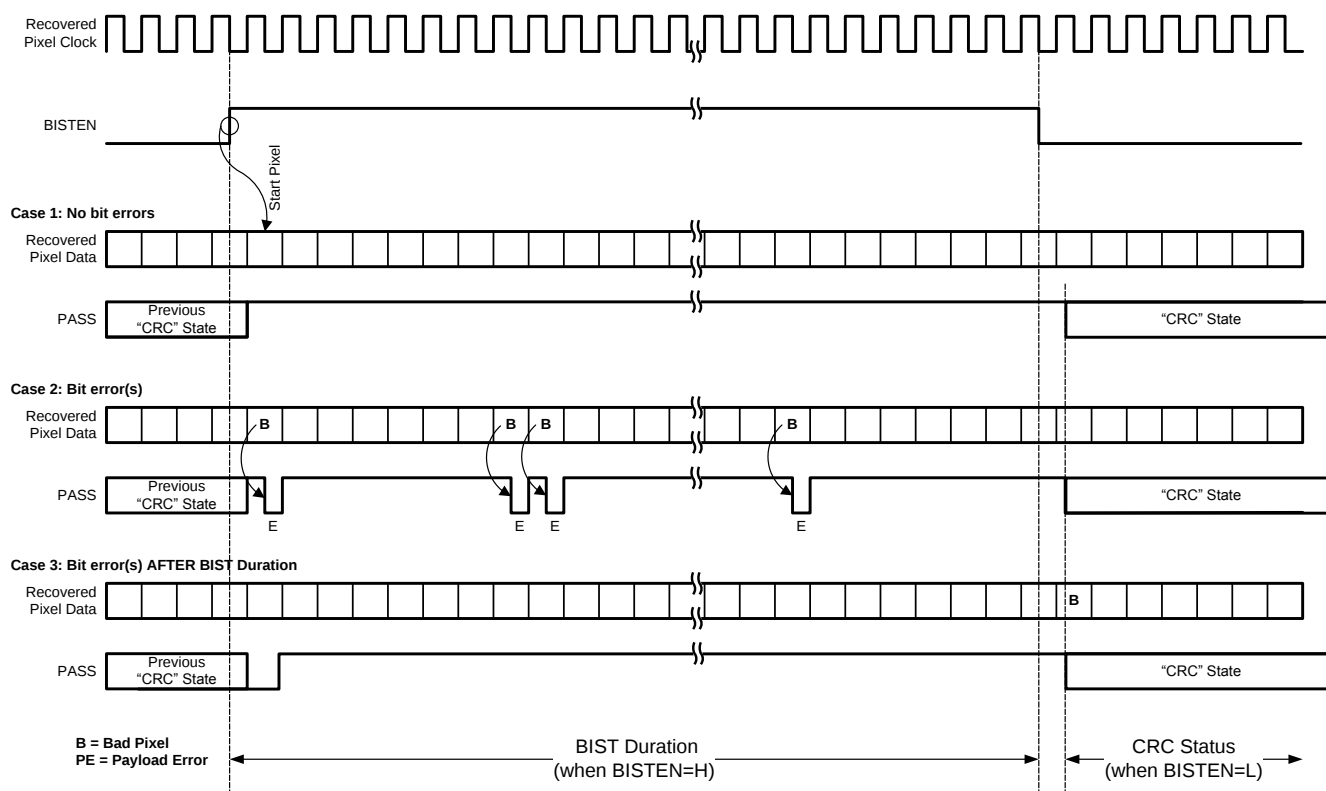
| DES GPIO [1:0] | Oscillator Source | min (MHz) | typ (MHz) | max (MHz) |
|----------------|-------------------|-----------|-----------|-----------|
| 00             | External PCLK     | 10        |           | 50        |
| 01             | Internal          |           | 50        |           |
| 10             | Internal          |           | 25        |           |
| 11             | Internal          |           | 12.5      |           |

The Deserializer GPIO[1:0] set to 00 will bypass the on-chip oscillator and an external oscillator to Serializer PCLK input is required. This allows the user to operate BIST under different frequencies other than the predefined ranges.

*Step 2: Enable AT SPEED BIST by placing the Serializer into BIST mode.*

The deserializer will communicate through the back-channel to configure Serializer into BIST mode. Once the BIST mode is set, the Serializer will initiate BIST transmission to the Deserializer.

Wait 10 ms for Deserializer to acquire lock and then monitor the LOCK pin transition from LOW to HIGH. At this point, AT SPEED BIST is operational and the BIST process has begun. The Serializer will start transfer of an internally generated PRBS data pattern through the high speed serial link. This pattern traverses across the interconnecting link to the Deserializer. Check the status of the PASS pin; a HIGH indicates a pass, a LOW indicates a fail. A fail will stay LOW for ½ a clock cycle. If two or more bits fail in a row the PASS pin will toggle ½ clock cycle HIGH and ½ clock cycle low. The user can use the PASS pin to count the number of fails on the high speed link. In addition, there is a defined SER and DES register that will keep track of the accumulated error count. The Serializer DS92LX1621 GPIO[0] pin will be assigned as a PASS flag error indicator for the bi-directional control channel link.



**Figure 35. BIST Timing Diagram**

*Step 3: Stop at SPEED BIST by turning off BIST mode in the Deserializer to determine Pass/Fail.*

To end BIST, the system must pull BISTEN pin of the Deserializer LOW. The BIST duration is fully defined by the BISTEN width and thus the Bit Error Rate is determined by how long the system holds BISTEN HIGH.

$$\frac{\text{BIST Duration (s)}}{1 \text{ Pixel period (ns)} \times \text{Total Bits}} = \text{BIST Duration (s)} \times \frac{f_{\text{pixel}} \text{ (MHz)}}{\text{Pixel}} \times \text{Total Pixels Transmitted} = \text{Total Bits Transmitted}$$

$$\begin{aligned} \bullet \text{ Bit (Pixel) Error Rate (for passing BIST)} &= [\text{Total Bits Transmitted}]^{-1} \\ &= [\text{Total Bits Transmitted} \times \text{Bits/Pixel}]^{-1} \end{aligned}$$

**Figure 36. BIST BER Calculation**

For instance, if BISTEN is held HIGH for 1 second and the PCLK is running at 43 MHz with 16 bpp, then the Bit Error Rate is no better than 1.46E-9.

*Step 4: Place system in Normal Operating Mode by disabling BIST at the Serializer.*

Once Step 3 is complete, AT SPEED BIST is over and the Deserializer is out of BIST mode. To fully return to Normal mode, apply Normal input data into the Serializer.

Any PASS result will remain unless it is changed by a new BIST session or cleared by asserting and releasing PDB. The default state of PASS after a PDB toggle is HIGH.

It is important to note that AT SPEED BIST will only determine if there is an issue on the link that is not related to the clock and data recovery of the link (whose status is flagged with LOCK pin).

## LVCMOS VDDIO OPTION

1.8V or 3.3V SER Inputs and DES Outputs are user configurable to provide compatibility with 1.8V and 3.3V system interfaces.

## REMOTE WAKE UP (Camera Mode)

After initial power up, the SER is in a low-power Standby mode. The DES (controlled by host controller) 'Remote Wake-up' register allows the DES side to generate a signal across the link to remotely wake-up the SER. Once the SER detects the wake-up signal, the SER switches from Standby mode to active mode. In active mode, the SER locks onto PCLK input (if present), otherwise the on-chip oscillator is used as the input clock source. Note the host controller should monitor the DES LOCK pin and confirm LOCK = H before performing any I<sup>2</sup>C communication across the link.

For Remote Wake-up to function properly:

- The chipset needs to be configured in Camera mode: SER M/S = 0 and DES M/S = 1
- The SER expects remote wake-up by default at power on.
- Configure the control channel driver of the DES to be in remote wake up mode by setting DES register 0x26 to 0xC0.
- Perform remote wake up on SER by setting DES register 0x01 b[2] to 1.
- Return the control channel driver of the DES to the normal operation mode by setting DES register 0x26 to 0.

The SER can also be put into standby mode by programming the DES remote wake up control register 0x01 b[2] REM\_WAKEUP to 0.

## POWERDOWN

The SER has a PDB input pin to ENABLE or Powerdown the device. The modes can be controlled by the host and is used to disable the link to save power when the remote device is not operational. An auto mode is also available. In this mode, the PDB pin is tied HIGH and the SER switches over to an internal oscillator when the PCLK stops or not present. When a PCLK starts again, the SER will then lock to the valid input PCLK and transmits the data to the DES. In powerdown mode, the high-speed driver outputs are static (HIGH).

The DES has a PDB input pin to ENABLE or Powerdown the device. This pin can be controlled by the system and is used to disable the DES to save power. An auto mode is also available. In this mode, the PDB pin is tied HIGH and the DES will enter powerdown when the serial stream stops. When the serial stream starts up again, the DES will lock to the input stream and assert the LOCK pin and output valid data. In powerdown mode, the Data and PCLK outputs are set by the OSS\_SEL control register.

## POWER UP REQUIREMENTS AND PDB PIN

It is required to delay and release the PDB input signal after VDD (VDDn and VDDIO) power supplies have settled to the recommended operating voltages. A external RC network can be connected to the PDB pin to ensure PDB arrives after all the VDD have stabilized.

## SIGNAL QUALITY ENHANCERS

### Des - Receiver Input Equalization (EQ)

The receiver inputs provided input equalization filter in order to compensate for loss from the media. The level of equalization is controlled via register setting.

## EMI REDUCTION

### Des - Receiver Staggered Output

The Receiver staggered outputs allows for outputs to switch in a random distribution of transitions within a defined window. Outputs transitions are distributed randomly. This minimizes the number of outputs switching simultaneously and helps to reduce supply noise. In addition it spreads the noise spectrum out reducing overall EMI.

### Des Spread Spectrum Clocking Compatibility

The DS92LX1622 parallel data and clock outputs have programmable SSCG ranges from 9 kHz–66 kHz and  $\pm 0.5\%$ – $\pm 2\%$  from 20 MHz to 50 MHz. The modulation rate and modulation frequency variation of output spread is controlled through the SSC control registers.

### PIXEL CLOCK EDGE SELECT (TRFB/RRFB)

The TRFB/RRFB selects which edge of the Pixel Clock is used. For the SER, this register determines the edge that the data is latched on. If TRFB register is 1, data is latched on the Rising edge of the PCLK. If TRFB register is 0, data is latched on the Falling edge of the PCLK. For the DES, this register determines the edge that the data is strobed on. If RRFB register is 1, data is strobed on the Rising edge of the PCLK. If RRFB register is 0, data is strobed on the Falling edge of the PCLK.

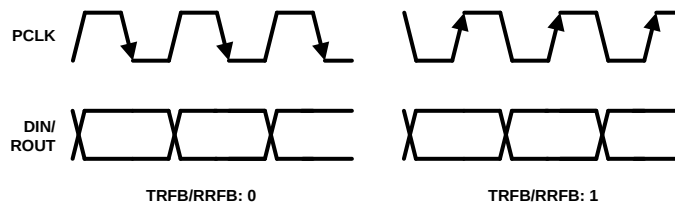


Figure 37. Programmable PCLK Strobe Select

## Applications Information

### AC COUPLING

The SER/DES supports only AC-coupled interconnects through an integrated DC balanced decoding scheme. To use the device in an AC-coupled application, insert external AC coupling capacitors in series in the Channel Link III signal path as illustrated in Figure 38.

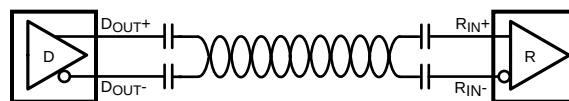


Figure 38. AC-Coupled Application

For high-speed Channel Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics. The most common used capacitor value for the interface is 0.1 $\mu$ F.

## TYPICAL APPLICATION CONNECTION

Figure 39 shows a typical connection of the DS92LX1621 Serializer.

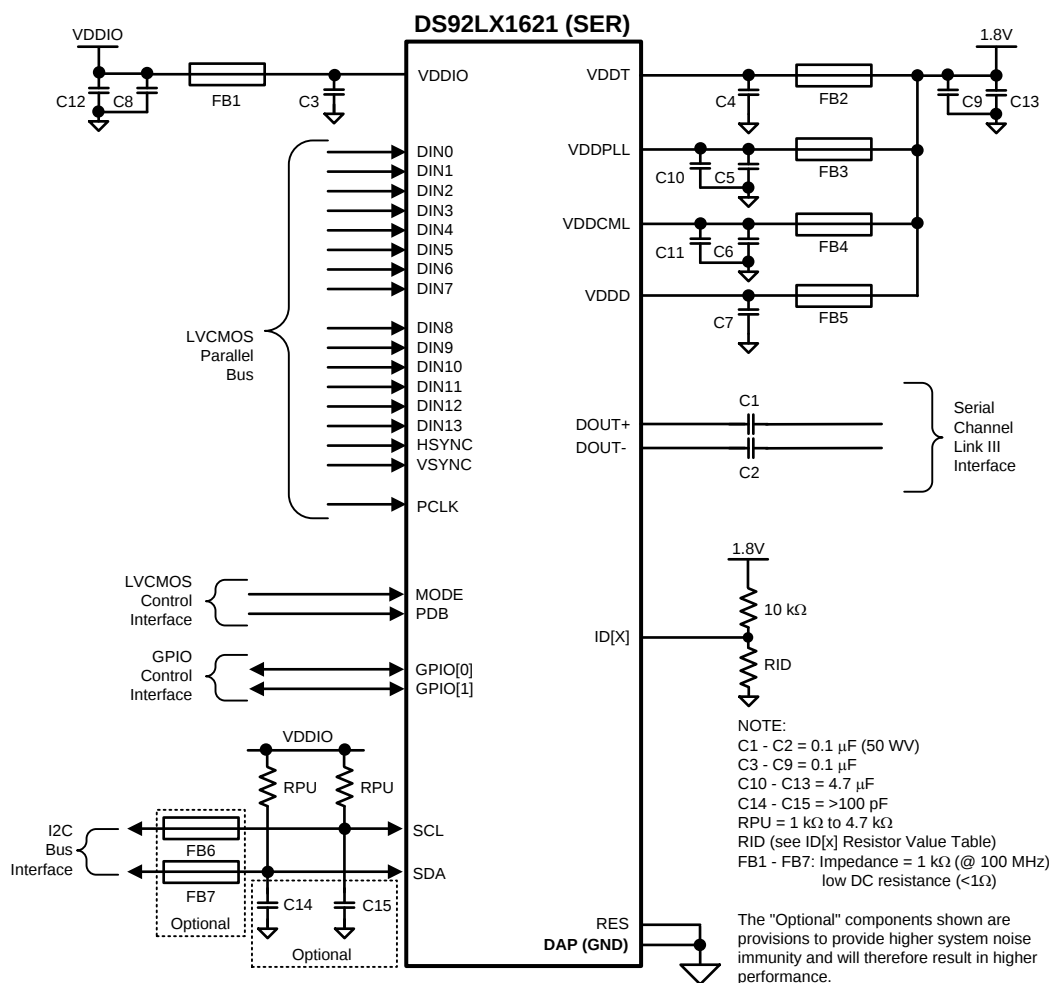


Figure 39. DS92LX1621 Typical Connection Diagram

Figure 40 shows a typical connection of the DS92LX1622 Deserializer.

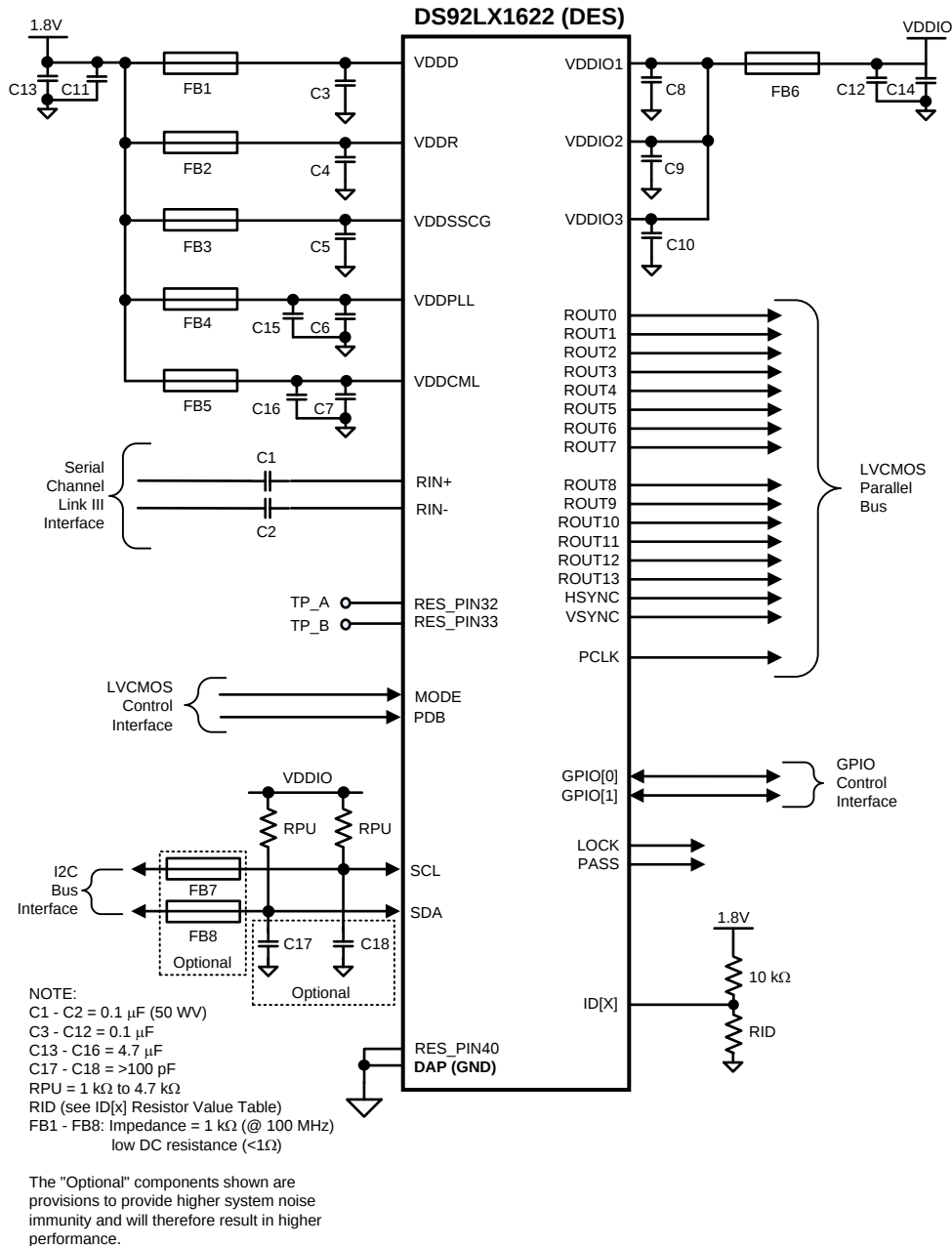


Figure 40. DS92LX1622 Typical Connection Diagram

## TRANSMISSION MEDIA

The Ser/Des chipset is intended to be used over a wide variety of balanced cables depending on distance and signal quality requirements. The Ser/Des employ internal termination providing a clean signaling environment. The interconnect for Channel Link III interface should present a differential impedance of 100 Ohms. Use of cables and connectors that have matched differential impedance will minimize impedance discontinuities. Shielded or un-shielded cables may be used depending upon the noise environment and application requirements. The chipset's optimum cable drive performance is achieved at 43 MHz at 10 meters length. The maximum signaling rate increases as the cable length decreases. Therefore, the chipset supports 50 MHz at shorter distances.

Other cable parameters that may limit the cable's performance boundaries are: cable attenuation, near-end crosstalk and intra-pair skew.

For obtaining optimal performance, the following is recommended:

- Use Shielded Twisted Pair (STP) cable
- $100\Omega \pm 10\%$  differential impedance and 24 AWG (or lower AWG) cable
- Low intra-pair skew (less than 0.1UI), impedance matched
- Terminate unused conductors
- Optimum settings for deserializer Register 0x27 (See [Table 2](#))

## PCB LAYOUT AND POWER SYSTEM CONSIDERATIONS

Circuit board layout and stack-up for the Ser/Des devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Closely-coupled differential lines of 100 Ohms are typically recommended for differential interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the LLP style package is provided in the *AN-1187 Leadless Leadframe Package (LLP) Application Report* (literature number [SNOA401](#)).

## INTERCONNECT GUIDELINES

For full details, see the *Channel-Link PCB and Interconnect Design-In Guidelines* (literature number [SNLA008](#)) and the *Transmission Line RAPIDESIGNER Operation and Applications Guide* (literature number [SNLA035](#)).

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the *LVDS Owner's Manual* (literature number [SNLA187](#)), which is available in PDF format from the TI [LVDS & CML Solutions](#) web site.

## REVISION HISTORY

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**Changes from Revision H (April 2013) to Revision I****Page**

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- Changed "tri-state" and "low" OSS values to reflect correct bit definition ..... [20](#)
  - Added user-recommended value for deserializer echo cancellation in general-purpose cables ..... [24](#)
  - Added tolerance for transmission cable impedance ..... [38](#)
  - Added tolerance range for transmission cable skew ..... [38](#)
  - Added reference to optimum settings information in deserializer Reg 0x27 ..... [38](#)
- 

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**Changes from Revision G (April 2013) to Revision H****Page**

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- Changed layout of National Data Sheet to TI format ..... [39](#)
-

## PACKAGING INFORMATION

| Orderable part number              | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|------------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DS92LX1621SQ/NOPB</a>  | Active        | Production           | WQFN (RTV)   32 | 1000   SMALL T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1621              |
| DS92LX1621SQ/NOPB.A                | Active        | Production           | WQFN (RTV)   32 | 1000   SMALL T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1621              |
| <a href="#">DS92LX1621SQE/NOPB</a> | Active        | Production           | WQFN (RTV)   32 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1621              |
| DS92LX1621SQE/NOPB.A               | Active        | Production           | WQFN (RTV)   32 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1621              |
| <a href="#">DS92LX1621SQX/NOPB</a> | Active        | Production           | WQFN (RTV)   32 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1621              |
| DS92LX1621SQX/NOPB.A               | Active        | Production           | WQFN (RTV)   32 | 4500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1621              |
| <a href="#">DS92LX1622SQ/NOPB</a>  | Active        | Production           | WQFN (RTA)   40 | 1000   SMALL T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1622              |
| DS92LX1622SQ/NOPB.A                | Active        | Production           | WQFN (RTA)   40 | 1000   SMALL T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1622              |
| <a href="#">DS92LX1622SQE/NOPB</a> | Active        | Production           | WQFN (RTA)   40 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1622              |
| DS92LX1622SQE/NOPB.A               | Active        | Production           | WQFN (RTA)   40 | 250   SMALL T&R       | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1622              |
| <a href="#">DS92LX1622SQX/NOPB</a> | Active        | Production           | WQFN (RTA)   40 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1622              |
| DS92LX1622SQX/NOPB.A               | Active        | Production           | WQFN (RTA)   40 | 2500   LARGE T&R      | Yes         | SN                                   | Level-3-260C-168 HR               | -40 to 85    | LX1622              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

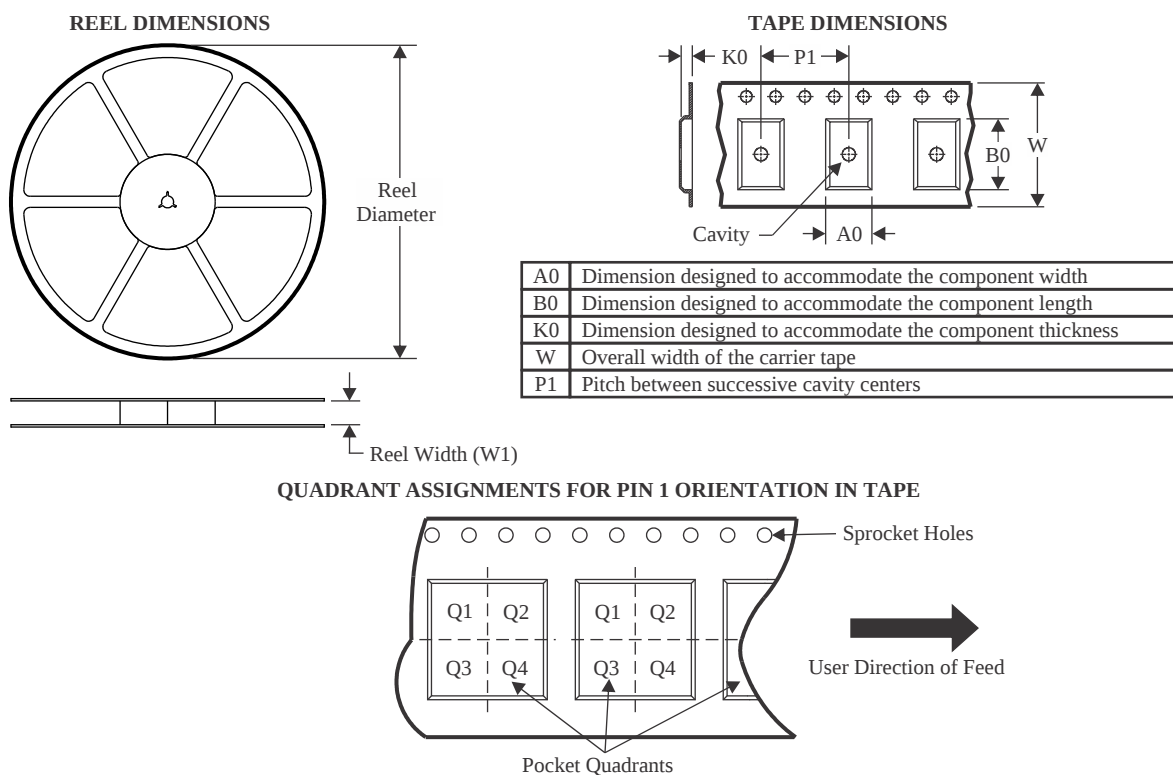
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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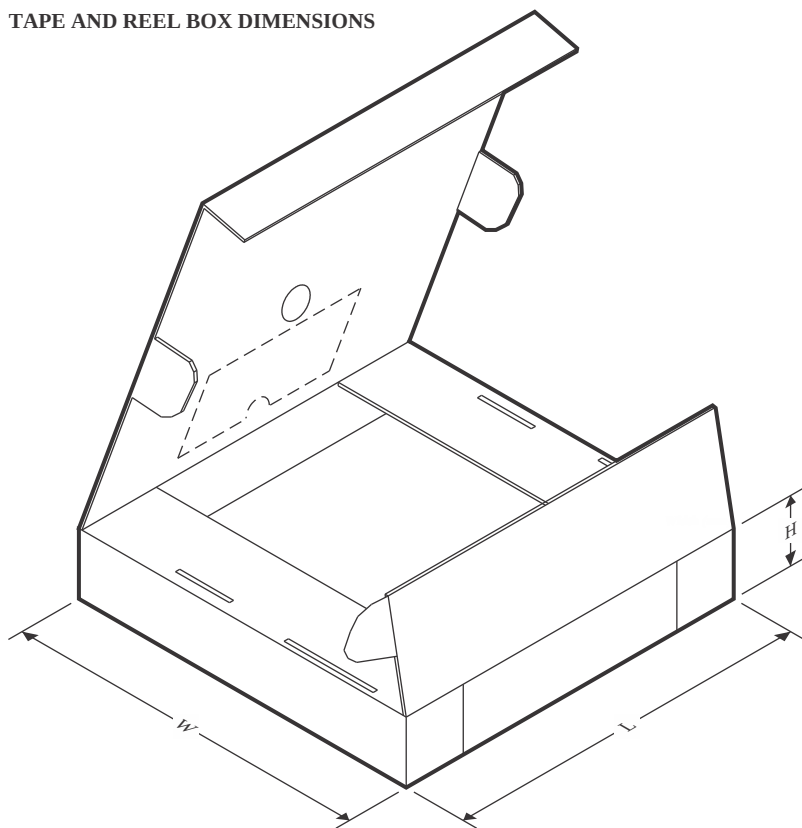
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

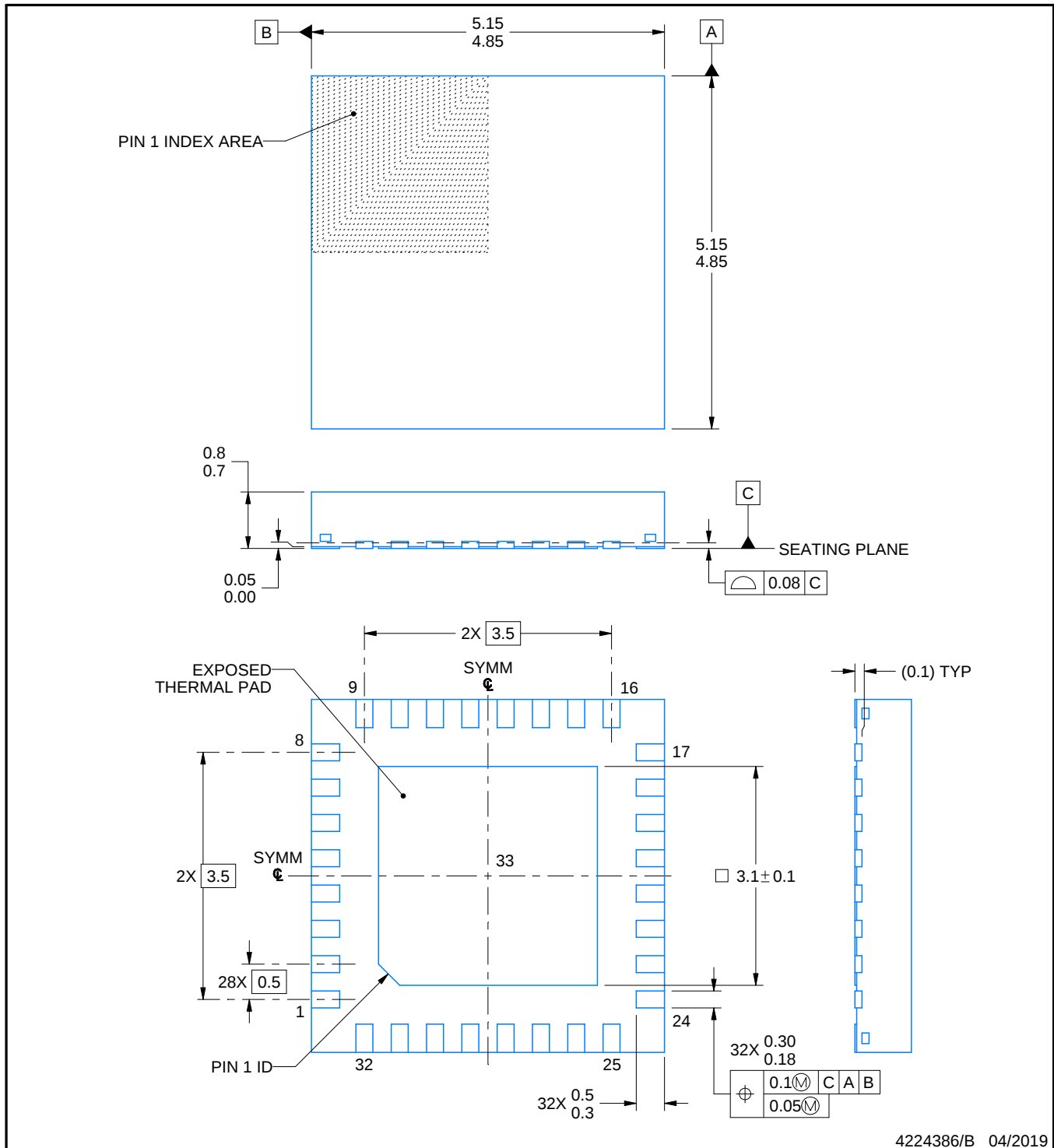
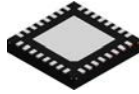
| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS92LX1621SQ/NOPB  | WQFN         | RTV             | 32   | 1000 | 177.8              | 12.4               | 5.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |
| DS92LX1621SQE/NOPB | WQFN         | RTV             | 32   | 250  | 177.8              | 12.4               | 5.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |
| DS92LX1621SQX/NOPB | WQFN         | RTV             | 32   | 4500 | 330.0              | 12.4               | 5.3     | 5.3     | 1.3     | 8.0     | 12.0   | Q1            |
| DS92LX1622SQ/NOPB  | WQFN         | RTA             | 40   | 1000 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |
| DS92LX1622SQE/NOPB | WQFN         | RTA             | 40   | 250  | 178.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |
| DS92LX1622SQX/NOPB | WQFN         | RTA             | 40   | 2500 | 330.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DS92LX1621SQ/NOPB  | WQFN         | RTV             | 32   | 1000 | 208.0       | 191.0      | 35.0        |
| DS92LX1621SQE/NOPB | WQFN         | RTV             | 32   | 250  | 208.0       | 191.0      | 35.0        |
| DS92LX1621SQX/NOPB | WQFN         | RTV             | 32   | 4500 | 356.0       | 356.0      | 36.0        |
| DS92LX1622SQ/NOPB  | WQFN         | RTA             | 40   | 1000 | 356.0       | 356.0      | 36.0        |
| DS92LX1622SQE/NOPB | WQFN         | RTA             | 40   | 250  | 208.0       | 191.0      | 35.0        |
| DS92LX1622SQX/NOPB | WQFN         | RTA             | 40   | 2500 | 356.0       | 356.0      | 36.0        |



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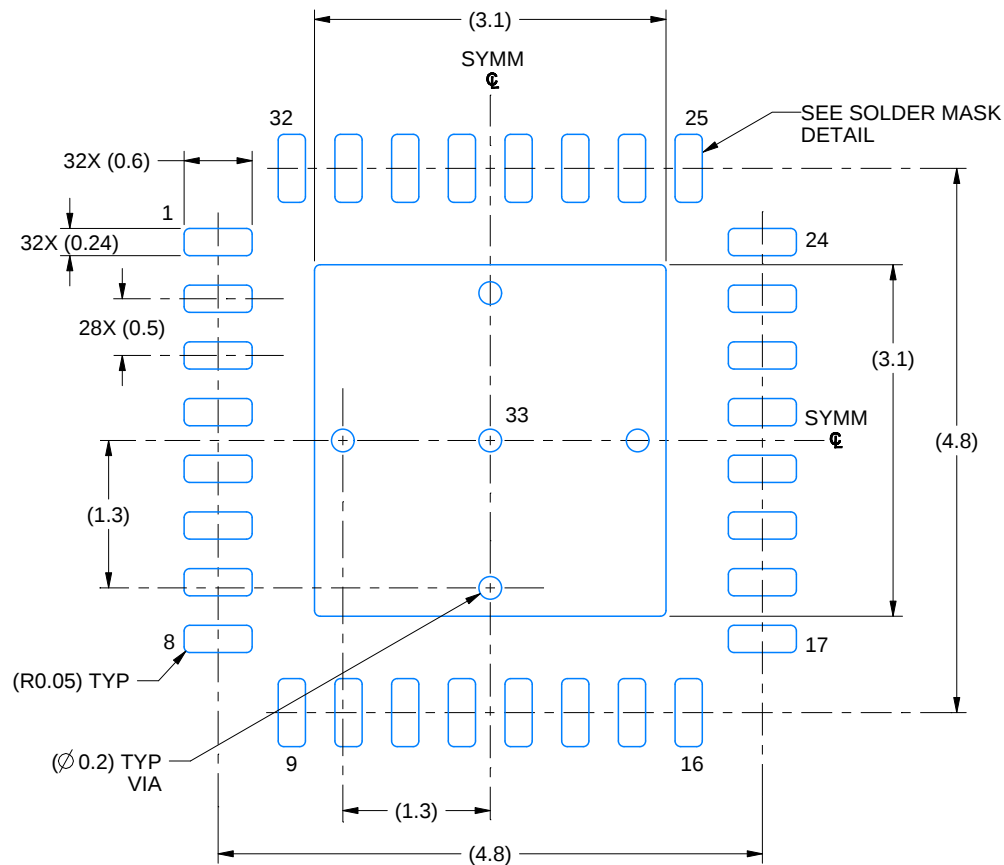
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

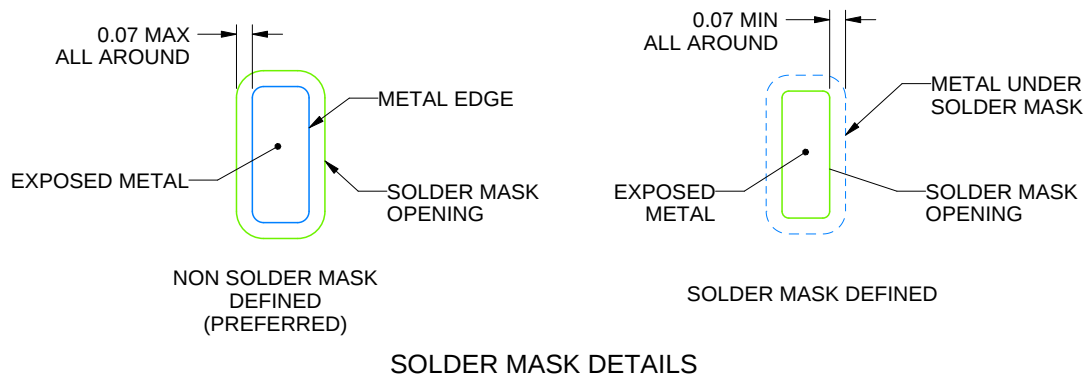
RTV0032A

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



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NOTES: (continued)

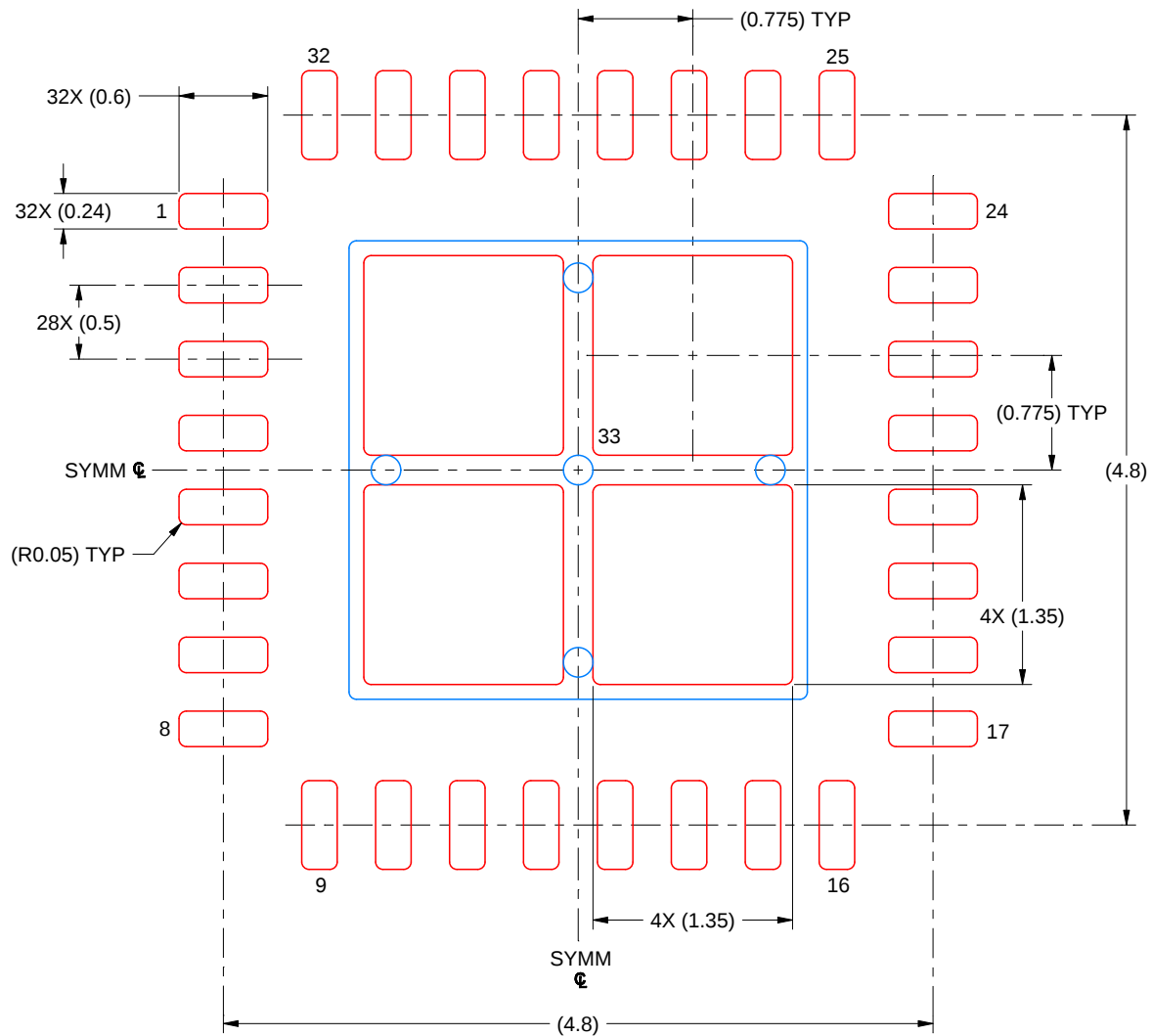
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTV0032A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 33  
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

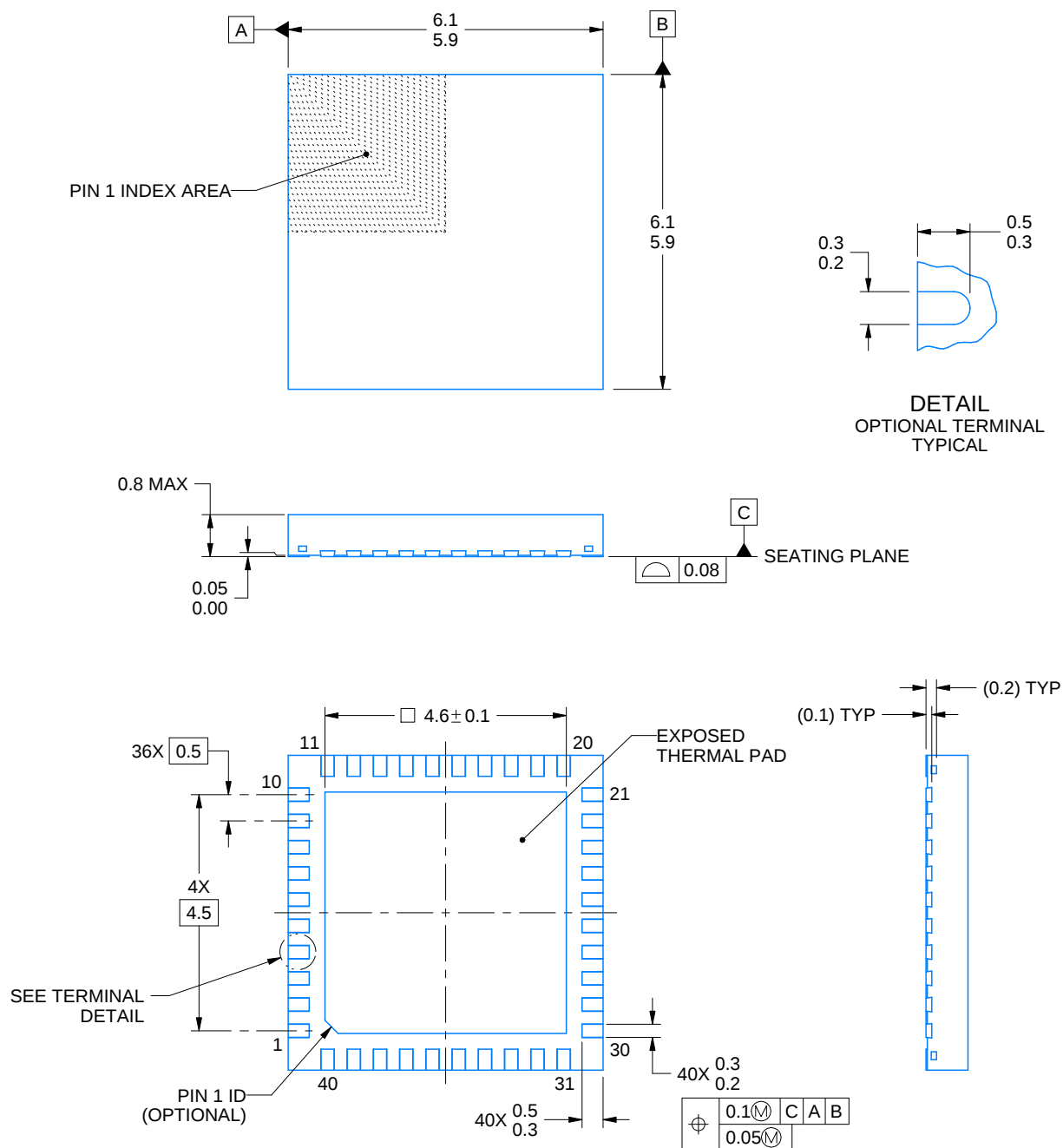
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## PACKAGE OUTLINE

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4214989/B 02/2017

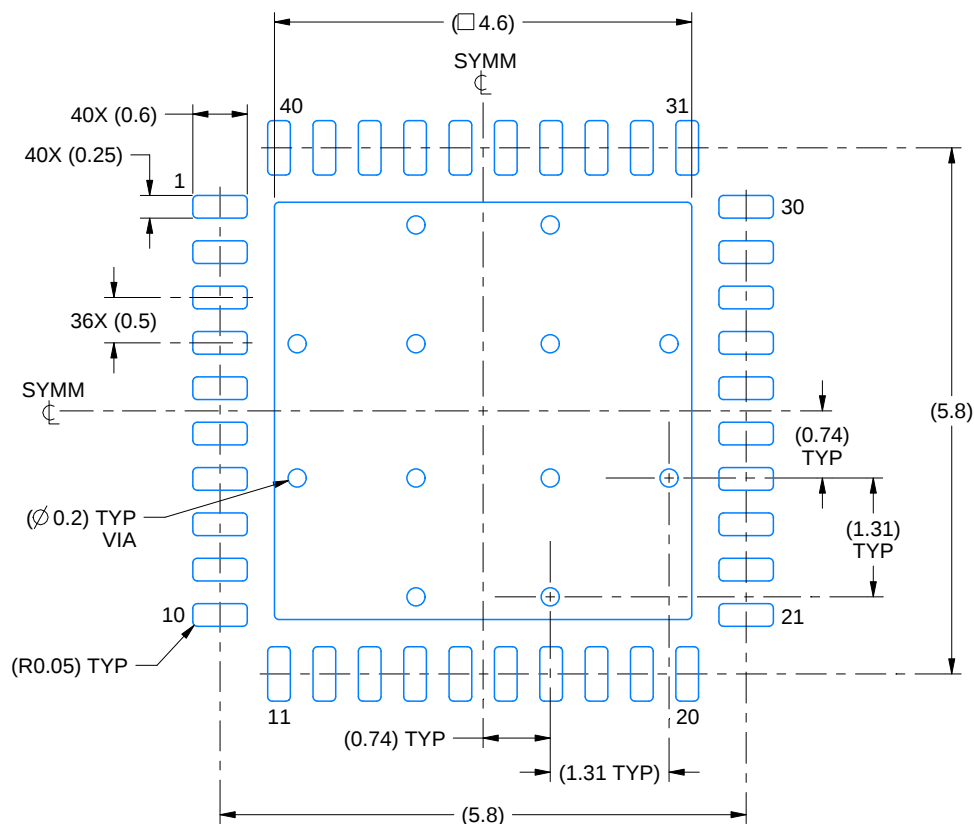
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

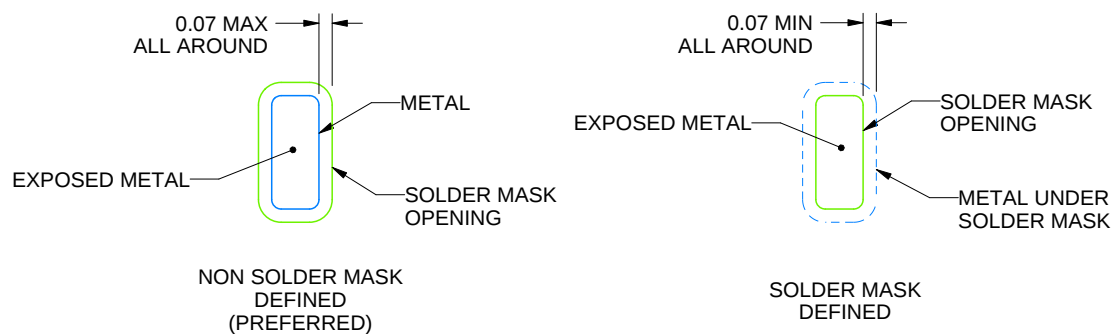
**RTA0040A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:12X



## SOLDER MASK DETAILS

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NOTES: (continued)

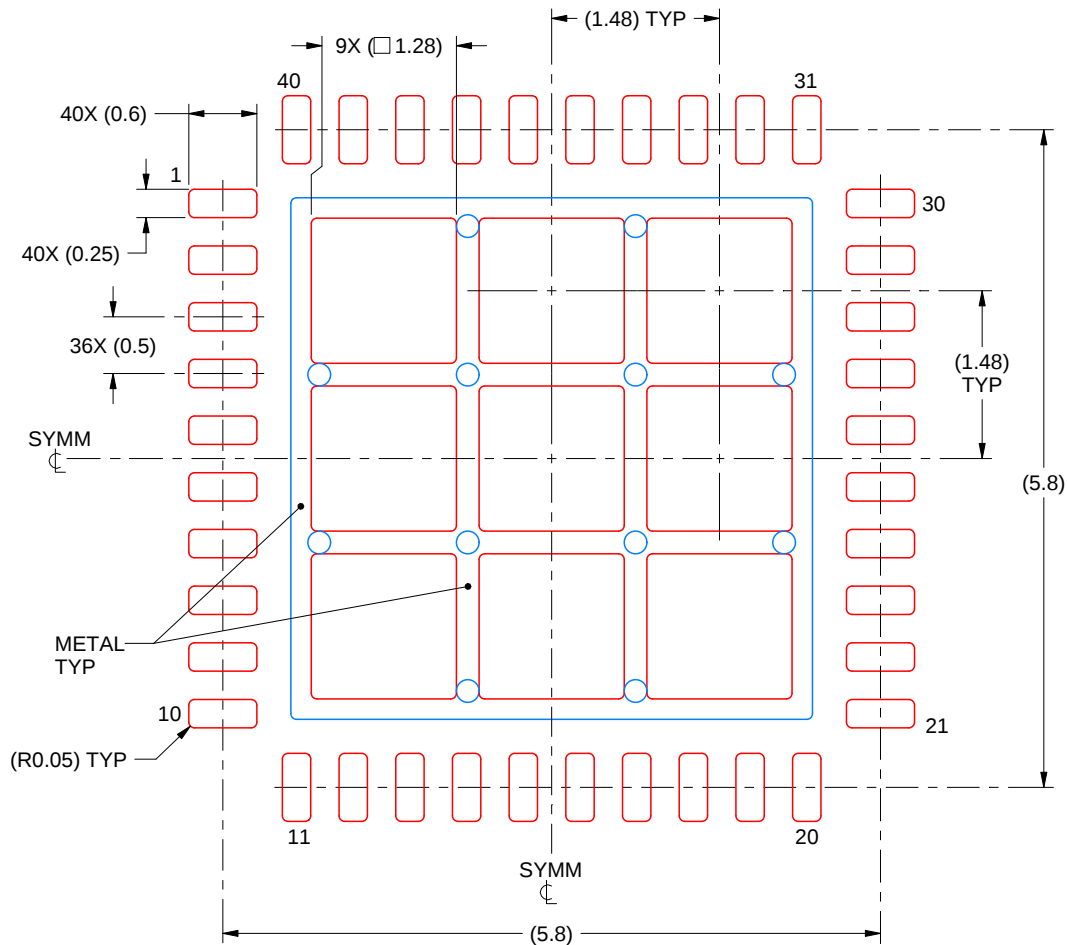
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTA0040A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
70% PRINTED SOLDER COVERAGE BY AREA  
SCALE:15X

4214989/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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