

BIAS POWER SUPPLY FOR TV AND MONITOR TFT LCD PANELS

Check for Samples: [TPS65161](#), [TPS65161A](#), [TPS65161B](#)

FEATURES

- 8-V to 14.7-V Input Voltage Range
- V_S Output Voltage Range up to 19 V
- TPS65161 has a 2.8-A Switch Current Limit
- TPS65161A has a 3.7-A Switch Current Limit
- TPS65161B has a 3.7-A Switch Current Limit and 100-mA Charge Pump Output Current
- 1.5% Accurate 2.3-A Step-Down Converter
- 500-kHz/750-kHz Fixed Switching Frequency
- Negative Charge Pump Driver for V_{GL}
- Positive Charge Pump Driver for V_{GH}
- Adjustable Sequencing for V_{GL} , V_{GH}
- Gate Drive Signal to Drive External MOSFET

- Internal and Adjustable Soft Start
- Short-Circuit Protection
- Overvoltage Protection
- Thermal Shutdown
- Available in HTSSOP-28 Package

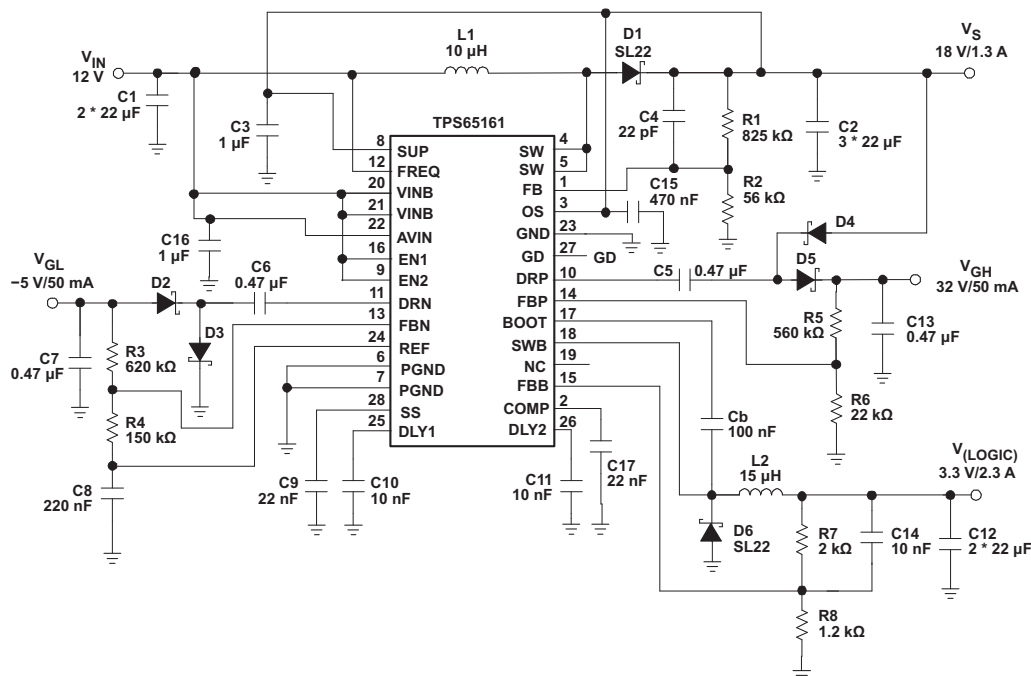
APPLICATIONS

- TFT LCD Displays for Monitor and LCD TV

DESCRIPTION

The TPS65161 family offers a compact power supply solution to provide all four voltages required by thin-film transistor (TFT) LCD panels. With their high current capabilities, the devices are ideal for large screen monitor panels and LCD TV applications.

TYPICAL APPLICATION



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

Compared to the TPS65160 and TPS65160A the TPS65161/A/B family of devices offer increased step-down converter output current. The TPS65161B also offers increased charge pump output current, and a higher undervoltage lockout threshold. The devices can be powered from a 12-V input supply and generate the four main supply voltages required by TFT LCD display panels.

Each device comprises a boost converter to generate the source voltage V_S , a step-down converter to generate the logic supply $V_{(LOGIC)}$, and regulated positive and negative charge pumps to generate the TFT bias voltages V_{GH} and V_{GL} . Both switching converters and both charge pumps operate from a central clock that can be set to either 750-kHz or 500-kHz by tying the FREQ pin high or low.

The TPS65161/A/B devices feature adjustable power supply sequencing, plus a number of safety features such as boost converter overvoltage protection, buck converter short-circuit protection, and thermal shutdown. The devices also incorporate a gate drive signal to control an external MOSFET isolation switch connected in series with V_S or V_{GH} (see the application section at the end of this data sheet for more information).

ORDERING INFORMATION ⁽¹⁾

| T_A | BOOST SWITCH CURRENT LIMIT $I_{LIM(min)}$ | CHARGE PUMP CURRENT LIMIT ⁽²⁾ | UVLO THRESHOLD | ORDERING | PACKAGE ⁽³⁾ | PACKAGE MARKING |
|------------------|-------------------------------------------------|---------------------------------------------|----------------|--------------|------------------------|--------------------|
| –40°C to 85°C | 2.8A | 100mA | 6V | TPS65161PWP | HTSSOP28 (PWP) | TPS65161 |
| | 3.7A | 100mA | 6V | TPS65161APWP | HTSSOP28 (PWP) | TPS65161A |
| | 3.7A | 200mA | 8V | TPS65161BPWP | HTSSOP28 (PWP) | TPS65161B |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
- (2) Because of the charge pumps' 50% duty cycle, the maximum current available from V_{GH} and V_{GL} in typical applications is equal to approximately half the charge pump current limit.
- (3) The PWP package is available taped and reeled. Add R-suffix to the device type (TPS65161PWPR) to order the device taped and reeled. The TPS65161PWPR package has quantities of 2000 devices per reel. Without suffix, the TPS65161PWP is shipped in tubes with 50 devices per tube.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | UNIT |
|-----------------------------------------------|------------------------------|
| Voltages on pin VIN ⁽²⁾ | –0.3 V to 16.5 V |
| Voltages on pin EN1, EN2, FREQ ⁽²⁾ | –0.3 V to 16.5 V |
| Voltage on pin SW ⁽²⁾ | 25 V |
| Voltage on pin SWB ⁽²⁾ | 20 V |
| Voltages on pin OS, SUP, GD ⁽²⁾ | 25 V |
| Continuous power dissipation | See Dissipation Rating Table |
| T_A Operating junction temperature | –40°C to 150°C |
| T_{stg} Storage temperature range | –65°C to 150°C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

| PACKAGE | RTH _{JA} | T _A ≤ 25°C POWER RATING | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------------|-------------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| 28-Pin HTSSOP | 28°C/W (PowerPAD ⁽¹⁾ soldered) | 3.57 W | 1.96 W | 1.42 W |

(1) See Texas Instruments application report [SLMA002](#) regarding thermal characteristics of the PowerPAD package.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------------|----------------------------------------------------------------------|-----|------|-----|------|
| V _S | Output voltage range of the main boost converter ⁽¹⁾ | | | 19 | V |
| C _{IN} | Input capacitor at VINB | | 2x22 | | μF |
| | Input capacitor AVIN | | 1 | | μF |
| L | Inductor boost converter ⁽²⁾ | | 10 | | μH |
| | Inductor buck converter ⁽²⁾ | | 15 | | |
| V _(LOGIC) | Output voltage range of the step-down converter V _(LOGIC) | 1.8 | | 5.0 | V |
| C _O | Output capacitor boost converter | | 3x22 | | μF |
| | Output capacitor buck converter | | 2x22 | | |
| T _A | Operating ambient temperature | –40 | | 85 | °C |
| T _J | Operating junction temperature | –40 | | 125 | °C |

(1) The maximum output voltage is limited by the overvoltage protection threshold and not be the maximum switch voltage rating.

(2) See application section for further information.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12 V, SUP = V_{IN}, EN1 = EN2 = V_{IN}, V_S = 15 V, V_(LOGIC) = 3.3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|-----------------------------------|-------------------------------------------------------------------------|-------|-------|-------|------|
| SUPPLY CURRENT | | | | | | |
| V _{IN} | Input voltage range | | 8 | | 14.7 | V |
| I _Q | Quiescent current into AVIN | V _{GH} = 2 × V _S , Boost converter not switching | | 0.2 | 2 | mA |
| | Quiescent current into VINB | V _{GH} = 2 × V _S , Buck converter not switching | | 0.2 | 0.5 | |
| I _{SD} | Shutdown current into AVIN | EN1 = EN2 = GND | | 0.1 | 2 | μA |
| | Shutdown current into VINB | EN1 = EN2 = GND | | 0.1 | 2 | |
| I _(SUP) | Shutdown current into SUP | EN1 = EN2 = GND | | 0.1 | 4 | μA |
| | Quiescent current into SUP | V _{GH} = 2 × V _S | | 0.2 | 2 | mA |
| V _{UVLO} | Undervoltage lockout threshold | TPS65161, TPS65161A; V _{IN} falling. | | 6 | 6.4 | V |
| | | TPS65161B; V _{IN} falling. | | 8 | 8.8 | |
| V _{ref} | Reference voltage | | 1.203 | 1.213 | 1.223 | V |
| | Thermal shutdown | Temperature rising | | 155 | | °C |
| | Thermal shutdown hysteresis | | | 5 | | °C |
| LOGIC SIGNALS EN1, EN2, FREQ | | | | | | |
| V _{IH} | High-level input voltage EN1, EN2 | | 2.0 | | | V |
| V _{IL} | Low-level input voltage EN1, EN2 | | | | 0.8 | V |
| V _{IH} | High-level input voltage FREQ | | 1.7 | | | V |
| V _{IL} | Low-level input voltage FREQ | | | | 0.4 | V |
| I _{lkg} | Input leakage current | EN1 = EN2 = FREQ = GND or V _{IN} | | 0.01 | 0.1 | μA |

ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{ V}$, $SUP = V_{IN}$, $EN1 = EN2 = V_{IN}$, $V_S = 15\text{ V}$, $V_{(LOGIC)} = 3.3\text{ V}$, $T_A = -40^{\circ}\text{C}$ to 85°C , typical values are at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------------|--------------------------------------|----------------------------------------------|---------------------|--------------------|--------------------|------|
| CONTROL AND SOFT START DLY1, DLY2, SS | | | | | | |
| I _(DLY1) | Delay1 charge current | V _(THRESHOLD) = 1.213 V | 3.3 | 4.8 | 6.2 | μA |
| I _(DLY2) | Delay2 charge current | | 3.3 | 4.8 | 6.2 | μA |
| I _{SS} | SS charge current | | 6 | 9 | 12 | μA |
| INTERNAL OSCILLATOR | | | | | | |
| f _{OSC} | Oscillator frequency | FREQ = high | 600 | 750 | 900 | kHz |
| | | FREQ = low | 400 | 500 | 600 | |
| BOOST CONVERTER (V _S) | | | | | | |
| V _S | Output voltage range ⁽¹⁾ | | | | 19 | V |
| V _(FB) | Feedback regulation voltage | | 1.136 | 1.146 | 1.156 | V |
| I _(FB) | Feedback input bias current | | | 10 | 100 | nA |
| r _{DS(on)} | N-MOSFET on-resistance (Q1) | I _(SW) = 500 mA | | 100 | 185 | mΩ |
| | P-MOSFET on-resistance (Q2) | I _(SW) = 200 mA | | 10 | 16 | Ω |
| I _{MAX} | Maximum P-MOSFET peak switch current | | | | 1 | A |
| I _{LIM} | N-MOSFET switch current limit (Q1) | TPS65161 | 2.8 | 3.5 | 4.2 | A |
| I _{LIM} | N-MOSFET switch current limit (Q1) | TPS65161A | 3.7 | 4.6 | 5.5 | A |
| I _{lkg} | Switch leakage current | V _(SW) = 15 V | | 1 | 10 | μA |
| OVP | Overvoltage protection | V _{OUT} rising | 19.5 | 20 | 21 | V |
| | Line regulation | 10.6 V ≤ V _{IN} ≤ 11.6 V at 1 mA | | 0.0008 | | %/V |
| | Load regulation | | | 0.03 | | %/A |
| GATE DRIVE (GD) | | | | | | |
| V _(GD) | Gate drive threshold ⁽²⁾ | V _(FB) rising | V _S -12% | V _S -8% | V _S -4% | V |
| V _{OL} | GD output low voltage | I _(sink) = 500 μA | | | 0.3 | V |
| | GD output leakage current | V _(GD) = 20 V | | 0.05 | 1 | μA |
| STEP-DOWN CONVERTER (V _(LOGIC)) | | | | | | |
| V _(LOGIC) | Output voltage range | | 1.8 | | 5 | V |
| V _(FBB) | Feedback regulation voltage | | 1.195 | 1.213 | 1.231 | V |
| I _(FBB) | Feedback input bias current | | | 10 | 100 | nA |
| r _{DS(on)} | N-MOSFET on-resistance (Q5) | I _(SW) = 500 mA | | 175 | 300 | mΩ |
| I _{LIM} | N-MOSFET switch current limit (Q5) | | 2.5 | 3.2 | 3.9 | A |
| I _{lkg} | Switch leakage current | V _(SW) = 0 V | | 1 | 10 | μA |
| | Line regulation | 10.6 V ≤ V _{IN} ≤ 11.6 V at 1 mA | | 0.0018 | | %/V |
| | Load regulation | | | 0.037 | | %/A |

- (1) The maximum output voltage is limited by the overvoltage protection threshold and not be the maximum switch voltage rating.
 (2) The GD signal is latched low when the main boost converter output V_S is within regulation. The GD signal is reset when the input voltage or enable of the boost converter is cycled low.

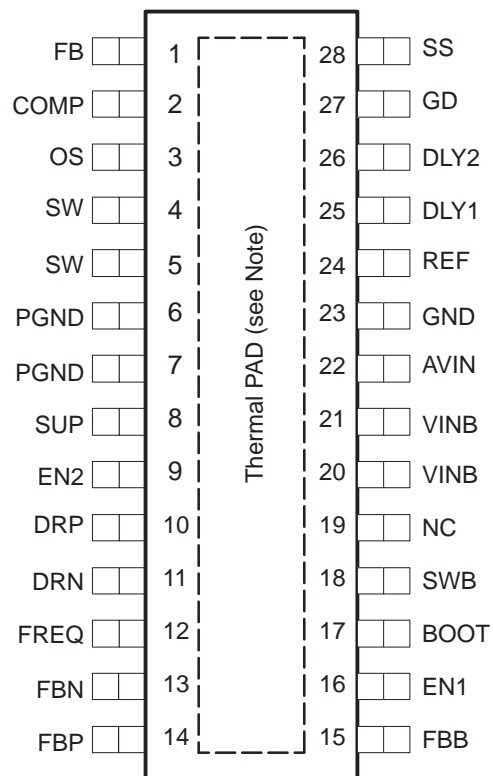
ELECTRICAL CHARACTERISTICS (continued)

$V_{IN} = 12\text{ V}$, $SUP = V_{IN}$, $EN1 = EN2 = V_{IN}$, $V_S = 15\text{ V}$, $V_{(LOGIC)} = 3.3\text{ V}$, $T_A = -40^{\circ}\text{C}$ to 85°C , typical values are at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------------------|---------------------------------------------------------------------------------------|-----------------------------------------------|----------------------------------------------------------------------------------|-------|-------|-------|------|
| NEGATIVE CHARGE-PUMP VGL | | | | | | | |
| V _O | Output voltage range | | | | | −2 | V |
| V _(FBN) | Feedback regulation voltage | | | −36 | 0 | 36 | mV |
| I _(FBN) | Feedback input bias current | | | | 10 | 100 | nA |
| r _{DS(on)} | Q4 P-Channel switch r _{DS(on)} | TPS65161, TPS65161A; I _{OUT} = 20 mA | | | 4.4 | | Ω |
| | | TPS65161B; I _{OUT} = 20 mA | | | 3.7 | | |
| V _(DropN) | Current sink voltage drop ⁽³⁾ | TPS65161, TPS65161A | I _(DRN) = 50 mA, V _(FBN) = V _(FBN) nominal −5% | | 0.13 | 0.19 | V |
| | | | I _(DRN) = 100 mA, V _(FBN) = V _(FBN) nominal −5% | | 0.27 | 0.42 | |
| | | TPS65161B | I _(DRN) = 100 mA, V _(FBN) = V _(FBN) nominal −5% | | 0.24 | 0.42 | |
| | | | I _(DRN) = 200 mA, V _(FBN) = V _(FBN) nominal −5% | | 0.52 | 0.90 | |
| POSITIVE CHARGE-PUMP OUTPUT VGH | | | | | | | |
| V _(FBP) | Feedback regulation voltage | | | 1.187 | 1.213 | 1.238 | V |
| I _(FBP) | Feedback input bias current | | | | 10 | 100 | nA |
| r _{DS(on)} | Q3 N-Channel switch r _{DS(on)} | I _{OUT} = 20 mA | | | 1.1 | | Ω |
| V _(DropP) | Current source voltage drop (V _(SUP) − V _(DRP)) ⁽⁴⁾ | TPS65161, TPS65161A | I _(DRP) = 50 mA, V _(FBP) = V _(FBP) nominal −5% | | 0.40 | 0.68 | V |
| | | | I _(DRP) = 100 mA, V _(FBP) = V _(FBP) nominal −5% | | 0.85 | 1.60 | |
| | | TPS65161B | I _(DRP) = 100 mA, V _(FBP) = V _(FBP) nominal −5% | | 0.63 | 1.60 | |
| | | | I _(DRP) = 200 mA, V _(FBP) = V _(FBP) nominal −5% | | 1.40 | 3.20 | |

(3) The maximum charge-pump output current is typically half the drive current of the internal current source or current sink.

(4) The maximum charge-pump output current is typically half the drive current of the internal current source or current sink.



NOTE: The thermally enhanced PowerPAD™ is connected to PGND.

PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|-----------|--------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME | NO. | | |
| SUP | 8 | I | This is the supply pin of the positive charge pump driver and can be connected to the input supply V_{IN} or the output of the main boost converter V_S . This depends mainly on the desired output voltage V_{GH} and numbers of charge pump stages. |
| FREQ | 12 | I | Frequency adjust pin. This pin allows setting the switching frequency with a logic level to 500 kHz = low and 750 kHz = high. |
| AVIN | 22 | I | Analog input voltage of the device. This is the input for the analog circuits of the device and should be bypassed with a 1- μ F ceramic capacitor for good filtering. |
| VINB | 20, 21 | I | Power input voltage pin for the buck converter. |
| EN1 | 16 | I | This is the enable pin of the buck converter and negative charge pump. When this pin is pulled high, the buck converter starts up, and after a delay time set by DLY1, the negative charge pump comes up. This pin must be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device. |
| EN2 | 9 | I | The boost converter starts only with EN1 = high, after the step-down converter is enabled. EN2 is the enable pin of the boost converter and positive charge pump. When this pin is pulled high, the boost converter and positive charge pump starts up after the buck converter is within regulation and a delay time set by DLY2 has passed by. This pin must be terminated and not be left floating. A logic high enables the device and a logic low shuts down the device. |
| DRN | 11 | O | Drive pin of the negative charge pump. |
| FBN | 13 | I | Feedback pin of negative charge pump. |
| REF | 24 | O | Internal reference output typically 1.213 V. A 220-nF capacitor needs to be connected to this pin. |
| PGND | 6, 7 | | Power ground |
| SS | 28 | O | This pin allows setting the soft-start time for the main boost converter V_S . Typically a 22-nF capacitor needs to be connected to this pin to set the soft-start time. |
| DLY1 | 25 | O | Connecting a capacitor from this pin to GND allows the setting of the delay time between $V_{(LOGIC)}$ (step-down converter output high) to V_{GL} during start-up. |
| DLY2 | 26 | O | Connecting a capacitor from this pin to GND allows the setting of the delay time between $V_{(LOGIC)}$ (step-down converter output high) to V_S boost converter and positive charge-pump V_{GH} during start-up. |
| COMP | 2 | | This is the compensation pin for the main boost converter. A small capacitor and, if required, a resistor is connected to this pin. |
| FBB | 15 | I | Feedback pin of the buck converter |
| SWB | 18 | O | Switch pin of the buck converter |
| NC | 19 | | Not connected |
| BOOT | 17 | I | N-channel MOSFET gate drive voltage for the buck converter. Connect a capacitor from the switch node SWB to this pin. |
| FBP | 14 | I | Feedback pin of positive charge pump. |
| DRP | 10 | O | Drive pin of the positive charge pump. |
| GD | 27 | | This is the gate drive pin which can be used to control an external MOSFET switch to provide input to output isolation of V_S or V_{GH} . See the circuit diagrams at the end of this data sheet. GD is an open-drain output and is latched low as soon as the boost converter is within 8% of its nominal regulated output voltage. GD goes high impedance when the EN2 input voltage is cycled low. |
| GND | 23 | | Analog ground |
| OS | 3 | I | Output sense pin. The OS pin is connected to the internal rectifier switch and overvoltage protection comparator. This pin needs to be connected to the output of the boost converter and cannot be connected to any other voltage rail. Connect a 470-nF capacitor from OS pin to GND to avoid noise coupling into this pin. The PCB trace of the OS pin needs to be wide because it conducts high current. |
| FB | 1 | I | Feedback of the main boost converter generating V_{source} (V_S). |
| SW | 4, 5 | I | Switch pin of the boost converter generating V_{source} (V_S). |
| PowerPAD™ | | | The PowerPAD needs to be connected and soldered to power ground (PGND). |

TABLE OF GRAPHS

| | | | FIGURE |
|-------------------------------------------------------|---------------------------------------|-----------------------------------------------------------------------|--------|
| MAIN BOOST CONVERTER (V_S) | | | |
| η | Efficiency main boost converter V_S | vs Load current $V_S = 15\text{ V}$, $V_{IN} = 12\text{ V}$ | 1 |
| $r_{DS(ON)}$ | N-channel main switch Q1 | vs Input voltage and temperature | 2 |
| | Soft-start boost converter | $C_{SS} = 22\text{ nF}$ | 3 |
| | PWM operation at full-load current | | 4 |
| | PWM operation at light-load current | | 5 |
| | Load transient response | | 6 |
| STEP-DOWN CONVERTER ($V_{(LOGIC)}$) | | | |
| η | Efficiency main boost converter V_S | vs Load current $V_{(LOGIC)} = 3.3\text{ V}$, $V_{IN} = 12\text{ V}$ | 7 |
| $r_{DS(ON)}$ | N-channel main switch Q5 | | 8 |
| | PWM operation - continuous mode | | 9 |
| | PWM operation - discontinuous mode | | 10 |
| | Soft start | | 11 |
| | Load transient response | | 12 |
| SYSTEM PERFORMANCE | | | |
| f_{osc} | Oscillation frequency | vs Input voltage and temperature | 13 |
| | Power-up sequencing | EN2 connected to V_{IN} | 14 |
| | Power-up sequencing | EN2 enabled separately | 15 |

TYPICAL CHARACTERISTICS

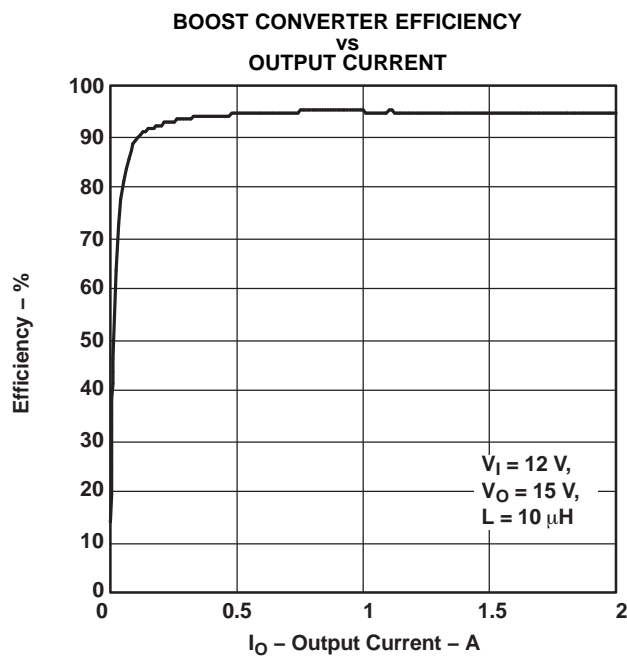


Figure 1.

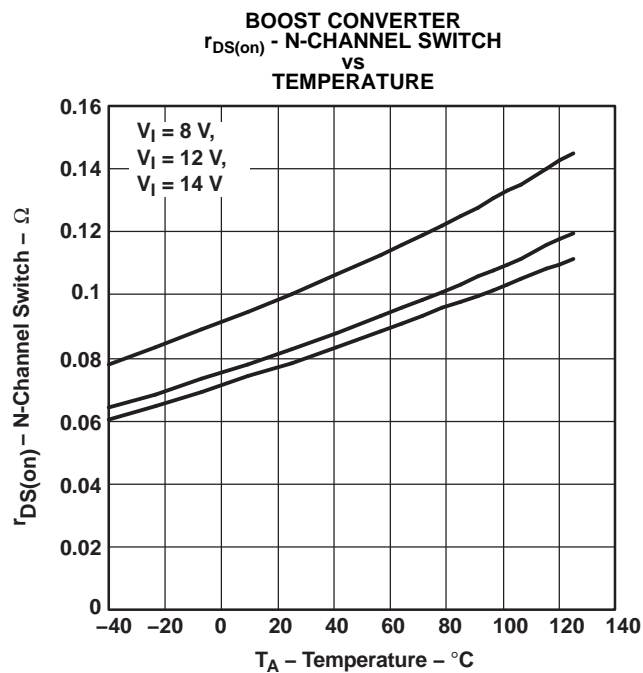
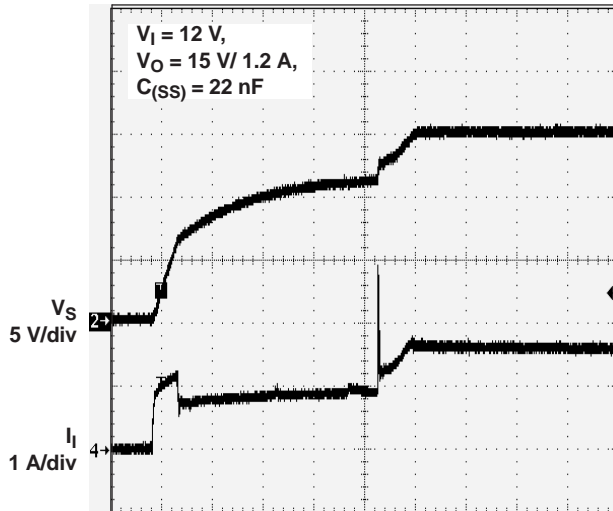


Figure 2.

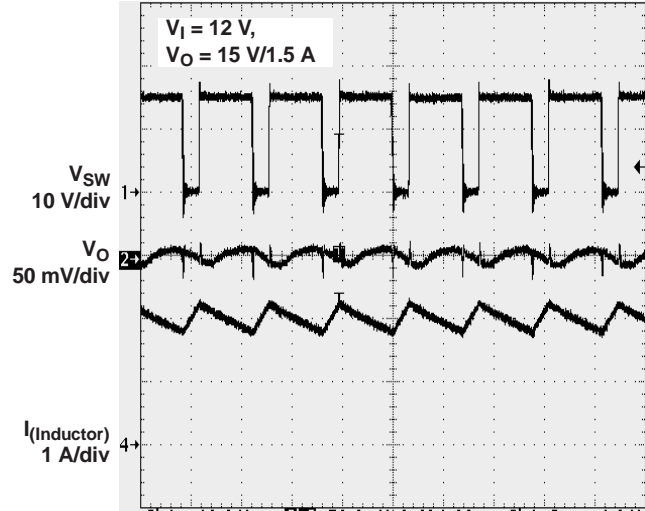
TYPICAL CHARACTERISTICS (continued)

SOFT-START BOOST CONVERTER



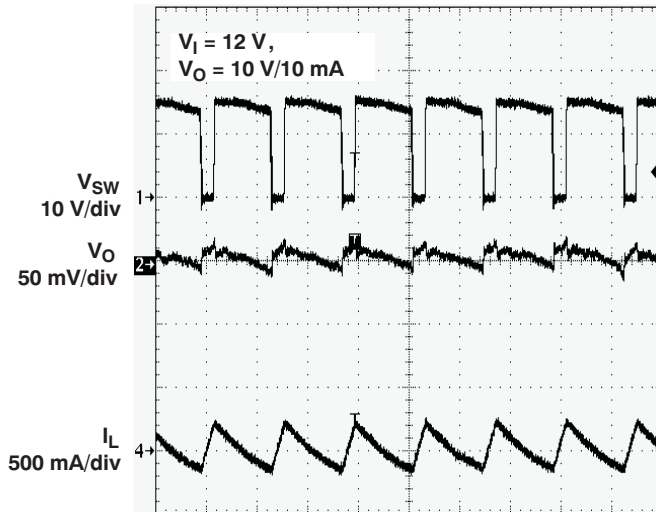
2 ms/div
Figure 3.

PWM OPERATION BOOST CONVERTER CONTINUOUS MODE



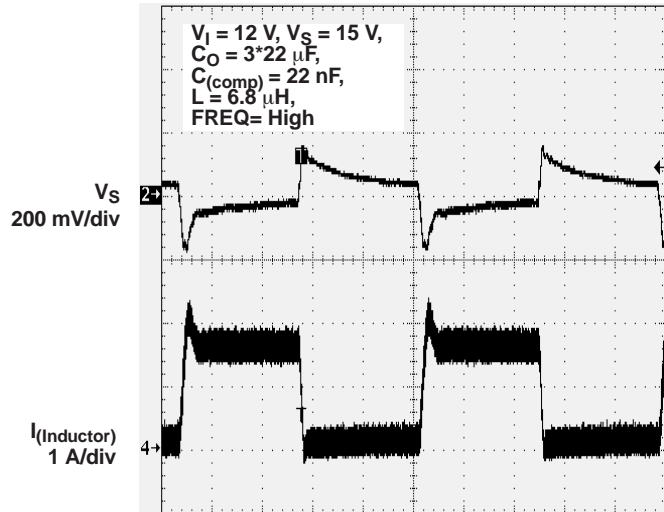
1 $\mu\text{s}/\text{div}$
Figure 4.

PWM OPERATION BOOST CONVERTER CONTINUOUS MODE: LIGHT LOAD



1 $\mu\text{s}/\text{div}$
Figure 5.

LOAD TRANSIENT RESPONSE BOOST CONVERTER



100 $\mu\text{s}/\text{div}$
Figure 6.

TYPICAL CHARACTERISTICS (continued)

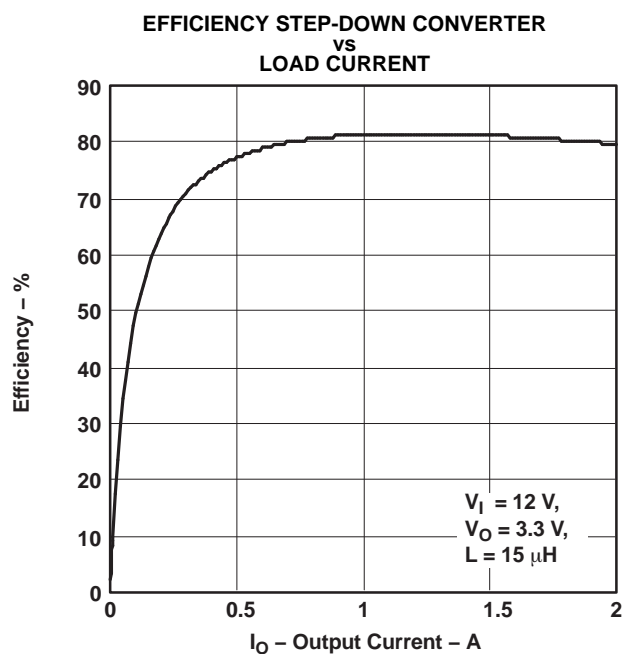


Figure 7.

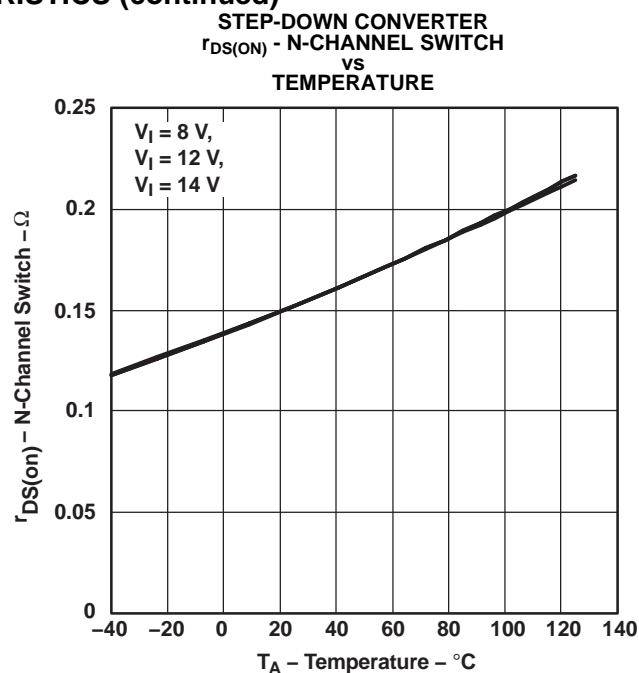
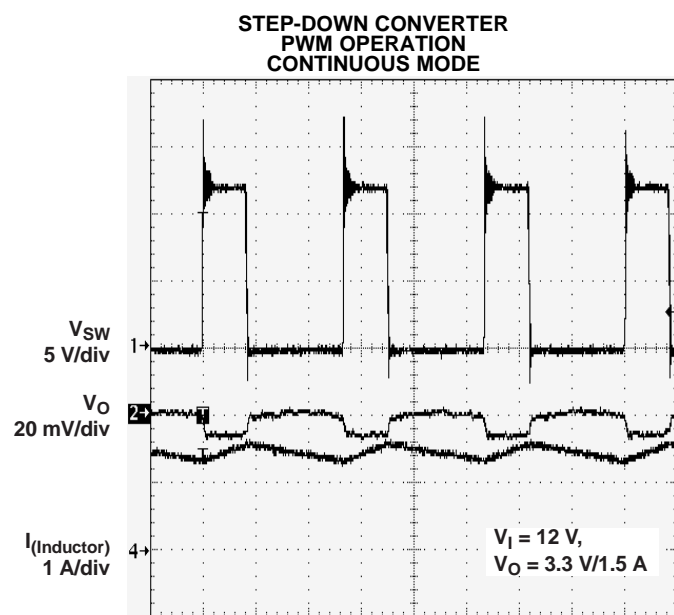
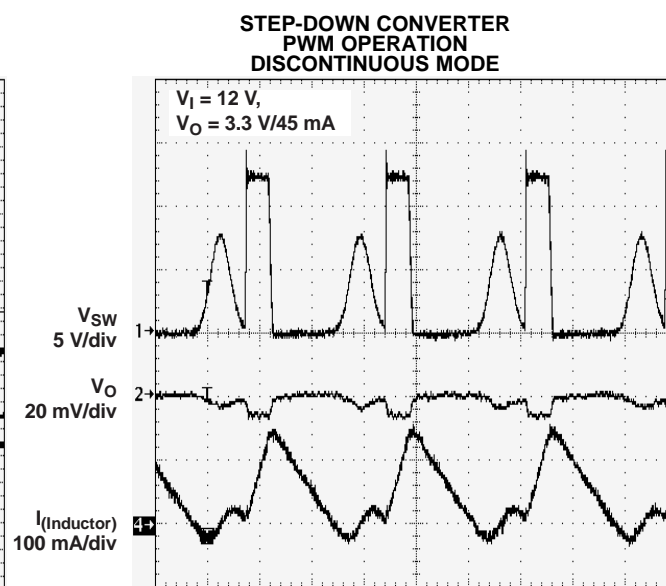


Figure 8.



500 ns/div
Figure 9.



500 ns/div
Figure 10.

TYPICAL CHARACTERISTICS (continued)

SOFT-START STEP-DOWN CONVERTER

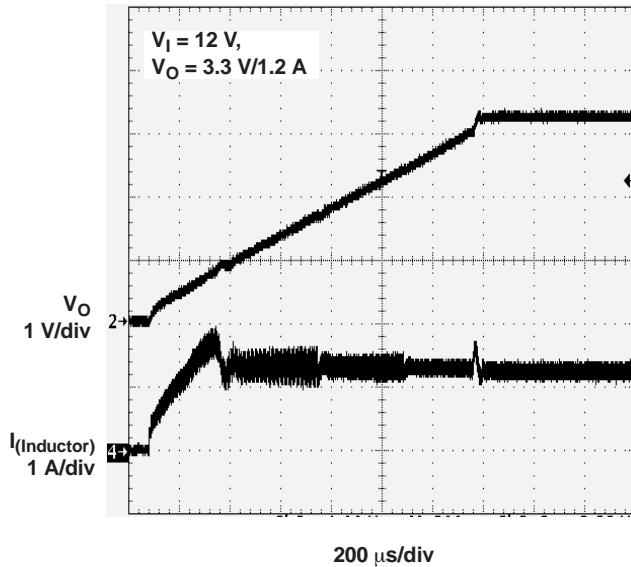


Figure 11.

LOAD TRANSIENT RESPONSE STEP-DOWN CONVERTER

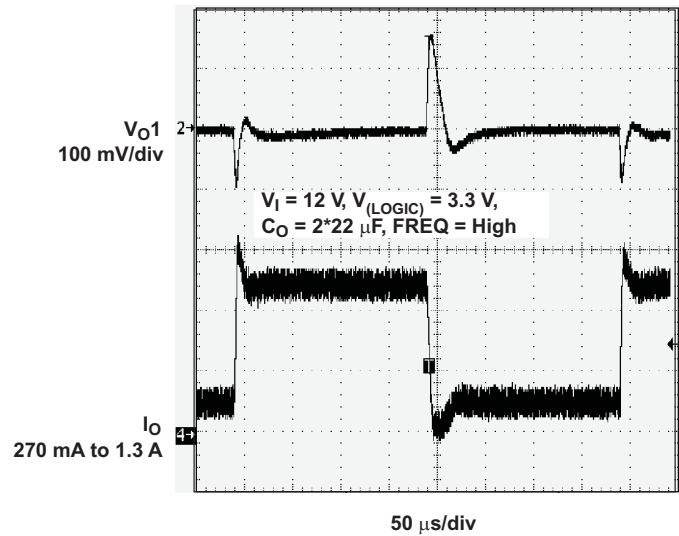


Figure 12.

SWITCHING FREQUENCY VS TEMPERATURE

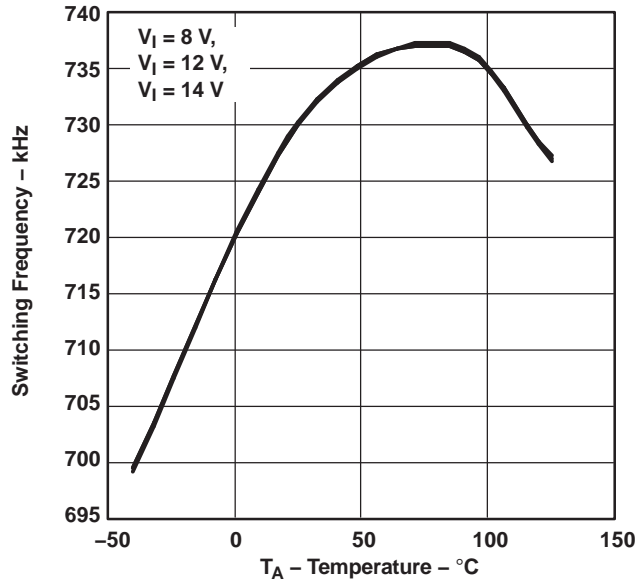


Figure 13.

POWER-UP SEQUENCING EN2 CONNECTED TO V_{IN}

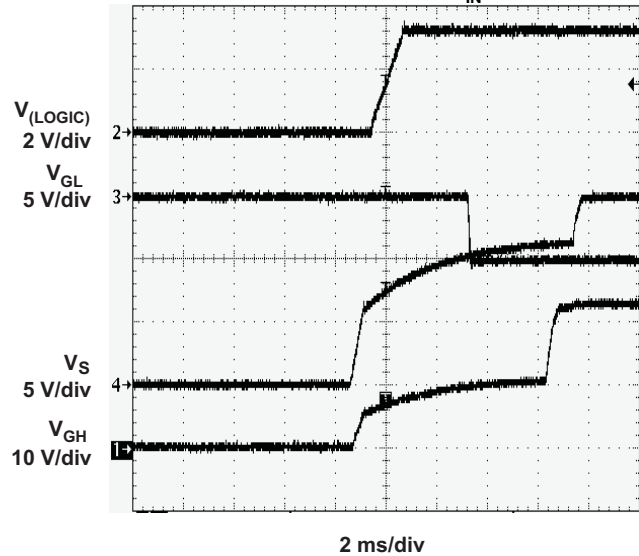
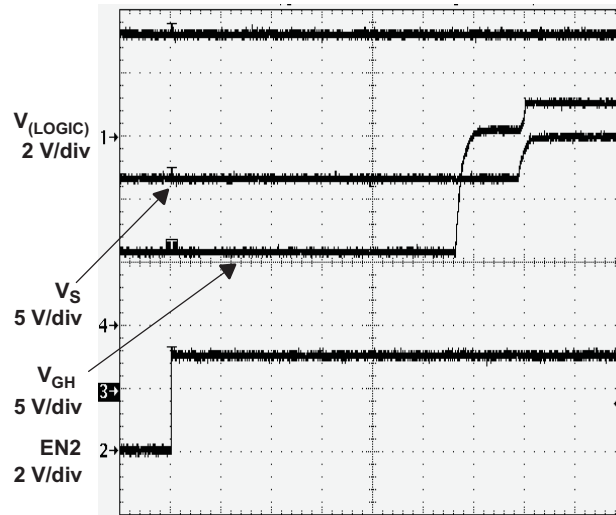


Figure 14.

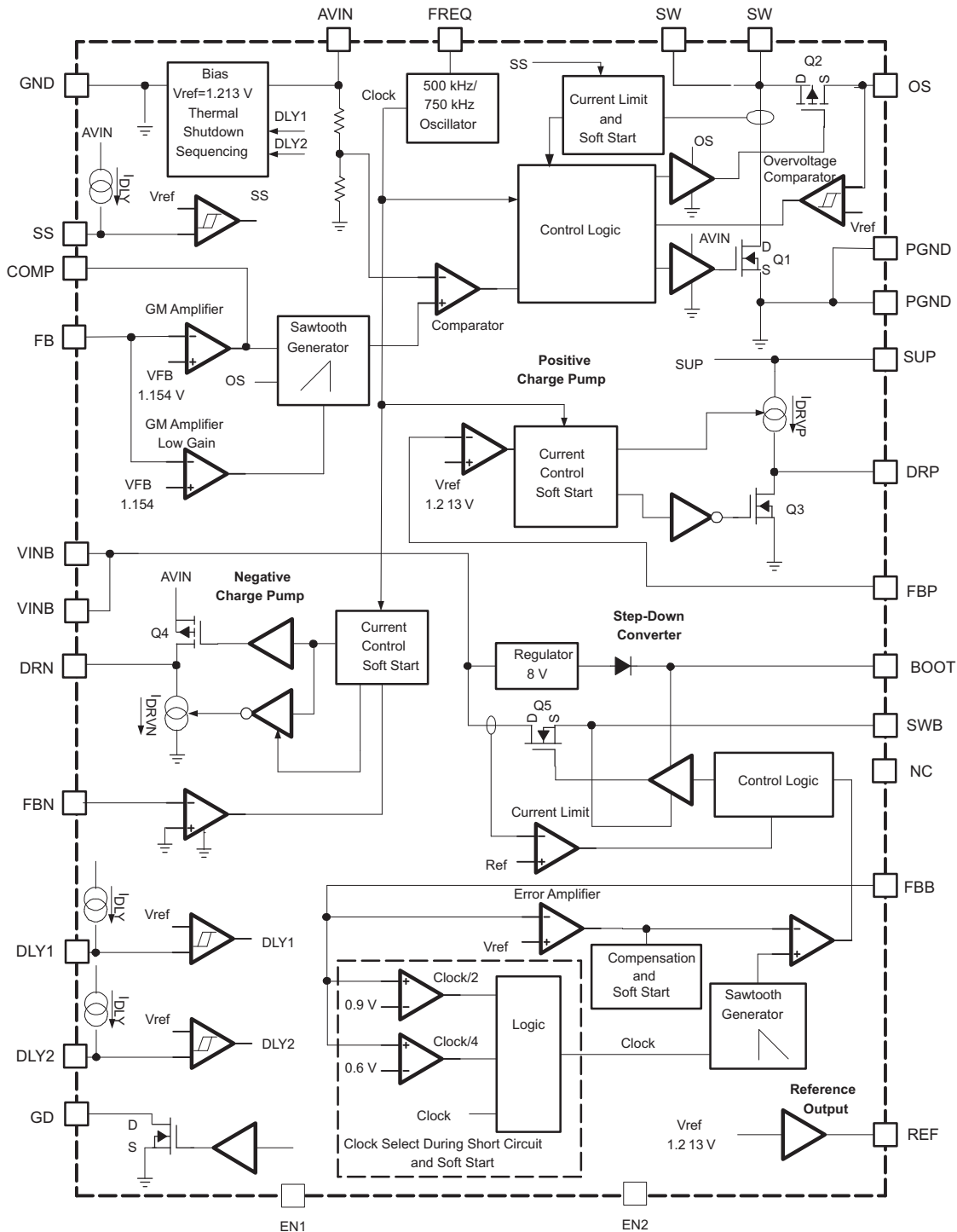
TYPICAL CHARACTERISTICS (continued)
POWER-UP SEQUENCING
EN2 ENABLED SEPARATELY



1 ms/div
Figure 15.

TYPICAL CHARACTERISTICS (continued)

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Boost Converter

The main boost converter operates in pulse-width modulation (PWM) and at a fixed switching frequency of 500 kHz or 750 kHz set by the FREQ pin. The converter uses an unique fast response, voltage-mode controller scheme with input voltage feedforward. This achieves excellent line and load regulation (0.03%-A load regulation typical) and allows the use of small external components. To add higher flexibility to the selection of external component values, the device uses external loop compensation. Although the boost converter looks like a nonsynchronous boost converter topology operating in discontinuous conduction mode at light load, the TPS65161 maintains continuous conduction even at light-load currents. This is achieved with a novel architecture using an external Schottky diode with an integrated MOSFET in parallel connected between SW and OS. See the Functional Block Diagram. The intention of this MOSFET is to allow the current to go negative that occurs at light-load conditions. For this purpose, a small integrated P-Channel MOSFET with typically $10\text{-}\Omega$ $r_{DS(on)}$ is sufficient. When the inductor current is positive, the external Schottky diode with the lower forward voltage conducts the current. This causes the converter to operate with a fixed frequency in continuous conduction mode over the entire load current range. This avoids the ringing on the switch pin as seen with standard nonsynchronous boost converter and allows a simpler compensation for the boost converter.

Soft Start (Boost Converter)

The main boost converter has an adjustable soft start to prevent high inrush current during start-up. The soft-start time is set by the external capacitor connected to the SS pin. The capacitor connected to the SS pin is charged with a constant current that increases the voltage on the SS pin. The internal current limit is proportional to the voltage on the soft-start pin. When the threshold voltage of the internal soft-start comparator is reached, the full current limit is released. The larger the soft-start capacitor value, the longer the soft-start time.

Overvoltage Protection of the Boost Converter

The main boost converter has an overvoltage protection to protect the main switch Q2 at pin (SW) in case the feedback (FB) pin is floating or shorted to GND. In such an event, the output voltage rises and is monitored with the overvoltage protection comparator over the OS pin. See the functional block diagram. As soon as the comparator trips at typically 20 V, TPS65161, the boost converter turns the N-Channel MOSFET switch off. The output voltage falls below the overvoltage threshold and the converter continues to operate.

Frequency Select Pin (FREQ)

The frequency select pin (FREQ) allows setting the switching frequency of the entire device to 500 kHz (FREQ = low) or 750 kHz (FREQ = high). A lower switching frequency gives a higher efficiency with a slightly reduced load transient regulation.

Thermal Shutdown

A thermal shutdown is implemented to prevent damage caused by excessive heat and power dissipation. Typically, the thermal shutdown threshold is 155°C.

Step-Down Converter

The nonsynchronous step-down converter operates at a fixed switching frequency using a fast response voltage mode topology with input voltage feedforward. This topology allows simple internal compensation, and it is designed to operate with ceramic output capacitors. The converter drives an internal 3.2-A N-channel MOSFET switch. The MOSFET driver is referenced to the switch pin SWB. The N-channel MOSFET requires a gate drive voltage higher than the switch pin to turn the N-Channel MOSFET on. This is accomplished by a bootstrap gate drive circuit running of the step-down converter switch pin. When the switch pin SWB is at ground, the bootstrap capacitor is charged to 8 V. This way, the N-channel gate drive voltage is typically around 8 V.

Soft Start (Step-Down Converter)

To avoid high inrush current during start-up, an internal soft start is implemented in the TPS65161. When the step-down converter is enabled over EN1, its reference voltage slowly rises from zero to its power-good threshold of typically 90% of V_{ref} . When the reference voltage reaches this power-good threshold, the error amplifier is released to its normal operation at its normal duty cycle. To further limit the inrush current during soft start, the converter frequency is set to $1/4^{th}$ of the switching frequency f_s and then $1/2$ of f_s determined by the comparator that monitors the feedback voltage. See the internal block diagram. Soft start is typically completed within 1 ms.

Short-Circuit Protection (Step-Down Converter)

To limit the short-circuit current, the device has a cycle-by-cycle current limit. To avoid the short-circuit current rising above the internal current limit when the output is shorted to GND, the switching frequency is reduced as well. This is implemented by two comparators monitoring the feedback voltage. The step-down converter switching frequency is reduced to $1/2$ of f_s when the feedback is below 0.9 V and to $1/4^{th}$ of the switching frequency when the feedback voltage is below 0.6 V.

Positive Charge Pump

The positive charge pump provides a regulated output voltage set by the external resistor divider. Figure 16 shows an extract of the positive charge-pump driver circuit. The operation of the charge-pump driver can be understood best with Figure 16. During the first cycle, Q3 is turned on and the flying capacitor C_{fly} charges to the source voltage, V_S . During the next clock cycle, Q3 is turned off and the current source charges the drive pin, DRP, up to the supply voltage, $V_{(SUP)}$. Because the flying capacitor voltage sits on top of the drive pin voltage, the maximum output voltage is $V_{(SUP)} + V_S$. The SUP pin can be connected either to the input voltage V_{IN} of the TPS65161 or the output voltage of the main boost converter V_S .

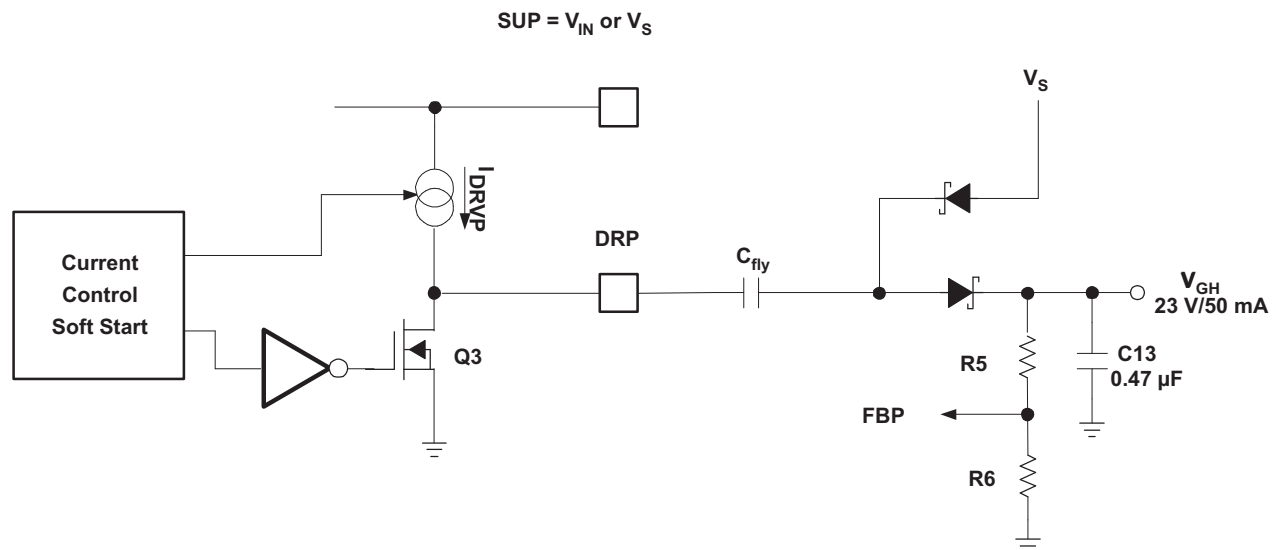


Figure 16. Extract of the Positive Charge-Pump Driver

If higher output voltages are required, another charge-pump stage can be added to the output.

Setting the output voltage:

$$V_{out} = 1.213 \times \left(1 + \frac{R5}{R6} \right)$$

$$R5 = R6 \times \left(\frac{V_{out}}{V_{FB}} - 1 \right) = R6 \times \left(\frac{V_{out}}{1.213} - 1 \right)$$

Negative Charge Pump

The negative charge pump provides a regulated output voltage set by the external resistor divider. The negative charge pump operates similar to the positive charge pump with the difference that it runs from the input voltage V_{IN} . The negative charge pump driver inverts the input voltage. The maximum negative output voltage is $V_{GL} = (-V_{IN}) + V_{drop}$. V_{drop} is the voltage drop across the external diodes and internal charge-pump MOSFETs. In case V_{GL} needs to be lower than $-V_{IN}$, an additional charge-pump stage needs to be added.

Setting the output voltage:

$$V_{out} = -V_{REF} \times \frac{R3}{R4} = -1.213 \text{ V} \times \frac{R3}{R4}$$

$$R3 = R4 \times \frac{|V_{out}|}{V_{REF}} = R4 \times \frac{|V_{out}|}{1.213}$$

The lower feedback resistor value, $R4$, should be in a range between 40 k Ω to 120 k Ω or the overall feedback resistance should be within 500 k Ω to 1 M Ω . Smaller values load the reference too heavily, and larger values may cause stability problems. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode has to be twice the load current of the output. For a 20-mA output current, the dual-Schottky diode BAV99 is a good choice.

Power-On Sequencing (EN1, EN2, DLY1, DLY2)

The TPS65161 has an adjustable power-on sequencing set by the capacitors connected to DLY1 and DLY2 and controlled by EN1 and EN2. Pulling EN1 high enables the step-down converter and then the negative charge-pump driver. DLY1 sets the delay time between the step-down converter and negative charge-pump driver. EN2 enables the boost converter and positive charge-pump driver at the same time. DLY2 sets the delay time between the step-down converter $V_{(LOGIC)}$ and the boost converter V_S . This is especially useful to adjust the delay when EN2 is always connected to V_{IN} . If EN2 goes high after the step-down converter is already enabled, then the delay DLY2 starts when EN2 goes high. See Figure 17 and Figure 18.

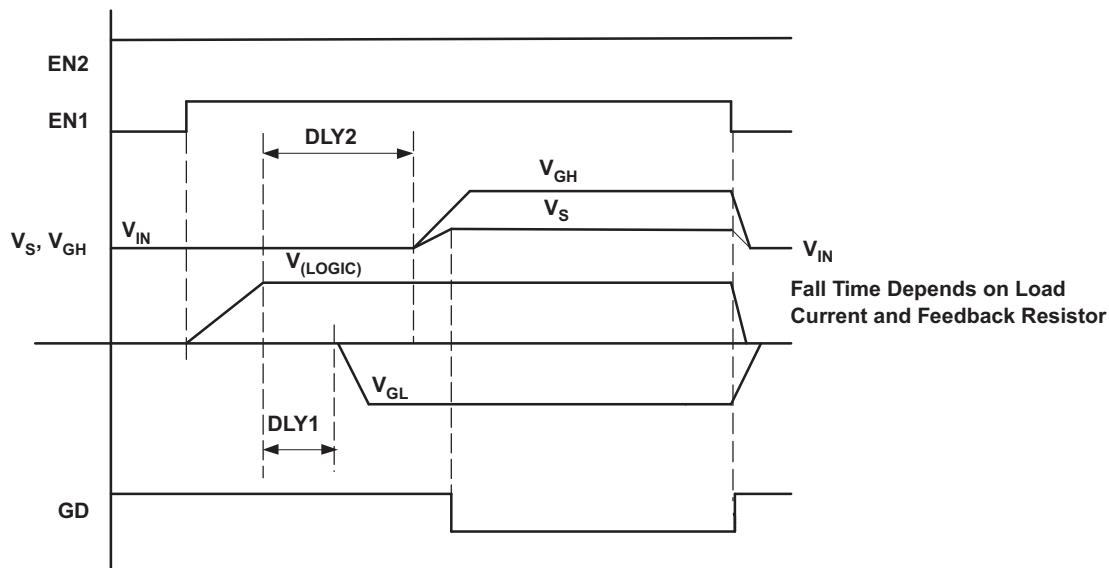


Figure 17. Power-On Sequencing With EN2 Always High (EN2 = V_{IN})

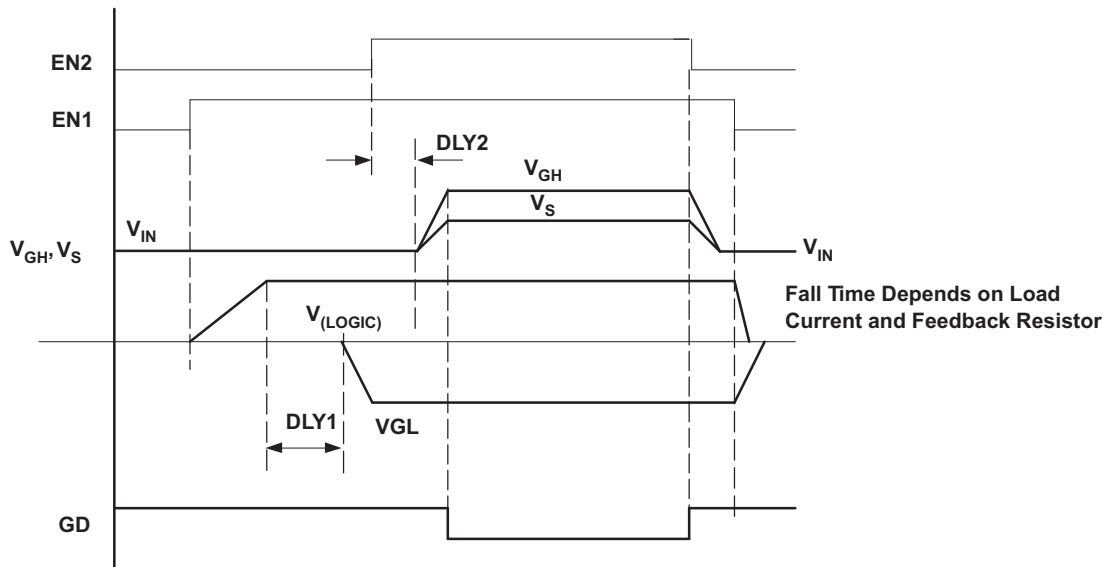


Figure 18. Power-On Sequencing Using EN1 and EN2

Setting the Delay Times DLY1, DLY2

Connecting an external capacitor to the DLY1 and DLY2 pins sets the delay time. If no delay time is required, these pins can be left open. To set the delay time, the external capacitor connected to DLY1 and DLY2 is charged with a constant current source of typically 4.8 μA . The delay time is terminated when the capacitor voltage has reached the internal reference voltage of $V_{\text{ref}} = 1.213 \text{ V}$. The external delay capacitor is calculated:

$$C_{\text{dly}} = \frac{4.8 \mu\text{A} \times t_d}{V_{\text{ref}}} = \frac{4.8 \mu\text{A} \times t_d}{1.213 \text{ V}} \text{ with } t_d = \text{Desired delay time}$$

Example for setting a delay time of 2.3 ms:

$$C_{\text{dly}} = \frac{4.8 \mu\text{A} \times 2.3 \text{ ms}}{1.213 \text{ V}} = 9.4 \text{ nF} \Rightarrow C_{\text{dly}} = 10 \text{ nF}$$

Gate Drive Pin (GD)

This is an open-drain output that goes low when the boost converter, V_S , is within regulation. The gate drive pin GD remains low until the input voltage or enable EN2 is cycled to ground.

Undervoltage Lockout

To avoid incorrect operation of the device at low input voltages, an undervoltage lockout is included which shuts down the device at voltages lower than 6 V.

Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. The TPS65161 has an analog input, AVIN, and two input pins for the buck converter VINB. A 1- μF input capacitor should be connected directly from the AVIN to GND. Two 22- μF ceramic capacitors are connected in parallel from the buck converter input VINB to GND. For better input voltage filtering, the input capacitor values can be increased. See [Table 1](#) and the Application Information section for input capacitor recommendations.

Table 1. Input Capacitor Selection

| CAPACITOR | VOLTAGE RATING | COMPONENT SUPPLIER | COMMENTS |
|------------|----------------|---------------------------|------------------------|
| 22 µF/1210 | 16 V | Taiyo Yuden EMK325BY226MM | C _{IN} (VINB) |
| 1 µF/1206 | 16 V | Taiyo Yuden EMK316BJ106KL | C _{IN} (AVIN) |

Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to use the converter efficiency, by taking the efficiency numbers from the provided efficiency curves or to use a worst-case assumption for the expected efficiency, e.g., 80%.

- Duty Cycle:
$$D = 1 - \frac{V_{in} \times \eta}{V_{out}}$$
- Maximum output current:
$$I_{avg} = (1 - D) \times I_{sw} = \frac{V_{in}}{V_{out}} \times 2.8 \text{ A with } I_{sw} = \text{minimum switch current of the TPS65161 (2.8 A).}$$
- Peak switch current:
$$I_{swpeak} = \frac{V_{in} \times D}{2 \times f_s \times L} + \frac{I_{out}}{1 - D}$$

With

I_{sw} = converter switch current (minimum switch current limit = 2.8 A)

f_s = converter switching frequency (typical 500 kHz/750 kHz)

L = Selected inductor value

η = Estimated converter efficiency (use the number from the efficiency curves or 0.8 as an estimation)

The peak switch current is the steady-state peak switch current that the integrated switch, inductor, and external Schottky diode must be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest.

Inductor Selection (Boost Converter)

The TPS65161 operates typically with a 10-µH inductor. Other possible inductor values are 6.8-µH or 22-µH. The main parameter for the inductor selection is the saturation current of the inductor, which should be higher than the peak switch current as previously calculated, with additional margin to cover for heavy load transients. The alternative, more conservative approach, is to choose the inductor with saturation current at least as high as the typical switch current limit of 3.5 A. The second important parameter is the inductor dc resistance. Usually, the lower the dc resistance the higher the efficiency. The efficiency difference between different inductors can vary between 2% to 10%. Possible inductors are shown in [Table 2](#).

Table 2. Inductor Selection (Boost Converter)

| INDUCTOR VALUE | COMPONENT SUPPLIER | DIMENSIONS in mm | I _{sat} /DCR |
|----------------|------------------------------|--------------------|-----------------------|
| 22 µH | Coilcraft MSS1038-103NX | 10,2 × 10,2 × 3,6 | 2.9 A/73 mΩ |
| 22 µH | Coilcraft DO3316-103 | 12,85 × 9,4 × 5,21 | 3.8 A/38 mΩ |
| 10 µH | Sumida CDRH8D43-100 | 8,3 × 8,3 × 4,5 | 4.0 A/29 mΩ |
| 10 µH | Sumida CDH74-100 | 7,3 × 8,0 × 5,2 | 2.75 A/43 mΩ |
| 10 µH | Coilcraft MSS1038-103NX | 10,2 × 10,2 × 3,6 | 4.4 A/35 mΩ |
| 6.8 µH | Wuerth Elektronik 7447789006 | 7,3 × 7,3 × 3,2 | 2.5 A/44 mΩ |

Output Capacitor Selection (Boost Converter)

For best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value and work best with the TPS65161. Usually, three 22-µF ceramic output capacitors in parallel are sufficient for most applications. If a lower voltage drop during load transients is required, more output capacitance can be added. See [Table 3](#) for the selection of the output capacitor.

Table 3. Output Capacitor Selection (Boost Converter)

| CAPACITOR | VOLTAGE RATING | COMPONENT SUPPLIER |
|------------|----------------|---------------------------|
| 22 µF/1812 | 16 V | Taiyo Yuden EMK432BJ226MM |

Rectifier Diode Selection (Boost Converter)

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the converter. The average rectified forward-current rating needed for the Schottky diode is calculated as the off-time of the converter times the maximum switch current of the TPS65161:

$$D = 1 - \frac{V_{in}}{V_{out}}$$

$$I_{avg} = (1 - D) \times I_{sw} = \frac{V_{in}}{V_{out}} \times 2.8 \text{ A with } I_{sw} = \text{minimum switch current of the TPS65161 (2.8 A).}$$

Usually, a Schottky diode with 2-A maximum average rectified forward-current rating is sufficient for most applications. Secondly, the Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

$$P_D = I_{avg} \times V_F = I_{sw} \times (1 - D) \times V_F \text{ (with } I_{sw} = \text{minimum switch current of the TPS65161 (2.8 A).}$$

Table 4. Rectifier Diode Selection (Boost Converter)

| CURRENT RATING I_{avg} | V_r | $V_{forward}$ | $R_{\theta JA}$ | SIZE | COMPONENT SUPPLIER |
|-----------------------------|-------|---------------|-----------------|------|----------------------------------|
| 3 A | 20 V | 0.36 at 3 A | 46°C/W | SMC | MBRS320, International Rectifier |
| 2 A | 20 V | 0.44 V at 3 A | 75°C/W | SMB | SL22, Vishay Semiconductor |
| 2 A | 20 V | 0.5 at 2 A | 75°C/W | SMB | SS22, Fairchild Semiconductor |

Setting the Output Voltage and Selecting the Feedforward Capacitor (Boost Converter)

The output voltage is set by the external resistor divider and is calculated as:

$$V_{out} = 1.146 \text{ V} \times \left(1 + \frac{R1}{R2}\right)$$

Across the upper resistor, a bypass capacitor is required to achieve a good load transients response and to have a stable converter loop. Together with R1, the bypass capacitor C_{ff} sets a zero in the control loop. Depending on the inductor value, the zero frequency needs to be set. For a 6.8-µH or 10-µH inductor, $f_z = 10 \text{ kHz}$ and for a 22-µH inductor, $f_z = 7 \text{ kHz}$.

$$C_{ff} = \frac{1}{2 \times \pi \times f_z \times R1} = \frac{1}{2 \times \pi \times 10 \text{ kHz} \times R1}$$

A value coming closest to the calculated value should be used.

Compensation (COMP) (Boost Converter)

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. A single capacitor connected to this pin sets the low-frequency gain. Usually, a 22-nF capacitor is sufficient for most of the applications. Adding a series resistor sets an additional zero and increases the high-frequency gain. The following formula calculates at what frequency the resistor increases the high-frequency gain.

$$f_z = \frac{1}{2 \times \pi \times C_c \times R_c}$$

Lower input voltages require a higher gain and therefore a lower compensation capacitor value.

Step-Down Converter Design Procedure

Setting the Output Voltage

The step-down converter uses an external voltage divider to set the output voltage. The output voltage is calculated as:

$$V_{\text{out}} = 1.213 \text{ V} \times \left(1 + \frac{R1}{R2}\right)$$

with R2 as 1.2 kΩ, and internal reference voltage $V_{(\text{ref})\text{typ}} = 1.213 \text{ V}$

At load current <1 mA, the device operates in discontinuous conduction mode. When the load current is reduced to zero, the output voltage rises slightly above the nominal output voltage. At zero load current, the device skips clock cycles but does not completely stop switching; thus, the output voltage sits slightly higher than the nominal output voltage. Therefore, the lower feedback resistor is selected to be around 1.2 kΩ to always have around 1-mA minimum load current.

Selecting the Feedforward Capacitor

The feedforward capacitor across the upper feedback resistor divider sets a zero in the converter loop transfer function. For a 15-μH inductor, $f_z = 8 \text{ kHz}$ and when a 22-μH inductor is used, $f_z = 17 \text{ kHz}$.

(Example for the 3.3-V output)

$$C_z = \frac{1}{2 \times \pi \times 8 \text{ kHz} \times R1} = \frac{1}{2 \times \pi \times 8 \text{ kHz} \times 2\text{k}\Omega} = 9.9 \text{ nF} \approx 10 \text{ nF}$$

Usually a capacitor value closest to the calculated value is selected.

Inductor Selection (Step-Down Converter)

The TPS65161 typically operates with a 15-μH inductor value. For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. This needs to be considered when selecting the appropriate inductor. In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter, plus the inductor ripple current that is calculated as:

$$\Delta I_L = V_{\text{out}} \times \frac{1 - \frac{V_{\text{out}}}{V_{\text{in}}}}{L \times f} \quad I_{L\text{max}} = I_{\text{outmax}} + \frac{\Delta I_L}{2}$$

With:

f = Switching frequency (750 kHz, 500 kHz minimal)

L = Inductor value (typically 15 μH)

ΔI_L = Peak-to-peak inductor ripple current

$I_{L\text{max}}$ = Maximum inductor current

The highest inductor current occurs at maximum V_{IN} . A more conservative approach is to select the inductor current rating just for the typical switch current of 3.2 A.

Table 5. Inductor Selection (Step-Down Converter)

| INDUCTOR VALUE | COMPONENT SUPPLIER | DIMENSIONS in mm | Isat/DCR |
|----------------|-------------------------|-------------------|---------------|
| 15 μH | Wuerth 7447789115 | 7,3 × 7,3 × 3,2 | 1.75 A/100 mΩ |
| 15 μH | Sumida CDRH8D28-150 | 8,3 × 8,3 × 3,0 | 1.9 A/53 mΩ |
| 15 μH | Sumida CDRH8D38-150 | 8,3 × 8,3 × 4,0 | 2.3 A/53 mΩ |
| 15 μH | Coilcraft MSS1038-153NX | 10,2 × 10,2 × 3,6 | 2.7 A/50 mΩ |

Rectifier Diode Selection (Step-Down Converter)

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the step-down converter. The averaged rectified forward current at which the Schottky diode needs to be rated is calculated as the off-time of the step-down converter times the maximum switch current of the TPS65161:

$$D = \frac{V_{out}}{V_{in}}$$

$$I_{avg} = (1 - D) \times I_{sw} = \left(1 - \frac{V_{out}}{V_{in}}\right) \times 2.5 \text{ A with } I_{sw} = \text{minimum switch current of the TPS65161 (2.5 A)}$$

Usually, a Schottky diode with 1.5-A or 2-A maximum average rectified forward current rating is sufficient for most applications. Secondly, the Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

$$P_D = I_{avg} \times V_F = I_{sw} \times (1 - D) \times V_F \text{ with } I_{sw} = \text{minimum switch current of the TPS65161 (2.5 A).} \quad (1)$$

Table 6. Rectifier Diode Selection (Step-Down Converter)

| CURRENT RATING I_{avg} | V_r | $V_{forward}$ | $R_{\theta JA}$ | SIZE | COMPONENT SUPPLIER |
|-----------------------------|-------|----------------|-----------------|------|----------------------------------|
| 3 A | 20 V | 0.36 V at 3 A | 46°C/W | SMC | MBRS320, International Rectifier |
| 2 A | 20 V | 0.44 V at 2 A | 75°C/W | SMB | SL22, Vishay Semiconductor |
| 2 A | 20 V | 0.5 V at 2 A | 75°C/W | SMB | SS22, Fairchild Semiconductor |
| 1.5 A | 20 V | 0.445 V at 1 A | 88°C/W | SMA | SL12, Vishay Semiconductor |

Output Capacitor Selection (Step-Down Converter)

The device is designed to work with ceramic output capacitors. When using a 15-μH inductor, two 22-μF ceramic output capacitors are recommended. More capacitance can be added to improve the load transient response.

Table 7. Output Selection (Step-Down Converter)

| CAPACITOR | VOLTAGE RATING | COMPONENT SUPPLIER |
|------------|----------------|---------------------------|
| 22 μF/0805 | 6.3 V | Taiyo Yuden JMK212BJ226MG |

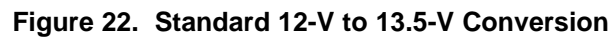
Layout Consideration

The PCB layout is an important step in the power supply design. An incorrect layout could cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching dc-dc converter at high load currents, too-thin PCB traces can cause significant voltage spikes. Good grounding becomes important as well. If possible, a common ground plane to minimize ground shifts between analog (GND) and power ground (PGND) is recommended. Additionally, the following PCB design layout guidelines are recommended for the TPS65161:

1. Separate the power supply traces for AVIN and VINB, and use separate bypass capacitors.
2. Use a short and wide trace to connect the OS pin to the output of the boost converter.
3. To minimize noise coupling into the OS pin, use a 470-nF bypass capacitor to GND.
4. Place the rectifier diode of the step down converter as close as possible to the SWB pin.
5. Use short traces for the charge-pump drive pins (DRN, DRP) of V_{GH} and V_{GL} because these traces carry switching waveforms.
6. Place a 1- μ F bypass capacitor from the SUP pin to GND.
7. Place the flying capacitors as close as possible to the DRP and DRN pin, avoiding a high voltage spike at these pins.
8. Place the Schottky diodes as close as possible to the IC, respective to the flying capacitors connected to the DRP and DRN.
9. Route the feedback network of the negative charge pump away from the drive pin traces (DRN) of the negative charge pump. This avoids parasitic coupling into the feedback network of the negative charge pump giving good output voltage accuracy and load regulation. To do this, use the FREQ pin and trace to isolate DRN from FBN.
10. Connect a 220-nF capacitor directly from the REF pin (24) to GND (23) for a stable and noise free reference voltage.

23







* Suggested values only; should be optimized for specific applications.

Figure 23. Standard 12-V to 17-V Conversion with 100-mA V_{GH} and V_{GL} Output Current

REVISION HISTORY

Changes from Original (April 2006) to Revision A Page

- Added device number TPS65161A 1

Changes from Revision A (September 2007) to Revision B Page

- Changed the ORDERING INFORMATION table 2
- Changed equation From: $D = 1 - (V_{out}/V_{in})$ To: $D = 1 - (V_{in}/V_{out})$ 19
- Changed equation From: $I_{sw} \times (1 \times D)$ To: $I_{sw} \times (1 - D)$ 19
- Changed From: TPS65161 (2.6 A) To: TPS65161 (2.8 A) 19
- Changed equation From: $D = 1 - (V_{out}/V_{in})$ To: $D = (V_{out}/V_{in})$ 21
- Changed From: TPS65161 (2 A) To: TPS65161 (2.5 A) 21
- Changed Title of [Table 7](#) From: Output Selection (Boost Converter) To: Output Selection (Step-Down Converter) 21

Changes from Revision B (November 2007) to Revision C Page

- Added device number TPS65161AB 1
- Changed the ORDERING INFORMATION table 2
- Added new figure - Standard 12-V to 17-V Conversion with 100-mA V_{GH} and V_{GL} Output Current 26

Changes from Revision C (October 2008) to Revision D Page

- Changed N-MOSFET on-resistance (Q1) To: (Q5) 4
- Changed N-MOSFET switch current limit (Q1) To: (Q5) 4
- Changed $r_{DS(ON)}$ - Figure 8 description From: N-channel main switch Q1 To: N-channel main switch Q5 8
- Changed Functional Block Diagram - component Q3 to Q5, add callout for component Q4 13

Changes from Revision D (September 2009) to Revision E Page

- Changed list item 3 From: To minimize noise coupling into the OS pin, use a 470-pF bypass capacitor to GND. To: To minimize noise coupling into the OS pin, use a 470-nF bypass capacitor to GND. 22

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|-----------------------------|
| TPS65161APWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS65161APWPRG4 | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS65161BPWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS65161BPWPRG4 | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS65161PWPR | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TPS65161PWPRG4 | ACTIVE | HTSSOP | PWP | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

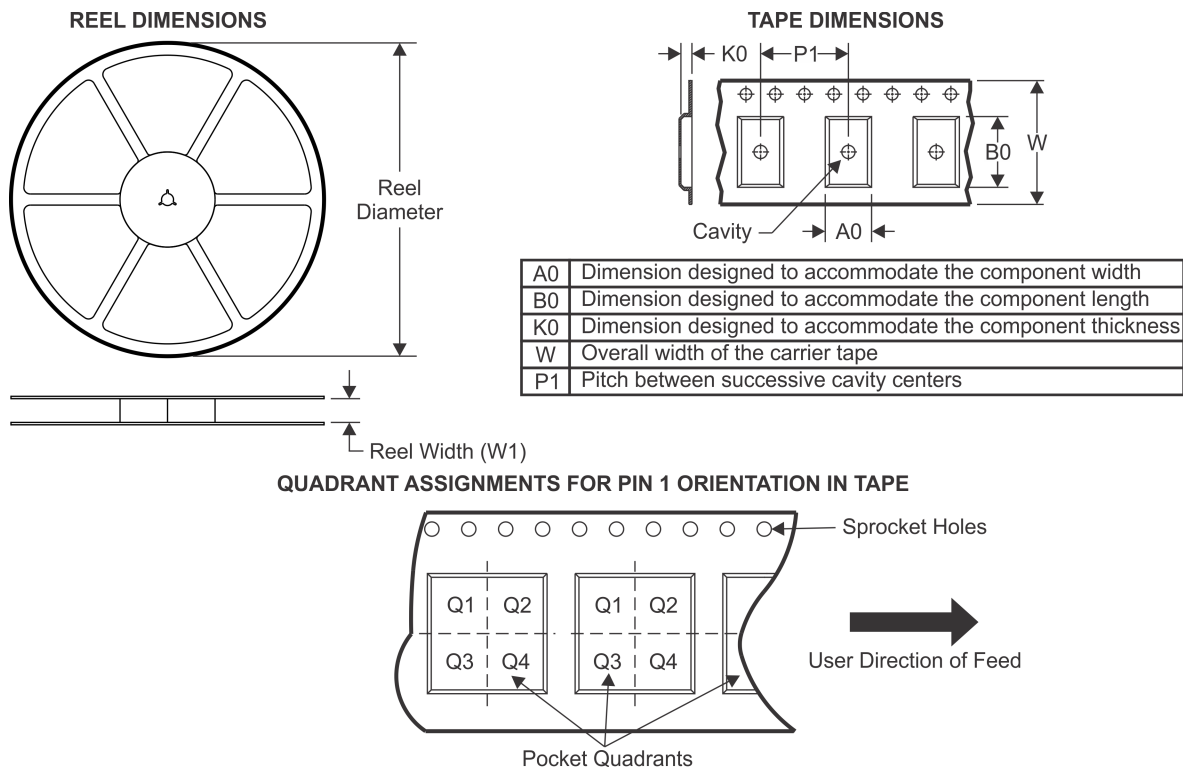
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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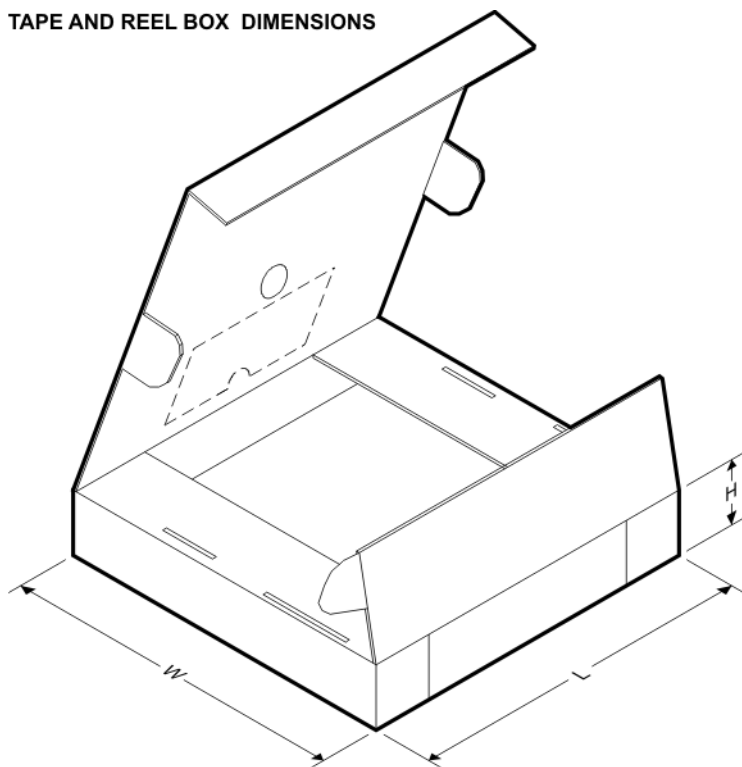
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65161APWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS65161BPWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |
| TPS65161PWPR | HTSSOP | PWP | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

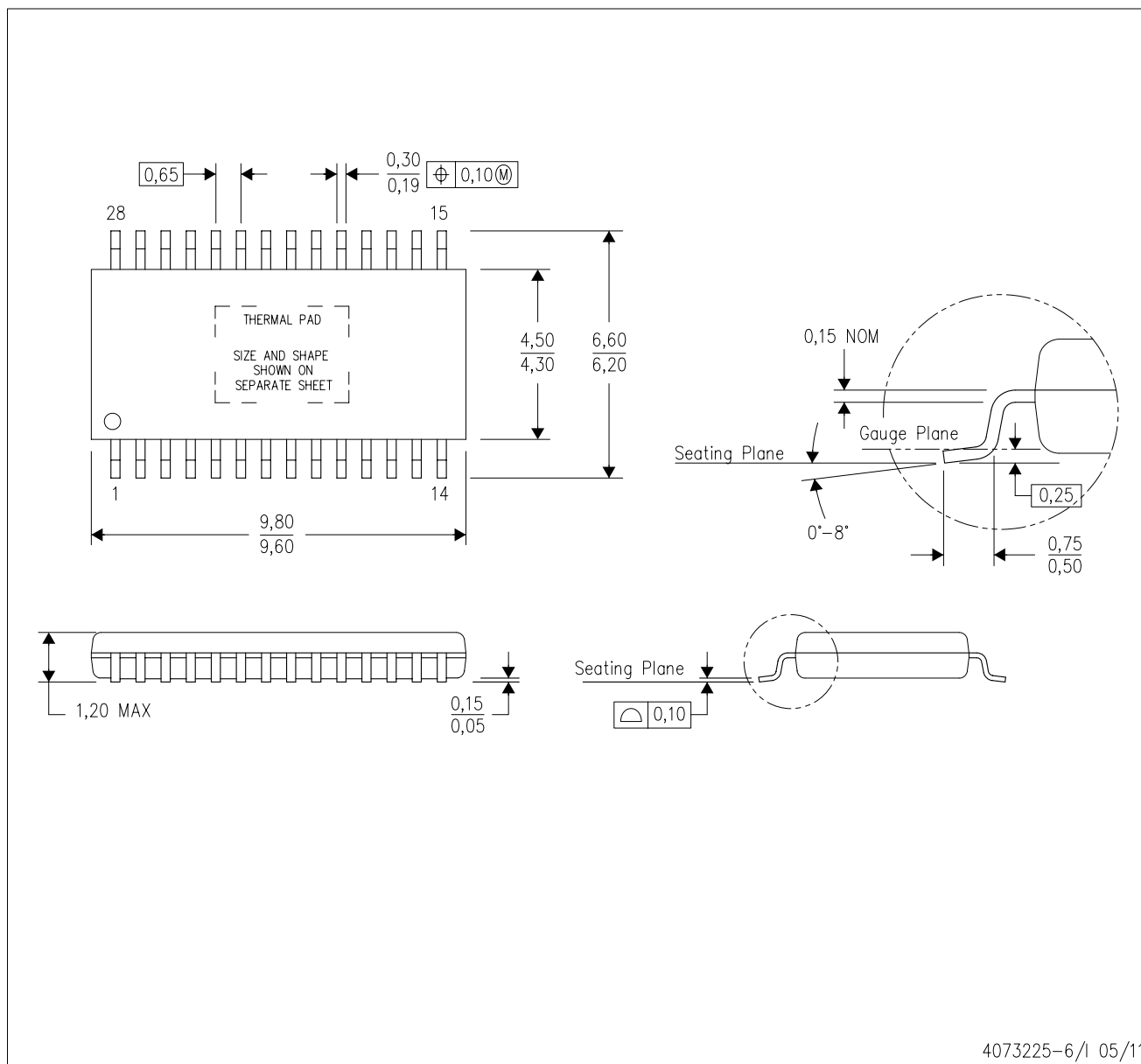


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65161APWPR | HTSSOP | PWP | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS65161BPWPR | HTSSOP | PWP | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS65161PWPR | HTSSOP | PWP | 28 | 2000 | 367.0 | 367.0 | 38.0 |

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

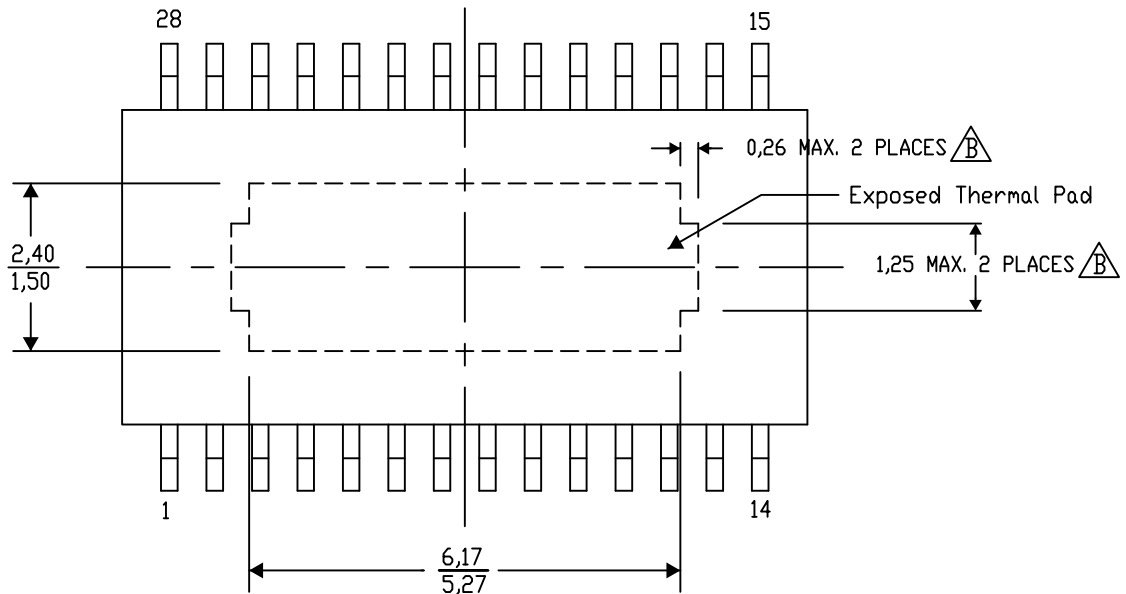
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206332-33/AD 01/13

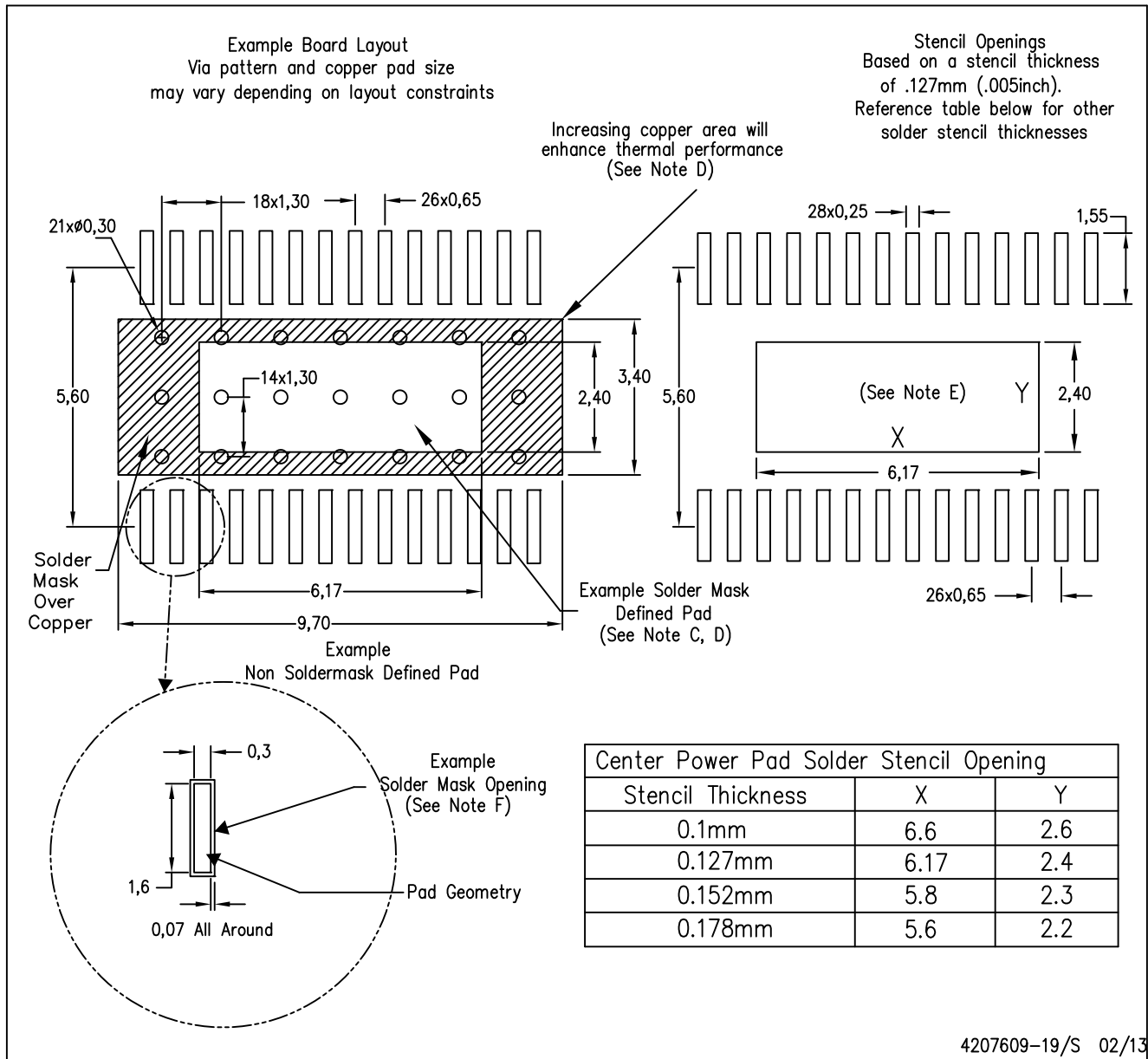
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
 - For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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