A Combination of Flash Memory and Mobile FCRAM™/SRAM– 2 chip Stacked MCP 9mm×9mm Series

This double chip stacked MCP with two different configurations is stored in a common 9mm×9mm package. Compared to our existing MCPs with similar configurations, this series has an at least 39% smaller mounting area.

Product Description

Along with the rapid popularization of mobile phones in recent years, the market needs for mobile devices are becoming increasingly varied. The largest demands by far are for miniaturization and increased functionality. However, high functionality can lead to product enlargement due to the increased number of parts. This dilemma must be solved by miniaturization of the parts themselves, and memory is no exception to this challenge.

Therefore, FUJITSU has developed and commercialized 2 chip stacked MCP 9mm×9mm series, in which the substrate mounting area has been reduced to a maximum of approximately 61%[*1] of the area in existing MCPs with similar configuration.

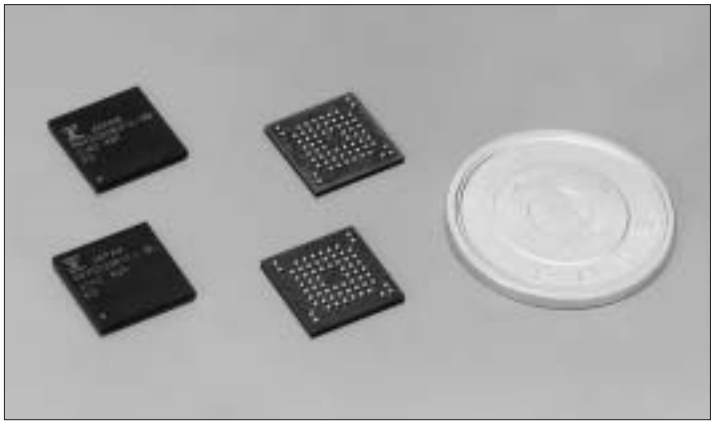
- **MB84VD23280FA**: 64M-bit NOR-type dual-operation flash memory+8M-bit SRAM
- **MB84VD23381FJ**: 64M-bit NOR-type dual-operation flash memory+16M-bit Mobile FCRAM[*2*3]
- **MB84VD23481FJ**: 64M-bit NOR-type dual-operation flash memory+32M-bit Mobile FCRAM
- **MB84VD23581FJ**: 64M-bit NOR-type dual-operation flash memory+64M-bit Mobile FCRAM

The 64M-bit NOR-type dual-operation flash memory mounted in all these products achieves a drastic improvement in chip miniaturization and electric features by means of new process technology. In turn, these improvements mean greater miniaturization and higher performance of the mobile devices.

We have developed our own 16M/32M/64M-bit Mobile FCRAMs as ASMs[*4] for mobile phones. These ASMs simultaneously achieve a high-speed access time of 80/70/70 ns, and a low power consumption with a standby current of 70/100/150 μA and power-down current of 10 μA.

During product development, it can be very expensive and time consuming to restart the development of a mounting substrate with each specification change. Since this product has a common package size and ball arrangement even among

Photo 1 External View



different types, another MCP from the same series can simply replace the MCP once a substrate is developed for this 9mm×9mm series. Hence, changes in memory configuration are easy when the product specification is changed, which helps decrease both product development time and designing cost.

Product Features

Small Packaging

- Size: 9mm×9mm×1.4(t)mm (common for all types)
- Package: FBGA[*5]− 65balls (56 signal balls and 9 reinforcement balls)

The actual mounting area is reduced to approximately 61% of the area in conventional types[*1].

High-Speed Accessing

- /CE access time: 70ns (flash memory). Approximately 18% speedup compared to conventional 64M-bit flash memory.
  80ns (16M-bit Mobile FCRAM)
  70ns (32M-bit Mobile FCRAM and 64M-bit Mobile FCRAM)
- Erase time: 0.2s (typical)/sector (flash memory)

Five times speedup compared to conventional 64M-bit flash memory.

Low Power Consumption Designing

- Standby current: 5μA at maximum (64M-bit flash memory)
  70μA at maximum
  (16M-bit Mobile FCRAM)
  100μA at maximum
  (32M-bit Mobile FCRAM)
  150μA at maximum
  (64M-bit Mobile FCRAM)
  15μA at maximum (8M-bit SRAM)
- Power-down current: 10μA at maximum (16/32/64M-bit Mobile FCRAM)
- Partial power-down[*6] current: 70μA at maximum (at 8M-bit data retaining) (32M-bit Mobile FCRAM)
  85μA at maximum (at 16M-bit data retaining) (64M-bit Mobile FCRAM)
- Read-out operation: 18mA at maximum (at 5MHz operation) (64M-bit flash memory)
  20mA at maximum (16M-bit Mobile FCRAM)
  25mA at maximum (32M/64M-bit Mobile FCRAM)
  40mA at maximum (at 10MHz operation) (8M-bit SRAM)
- Write/Erase operation: 35mA at maximum (64M-bit flash memory)

64M-bit Dual-Operation Flash Memory

Capable of high-speed access at 70ns with low power consumption and standby power consumption of 1μA (typical)

- Configuration: 4-bank configuration with (512-word×16-bit)×2+(1536-word×16-bit)×2

FlexBank™ architecture is adopted so that the 4 banks can be combined at will. Furthermore, the dual-operation function enables simultaneous writing/reading/deleting.

Figure 1 Structure Diagram of Stacked MCP

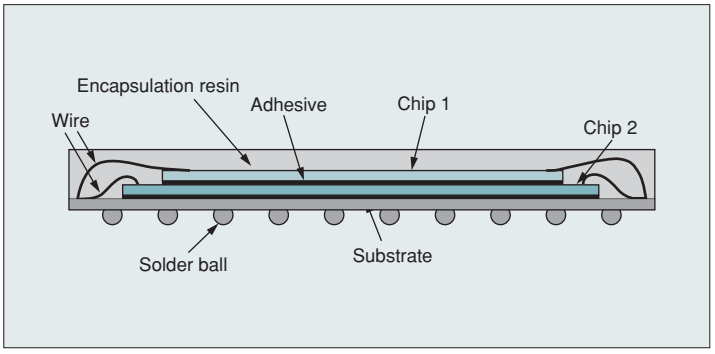
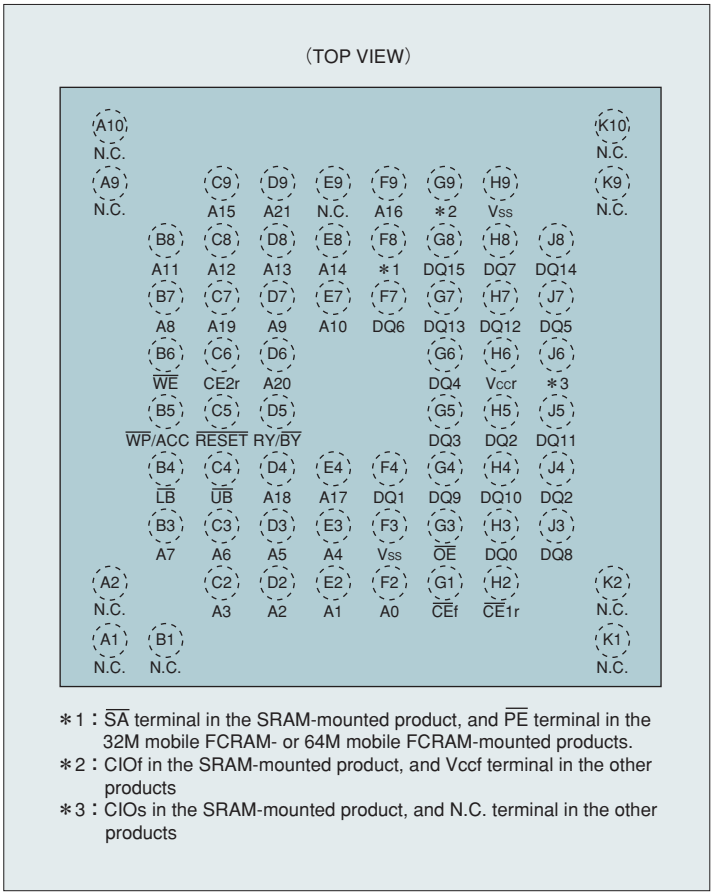


Figure 2 Pin Assignment



*1 : SA terminal in the SRAM-mounted product, and PE terminal in the 32M mobile FCRAM- or 64M mobile FCRAM-mounted products.
*2 : CIOf in the SRAM-mounted product, and Vccf terminal in the other products
*3 : CIOs in the SRAM-mounted product, and N.C. terminal in the other products

Mobile FCRAM

In the double stacked MCP 9mm×9mm series, a 16M-bit, 32M-bit, or 64M-bit is mounted. The 16M-bit mobile FCRAM obtains both high-speed and low power consumption with access time of 80ns while maintaining a maximum of 70μA power consumption during standby. The 32M/64M-bit mobile FCRAM has an even higher access speed of 70ns while mounting 3 types of power-down modes to suppress the power consumption.

Since mobile FCRAM is a pseudo-SRAM which adopts an asynchronous SRAM interface, it costs less than pure SRAM and can be easily introduced as a replacement for pure SRAM in existing systems.

8M-bit SRAM

With the CIOs terminal, data bus width can be switched between ×8 and ×16. Furthermore, this product has 2 terminals, negative logic CE1s and positive logic CE2s, for element selection signal, either of which can be chosen according to the purpose, e.g., decoding, battery backup, etc.

Fig.1 shows the stacked MCP structure diagram, **Fig.2** shows the pin assignment, and **Fig.3** and **4** show the block diagram. **Table 1** shows the main characteristics.

Future Development

This article introduced the stacked MCP 9mm×9mm series, in which a 64M-bit flash memory and various SRAM/mobile FCRAMs are consolidated under a uniform package size. This product facilitates easy memory configuration changes during product development and design, while addressing customer needs for electrical features and small package size.

FUJITSU continues to promote the smooth development and commercialization of MCPs to meet an increasingly diverse range of customer needs. *

Figure 3 Block Diagram (Flash Memory + FCRAM)

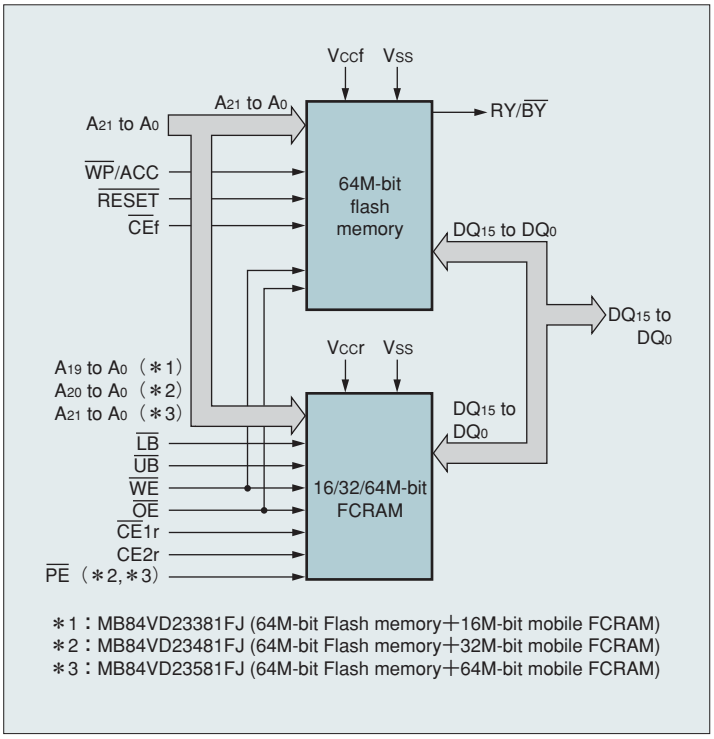
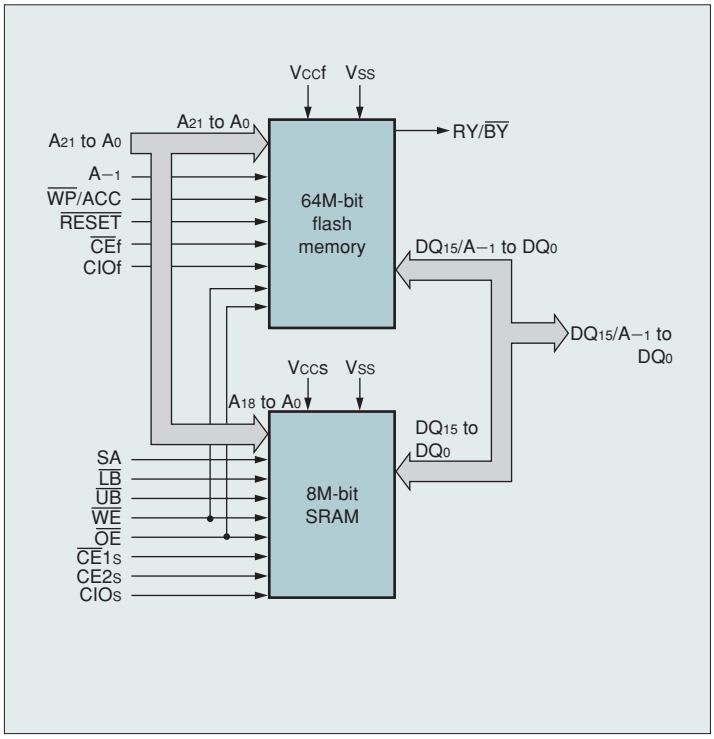


Figure 4 Block Diagram (Flash Memory + SRAM)



NOTES

*1: Compared to MB84VD23381EJ (package size:11mm×12mm×1.4(t)mm) mounted with 64M-bit flash memory and 16M-bit mobile FCRAM.

*2: FCRAM (Fast Cycle Random Access Memory): A high-speed, low power consumption RAM core developed by FUJITSU.

*3: Mobile FCRAM: A low power pseudo-SRAM for mobile phone and mobile terminal applications. It consists of an FCRAM core, and an asynchronous SRAM interface.

*4: ASM (Application Specific Memory): A memory product specialized for individual purposes.

*5: FBGA (Fine-pitch Ball Grid Array): A type of surface-mountable packaging.

*6: Partial Power-Down: An operation mode to reduce power consumption. Only a section with a certain density size of the total density (8M-bit in 32M-bit mobile FCRAM, and 16M-bit in 64M-bit mobile FCRAM) goes into standby (data retention), and the remaining section (24M-bit in 32M-bit mobile FCRAM, and 48M-bit in 64M-bit mobile FCRAM) goes into power-down (no data retention) mode. This reduces the power consumption more than the normal standby mode.

* FCRAM is a trademark of FUJITSU LIMITED.

* FlexBank is a domestic trademark of FUJITSU LIMITED. in Japan.

Table 1 Main Characteristics

Product configuration		MB84VD23280FA	MB84VD23381FJ	MB84VD23481FJ	MB84VD23581FJ
Internal Device		64M-bit dual-operation flash memory			
		8M-bit SRAM	16M-bit mobile FCRAM (second generation product)	32M-bit mobile FCRAM (second generation product)	64M-bit mobile FCRAM (first generation product)
I/O configuration		×8, ×16	×16		
Power supply voltage		2.7 to 3.1V			
Operation temperature		−40 to 85℃	−30 to 85℃		
RAM AC characteristics	Read cycle time	70ns	90ns	70ns	
	Write cycle time	70ns	90ns	70ns	
	/CE access time	70ns	80ns	65ns	
Flash AC characteristics	Read cycle time	70ns			
	Write cycle time	70ns			
	/CE access time	70ns			
RAM current consumption	During operation	40mA (Max.)	20mA (Max.)	25mA (Max.)	
	During standby	15μA (Max.)	70μA (Max.)	100μA (Max.)	150μA (Max.)
	During power down	—	10μA (Max.)		
Flash current consumption	During operation	18mA (Max.)			
	While writing	35mA (Max.)			
	While erasing	35mA (Max.)			
	During standby	5μA (Max.)			
Flash erase time (typical)		0.2s/sector			
Flash write time		8μs (in I/O×8 mode), 16μs (in I/O×16 mode)	16μs		
Package size		9.0mm×9.0mm×1.4 (t) mm			
Ball quantity	Signal	56 (JEDEC standard)			
	Circumference	9			