

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

**TC74HC125AP, TC74HC125AF
TC74HC126AP, TC74HC126AF**

TC74HC125AP/AF Quad Bus Buffer

TC74HC126AP/AF Quad Bus Buffer

The TC74HC125A/126A are high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

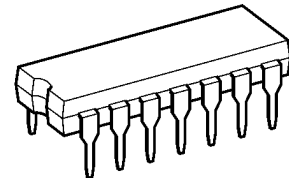
The TC74HC125A requires the 3-state control input $\overline{G}$ to be set high to place the output into the high impedance state, whereas the TC74HC126A requires the control input to be set low to place the output into high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

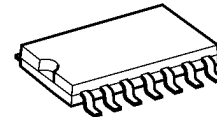
- High speed: $t_{pd} = 10 \text{ ns}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 4 \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6 \text{ mA}$ (min)
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (\text{opr}) = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS125/126

TC74HC125AP, TC74HC126AP



DIP14-P-300-2.54

TC74HC125AF, TC74HC126AF



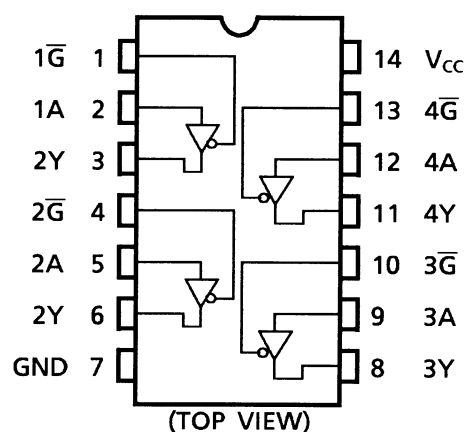
SOP14-P-300-1.27A

Weight

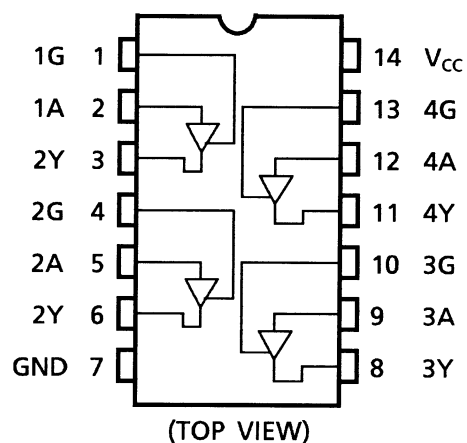
DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)

Pin Assignment

TC74HC125A

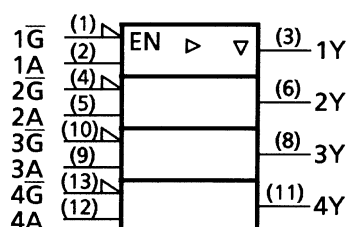


TC74HC126A

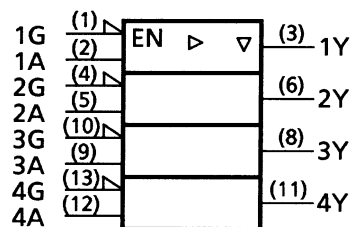


IEC Logic Symbol

TC74HC125A



TC74HC126A



Truth Table

TC74HC125A

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care

Z: High impedance

TC74HC126A

Inputs		Output
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't care

Z: High impedance

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 35	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 ($V_{CC} = 2.0$ V) 0 to 500 ($V_{CC} = 4.5$ V) 0 to 400 ($V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics
DC Characteristics

Characteristics	Symbol	Test Condition		V _{CC} (V)	Ta = 25°C			Ta = –40 to 85°C		Unit
					Min	Typ.	Max	Min	Max	
High-level input voltage	V _{IH}	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low-level input voltage	V _{IL}	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = –20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			I _{OH} = –6 mA I _{OH} = –7.8 mA	6.0	5.9	6.0	—	5.9	—	
				4.5	4.18	4.31	—	4.13	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			I _{OL} = 6 mA I _{OL} = 7.8 mA	6.0	—	0.0	0.1	—	0.1	
				4.5	—	0.17	0.26	—	0.33	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	6.0	—	—	±0.5	—	±5.0	μA	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND	6.0	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	6.0	—	—	4.0	—	40.0	μA	

AC Characteristics (input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			CL (pF)	VCC (V)	Min	Typ.	Max	Min	Max
Output transition time	t_{TLH} t_{THL}	—	50	2.0	—	20	60	—	75
				4.5	—	6	12	—	15
				6.0	—	5	10	—	13
Propagation delay time	t_{pLH} t_{pHL}	—	50	2.0	—	30	90	—	115
				4.5	—	11	18	—	23
				6.0	—	10	15	—	20
			150	2.0	—	42	130	—	165
				4.5	—	14	26	—	33
				6.0	—	12	22	—	28
Output enable time	t_{pZL} t_{pZH}	$R_L = 1 \text{ k}\Omega$	50	2.0	—	30	90	—	115
				4.5	—	11	18	—	23
				6.0	—	10	15	—	20
			150	2.0	—	42	130	—	165
				4.5	—	14	26	—	33
				6.0	—	12	22	—	28
Output disable time	t_{pLZ} t_{pHZ}	$R_L = 1 \text{ k}\Omega$	50	2.0	—	24	100	—	125
				4.5	—	12	20	—	25
				6.0	—	10	17	—	21
Input capacitance	C_{IN}	—			—	5	10	—	10
Output capacitance	C_{OUT}	—			—	10	—	—	—
Power dissipation capacitance	C_{PD} (Note)	—			—	41	—	—	—

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

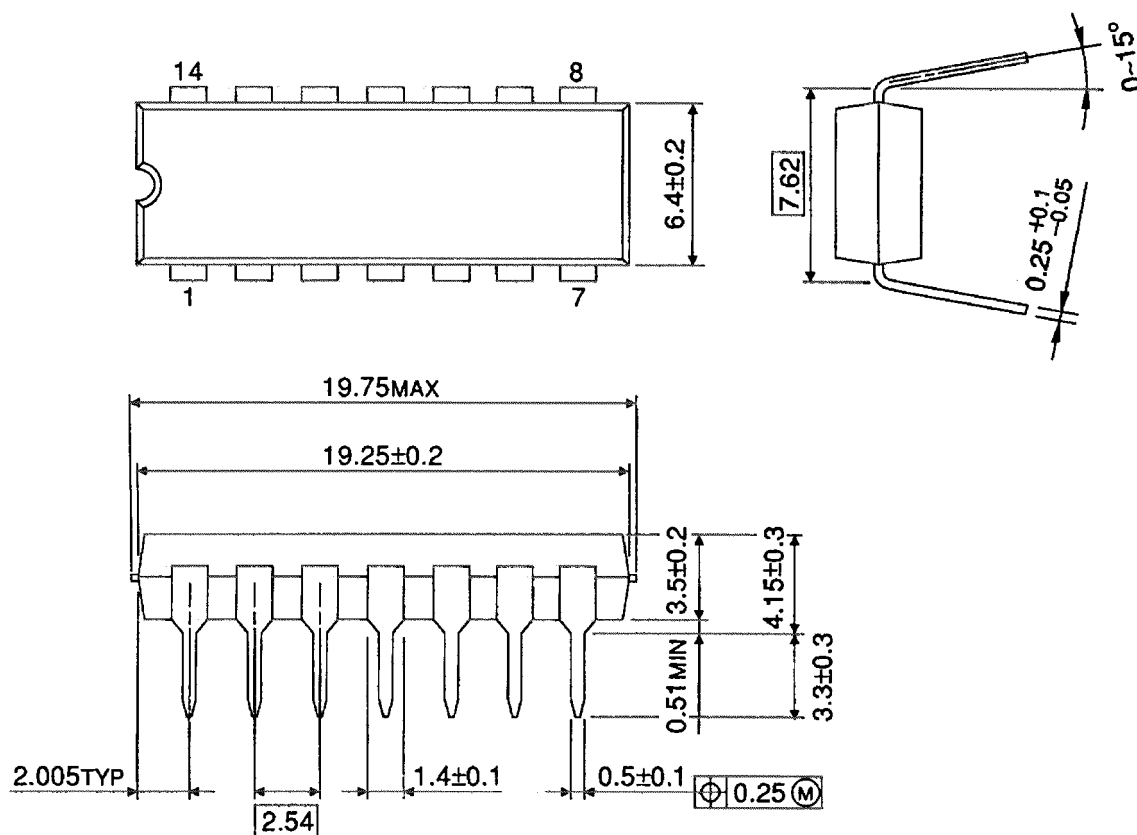
Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

Package Dimensions

DIP14-P-300-2.54

Unit : mm

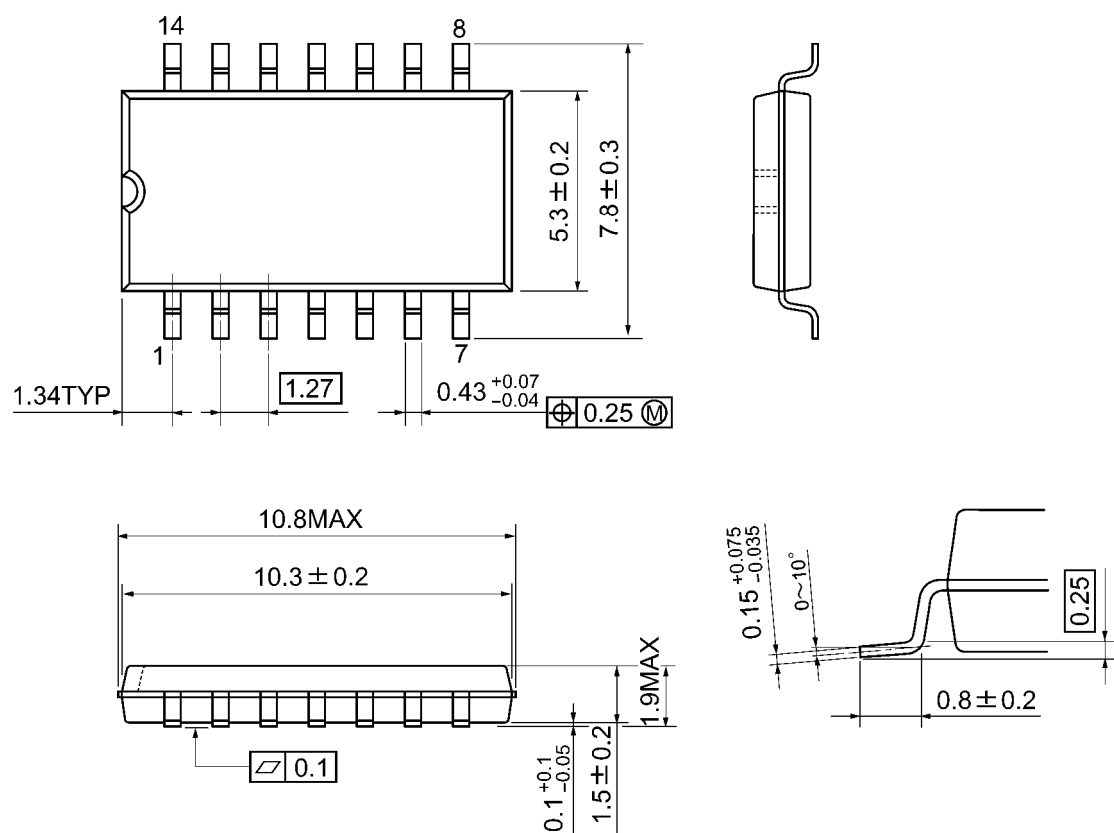


Weight: 0.96 g (typ.)

Package Dimensions

SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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