

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode
Power Field-Effect Transistors

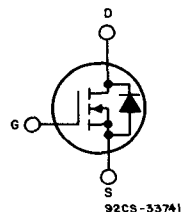
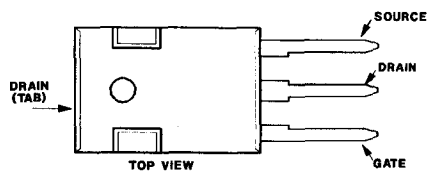
34 A and 40 A, 60 V – 100 V

 $r_{DS(on)} = 0.055 \Omega$ and 0.08Ω **Features:**

- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

The IRFP150, IRFP151, IRFP152, and IRFP153 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

N-CHANNEL ENHANCEMENT MODE**TERMINAL DIAGRAM****TERMINAL DESIGNATION****JEDEC TO-247****Absolute Maximum Ratings**

Parameter		IRFP150	IRFP151	IRFP152	IRFP153	Units
V _{DS}	Drain - Source Voltage ①	100	60	100	60	V
V _{DGR}	Drain - Gate Voltage (R _{GS} = 20 KΩ) ①	100	60	100	60	V
I _D @ T _C = 25°C	Continuous Drain Current ②	40		34		A
I _D @ T _C = 100°C	Continuous Drain Current	26		22		A
I _{DM}	Pulsed Drain Current ②	160		140		A
V _{GS}	Gate - Source Voltage	± 20				V
P _D @ T _C = 25°C	Max. Power Dissipation	180				W
	Linear Derating Factor	1.4				W/°C
I _{LM}	Inductive Current, Clamped	(See Fig. 14) L = 100μH		140		A
T _J T _{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFP150, IRPF151, IRFP152, IRFP153

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DS} Drain - Source Breakdown Voltage	IRFP150	100	—	—	V	$V_{GS} = 0\text{V}$ $I_D = 250\text{ }\mu\text{A}$
	IRFP152	—	—	—	—	
	IRFP151	60	—	—	V	
	IRFP153	—	—	—	—	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	500	nA	$V_{GS} = 20\text{V}$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-500	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0\text{V}$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ④ ⑤	IRFP150	40	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, $V_{GS} = 10\text{V}$
	IRFP151	—	—	—	—	
	IRFP152	34	—	—	A	
	IRFP153	—	—	—	—	
$R_{DS(on)}$ Static Drain-Source On-State Resistance ④	IRFP150	—	0.045	0.055	Ω	$V_{GS} = 10\text{V}$, $I_D = 22\text{A}$
	IRFP151	—	—	—	—	
	IRFP152	—	0.060	0.080	Ω	
	IRFP153	—	—	—	—	
g_{fs} Forward Transconductance ④	ALL	13	20	—	S (②)	$V_{DS} = 2 \times V_{GS}$, $I_{DS} = 20.5$
C_{iss} Input Capacitance	ALL	—	2400	—	pF	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{ MHz}$
C_{oss} Output Capacitance	ALL	—	1000	—	pF	See Fig. 10
C_{rss} Reverse Transfer Capacitance	ALL	—	200	—	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	16	24	ns	$V_{DD} = 50\text{V}$, $I_D \approx 38\text{A}$, $R_G = 6.8\Omega$, $R_D = 1.3\Omega$
t_r Rise Time	ALL	—	140	210	ns	See Fig. 16
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	59	89	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	ALL	—	92	140	ns	
Q_g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	73	110	nC	$V_{GS} = 10\text{V}$, $I_D = 38\text{A}$, $V_{DS} = 0.8\text{ Max. Rating}$. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	18	27	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	27	41	nC	
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.

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Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRFP150	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRFP151	—	—	—	—	
	IRFP152	—	—	34	A	
	IRFP153	—	—	—	—	
I_{SM} Pulse Source Current (Body Diode) ③	IRFP150	—	—	170	A	
	IRFP151	—	—	—	—	
	IRFP152	—	—	140	A	
	IRFP153	—	—	—	—	
V_{SD} Diode Forward Voltage ②	ALL	—	—	2.5	V	$T_C = 25^\circ\text{C}$, $I_S = 41\text{A}$, $V_{GS} = 0\text{V}$
t_{rr} Reverse Recovery Time	ALL	98	220	530	ns	$T_J = 25^\circ\text{C}$, $I_F = 38\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
Q_{RR} Reverse Recovered Charge	ALL	0.41	0.97	2.5	μC	$T_J = 25^\circ\text{C}$, $I_F = 38\text{A}$, $dI_F/dt = 100\text{A}/\mu\text{s}$
t_{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	0.70	$^\circ\text{C}/\text{W}$	
R_{thCS} Case-to-Sink	ALL	—	0.10	—	$^\circ\text{C}/\text{W}$	Mounting surface flat, smooth, and greased.
R_{thJA} Junction-to-Ambient	ALL	—	—	40	$^\circ\text{C}/\text{W}$	Typical socket mount
Mounting Torque	ALL	—	—	10	in. • lbs.	Standard 6-32 screw

① $T_J = 25^\circ\text{C}$ to 150°C .

② Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

③ @ $V_{dd} = 25\text{V}$, $T_J = 25^\circ\text{C}$, $L = 100\text{ }\mu\text{H}$, $R_G = 25\Omega$ ④ Pulse Test: Pulse width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.⑤ I_D current limited by pin diameter

IRFP150, IRFP151, IRFP152, IRFP153

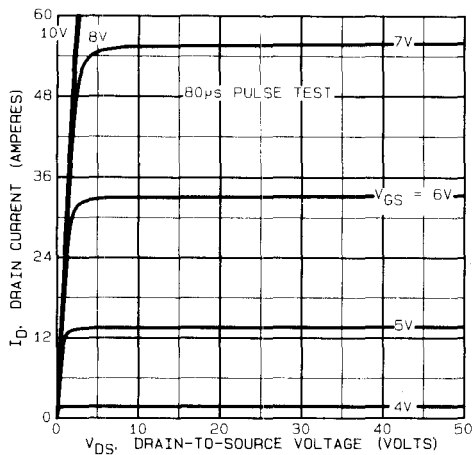


Fig. 1 - Typical Output Characteristics

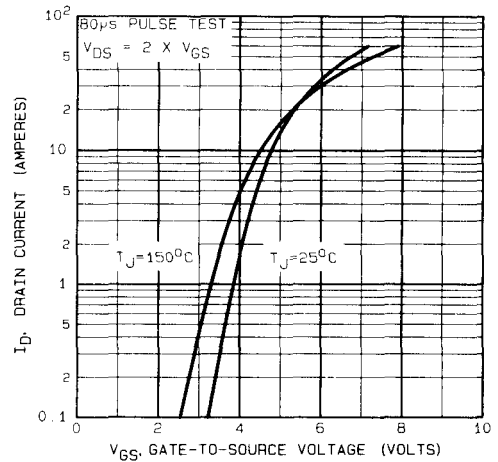


Fig. 2 - Typical Transfer Characteristics

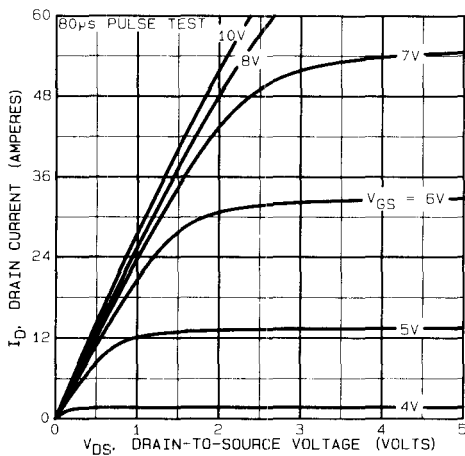


Fig. 3 - Typical Saturation Characteristics

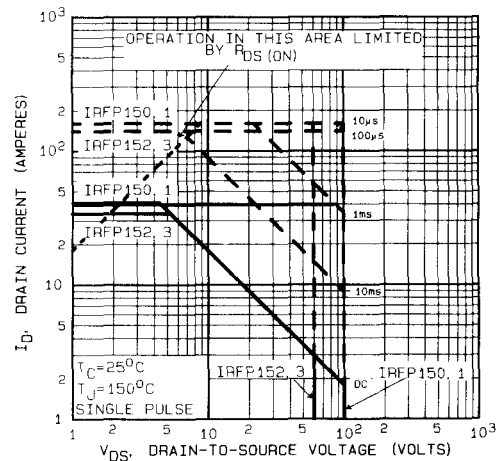


Fig. 4 - Maximum Safe Operating Area

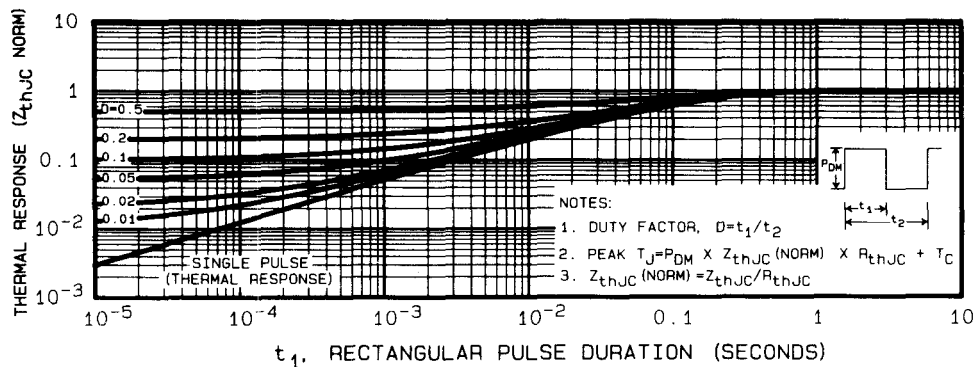


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to Case Vs. Pulse Duration

IRFP150, IRFP151, IRFP152, IRFP153

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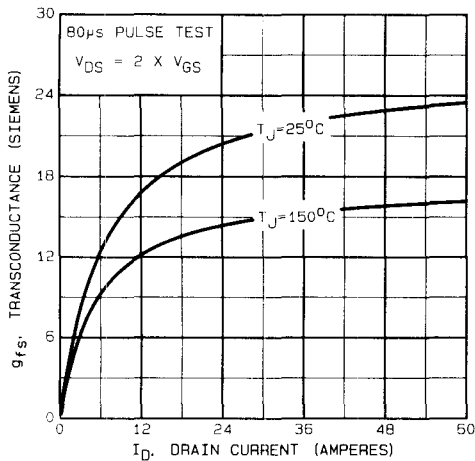


Fig. 6 – Typical Transconductance Vs. Drain Current

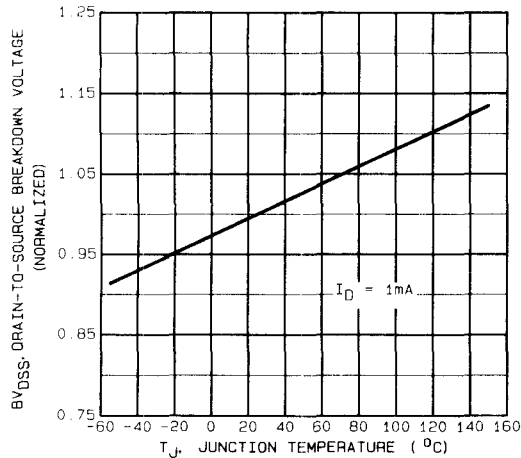


Fig. 8 – Breakdown Voltage Vs. Temperature

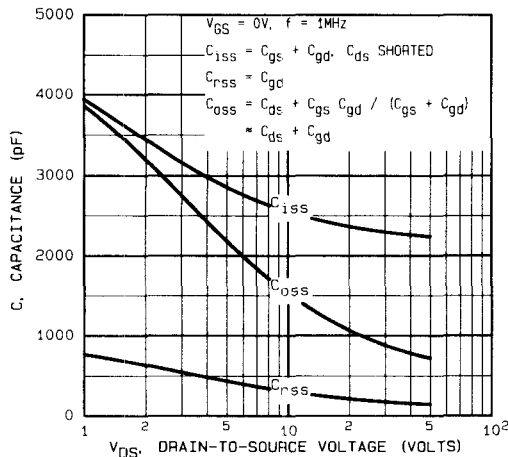


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

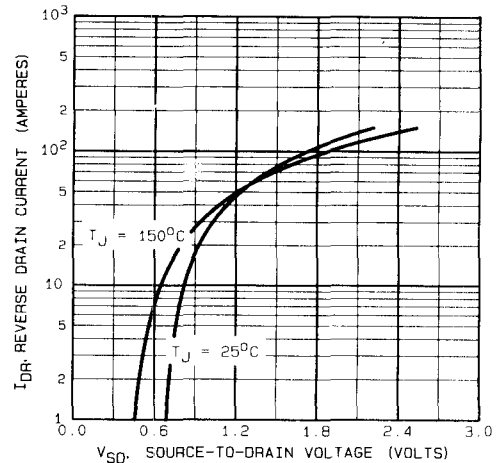


Fig. 7 – Typical Source-Drain Diode Forward Voltage

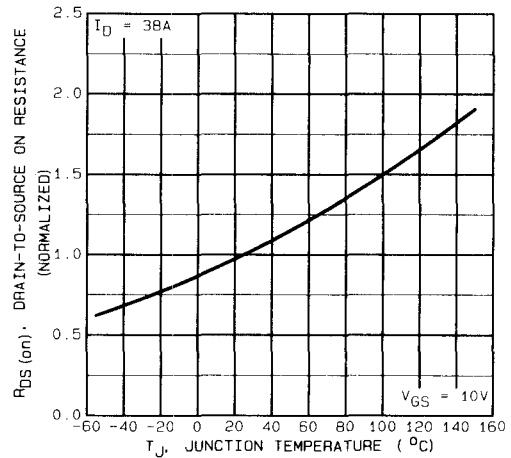


Fig. 9 – Normalized On-Resistance Vs. Temperature

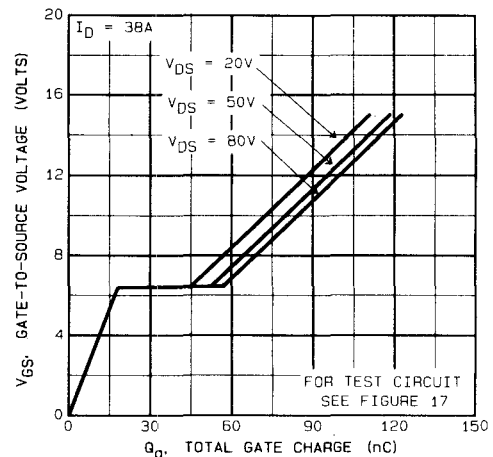


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRFP150, IRFP151, IRFP152, IRFP153

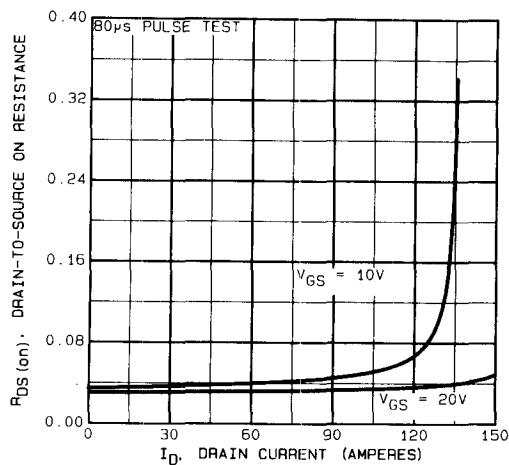


Fig. 12 — Typical On-Resistance Vs. Drain Current

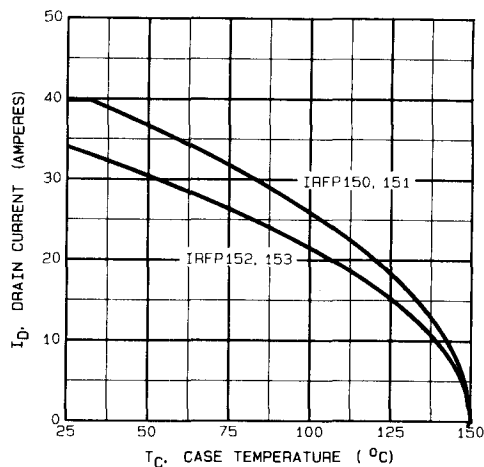


Fig. 13 — Maximum Drain Current Vs. Case Temperature

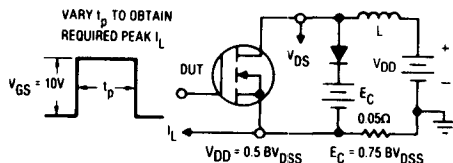


Fig. 14 — Clamped Inductive Test Circuit

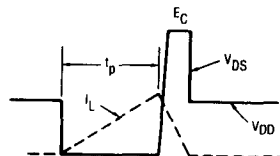


Fig. 15 — Clamped Inductive Waveforms

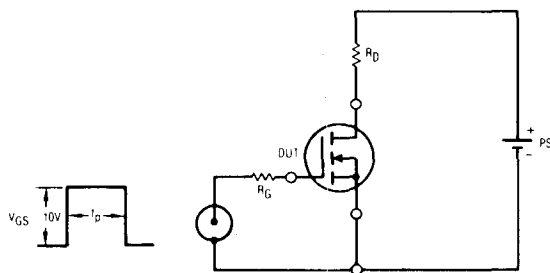


Fig. 16 — Switching Time Test Circuit

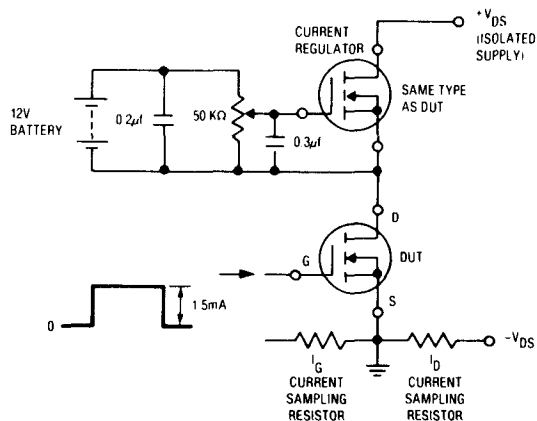


Fig. 17 — Gate Charge Test Circuit