150-mA, 30-V, 1-µA I_Q Voltage Regulators with Enable

FEATURES

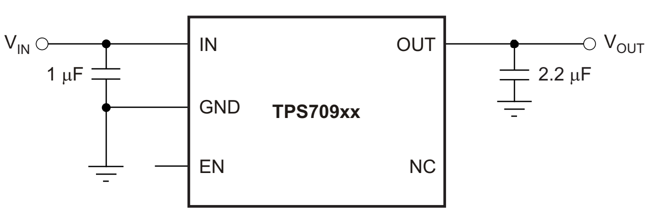
- **Ultralow I_Q: 1 µA**
- **Reverse Current Protection**
- **Low $I_{SHUTDOWN}$: 150 nA**
- **Input Voltage Range: 2.7 V to 30 V**
- **Supports 200-mA Peak Output**
- **Low Dropout: 245 mV at 50 mA**
- **2% Accuracy Over Temperature**
- **Available in Fixed-Output Voltages: 1.2 V to 6.5 V**
- **Thermal Shutdown and Overcurrent Protection**
- **Packages: SOT-23-5, SON-6, SOT-223-4[(1)]**

(1) The SOT-223-4 (DCY) package is a product preview device.

APPLICATIONS

- **Zigbee™ Networks**
- **Home Automation**
- **Metering**
- **Weighing Scales**
- **Portable Power Tools**
- **Remote Control Devices**
- **Wireless Handsets, Smart Phones, PDAs, WLAN, and Other PC Add-On Cards**
- **White Goods**

TYPICAL APPLICATION CIRCUIT



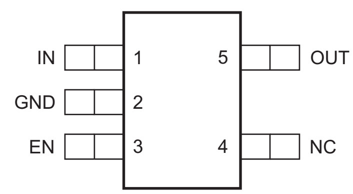
DESCRIPTION

The TPS709xx series of linear regulators are ultralow, quiescent current devices designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. Quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety.

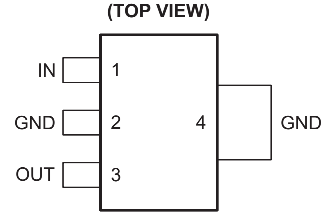
These regulators can be put into shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to 150 nA, typical.

The TPS709xx series is available in SON-6, SOT-23-5, and SOT-223-4 packages.

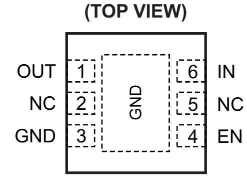
DBV PACKAGE
SOT-23-5
(TOP VIEW)



DCY PACKAGE
SOT-223-4
(TOP VIEW)



DRV PACKAGE
2-mm × 2-mm SON-6
(TOP VIEW)



NOTE: The DCY package is a product preview device.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS[1]

PRODUCT	V_{OUT}
TPS709**xxyyyz**	**XX** is the nominal output voltage (for example 28 = 2.8 V). **YYY** is the package designator **Z** is the package quantity; ***R*** is for reel (3000 pieces), ***T*** is for tape (250 pieces)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

Specified at T_J = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	V_{IN}	–0.3	+32	V
	V_{EN}	–0.3	+7	V
	V_{OUT}	–0.3	+7	V
Maximum output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See the Thermal Information table		
Temperature	Junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		2	kV
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1]		TPS709xx			UNITS
		DBV (SOT-23)	DCY (SOT-223)	DRV (SON)	
		5 PINS	4 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	212.1	64.7	73.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	78.5	47.5	97.0	
θ_{JB}	Junction-to-board thermal resistance	39.5	13.9	42.6	
ψ_{JT}	Junction-to-top characterization parameter	2.86	6.8	2.9	
ψ_{JB}	Junction-to-board characterization parameter	38.7	13.8	42.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	12.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

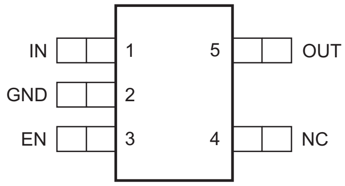
At T_A = –40°C to +85°C, V_{IN} = $V_{OUT\ (typ)}$ + 1 V or 2.7 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = 2 V, and C_{IN} = C_{OUT} = 2.2-μF ceramic, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER		TEST CONDITIONS	TPS709xx MIN	TPS709xx TYP	TPS709xx MAX	UNIT
V_{IN}	Input voltage range		2.7		30	V
V_{OUT}	Output voltage range		1.2		6.5	V
V_O	DC output accuracy	V_{OUT} < 3.3 V	–2		2	%
		V_{OUT} ≥ 3.3 V	–1		1	%
ΔV_O	Line regulation	($V_{OUT(NOM)}$ + 1 V, 2.7 V) ≤ V_{IN} ≤ 30 V		3	10	mV
	Load regulation	V_{IN} = V_{OUT} (typ) + 1.5 V or 3 V (whichever is greater), 100 μA ≤ I_{OUT} ≤ 150 mA		20	50	mV
V_{DO}	Dropout voltage (1) (2)	TPS70933, I_{OUT} = 50 mA		295	650	mV
		TPS70933, I_{OUT} = 150 mA		960	1400	mV
		TPS70950, I_{OUT} = 50 mA		245	500	mV
		TPS70950, I_{OUT} = 150 mA		690	1200	mV
		TPS70965, I_{OUT} = 50 mA		180	500	mV
		TPS70965, I_{OUT} = 150 mA		460	1000	mV
I_{CL}	Output current limit (3)	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	200	320	500	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA, V_{OUT} ≤ 3.3 V		1.3	2.05	μA
		I_{OUT} = 0 mA, V_{OUT} > 3.3 V		1.4	2.25	μA
		I_{OUT} = 150 mA		350		μA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 2.7 V		150		nA
PSRR	Power-supply rejection ratio	f = 10 Hz		80		dB
		f = 100 Hz		62		dB
		f = 1 kHz		52		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 10 mA, V_{IN} = 2.7 V, V_{OUT} = 1.2 V		190		μV_{RMS}
t_{STR}	Start-up time (4)	$V_{OUT(NOM)}$ ≤ 3.3 V		200	600	μs
		$V_{OUT(NOM)}$ > 3.3 V		500	1500	μs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9			V
	Enable pin high (disabled)		0		0.4	V
I_{EN}	EN pin current	EN = 1.0 V, V_{IN} = 5.5 V		300		nA
I_{REV}	Reverse current (flowing out of IN pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		10		nA
	Reverse current (flowing into OUT pin)	V_{OUT} = 3 V, V_{IN} = V_{EN} = 0 V		100		nA
t_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+158		°C
		Reset, temperature decreasing		+140		°C
T_J	Operating junction temperature		–40		+125	°C

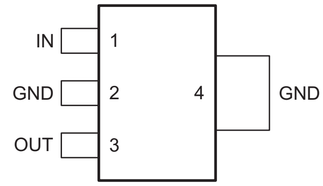
(1) V_{DO} is measured with V_{IN} = 0.98 × $V_{OUT(NOM)}$.
(2) Dropout is only valid when V_{OUT} ≥ 2.8 V because of the minimum input voltage limits.
(3) Measured with V_{IN} = V_{OUT} + 3 V for V_{OUT} ≤ 2.5 V. Measured with V_{IN} = V_{OUT} + 2.5 V for V_{OUT} > 2.5 V.
(4) Startup time = time from EN assertion to 0.95 × $V_{OUT(NOM)}$ and load = 47 Ω.

PIN CONFIGURATIONS

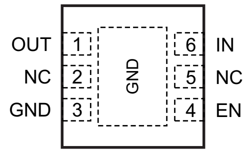
DBV PACKAGE
SOT-23-5
(TOP VIEW)



DCY PACKAGE
SOT-223-4
(TOP VIEW)



DRV PACKAGE
SON-6
(TOP VIEW)

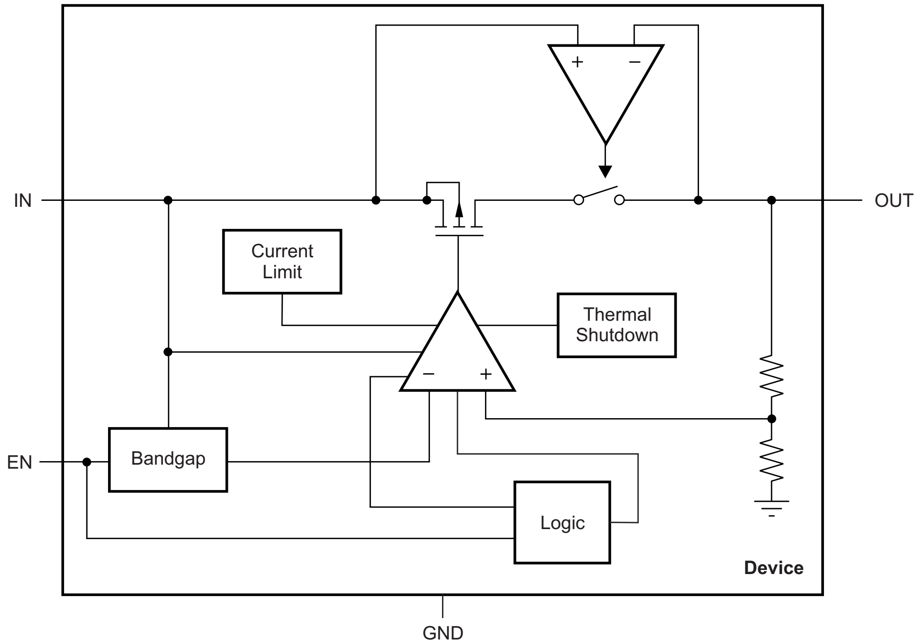


NOTE: The DCY package is a product preview device.

PIN DESCRIPTIONS

PIN NAME	PIN NO.			DESCRIPTION
	DBV	DCY	DRV	
EN	3	—	4	Enable pin. Driving this pin high enables the device. Driving this pin low puts the device into low current shutdown. This pin has an internal pull-up resistor and can be left floating to enable the device.
GND	2	2, 4	3	Ground
IN	1	1	6	Unregulated input to the device
NC	4	—	2, 5	No internal connection
OUT	5	3	1	Regulated output voltage. A small 2.2-µF or greater ceramic capacitor should be connected from this pin to ground to assure stability.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 μF, and V_{IN} = $V_{OUT(TYP)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = +25°C.

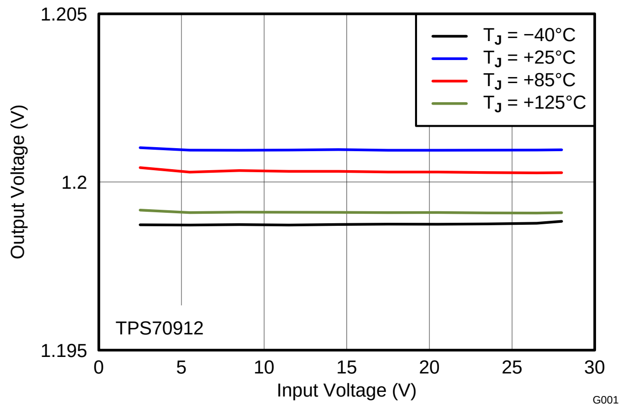


Figure 1. 1.2-V LINE REGULATION vs V_{IN} AND TEMPERATURE

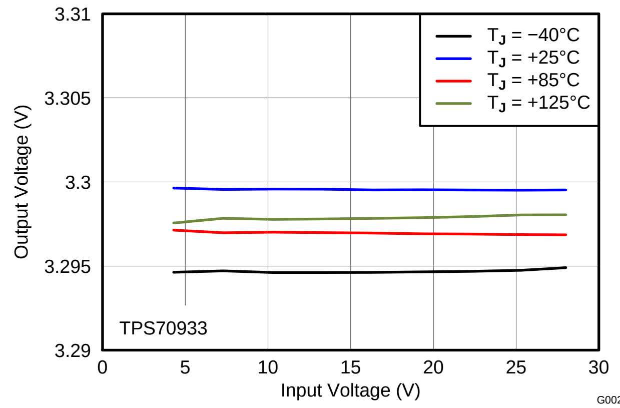


Figure 2. 3.3-V LINE REGULATION vs V_{IN} AND TEMPERATURE

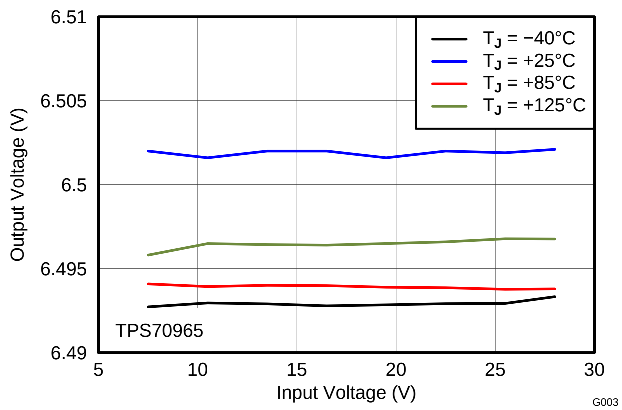


Figure 3. 6.5-V LINE REGULATION vs V_{IN} AND TEMPERATURE

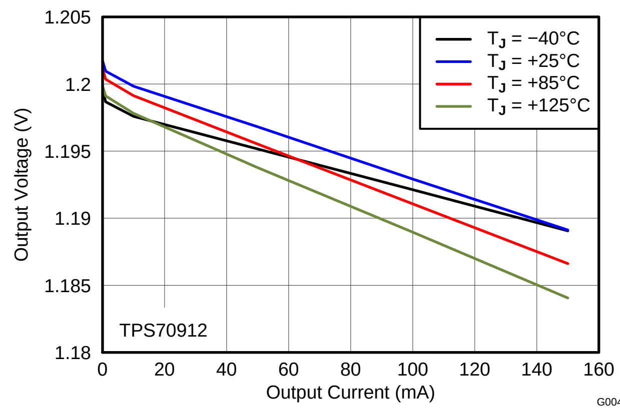


Figure 4. 1.2-V LOAD REGULATION vs I_{OUT} AND TEMPERATURE

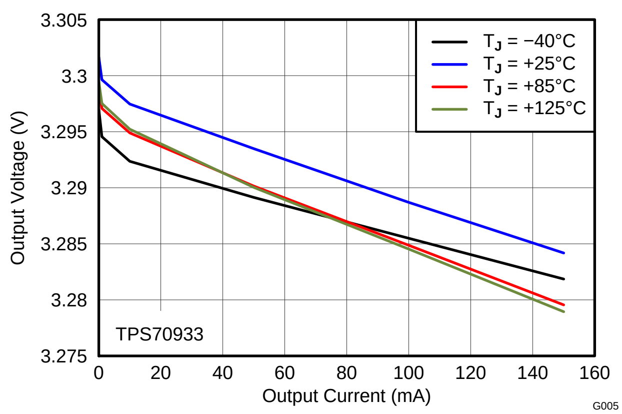


Figure 5. 3.3-V LOAD REGULATION vs I_{OUT} AND TEMPERATURE

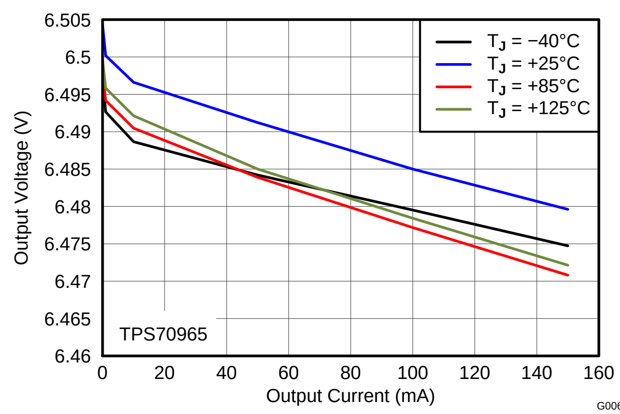


Figure 6. 6.5-V LOAD REGULATION vs I_{OUT} AND TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 μF, and V_{IN} = $V_{OUT(TYP)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = +25°C.

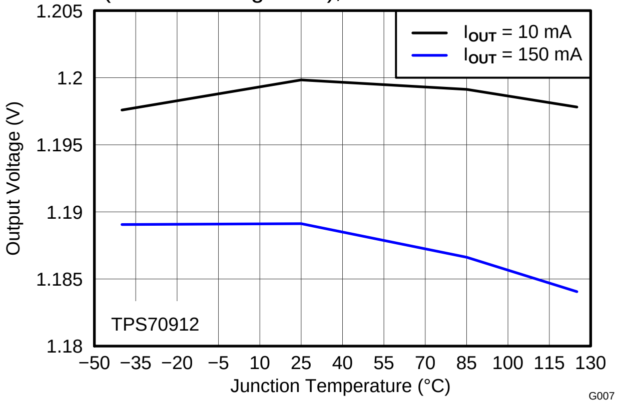


Figure 7. V_{OUT} vs TEMPERATURE

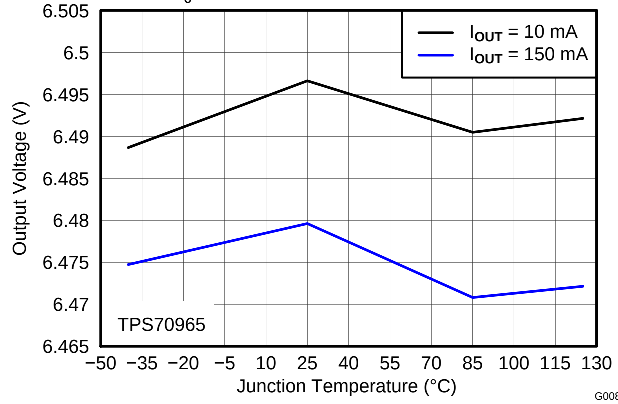


Figure 8. V_{OUT} vs TEMPERATURE

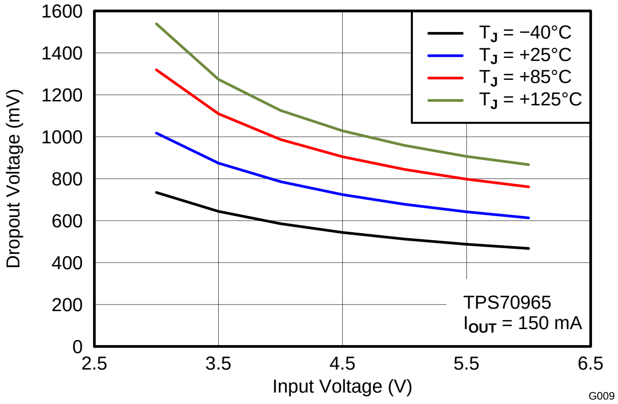


Figure 9. DROPOUT VOLTAGE vs V_{IN} AND TEMPERATURE

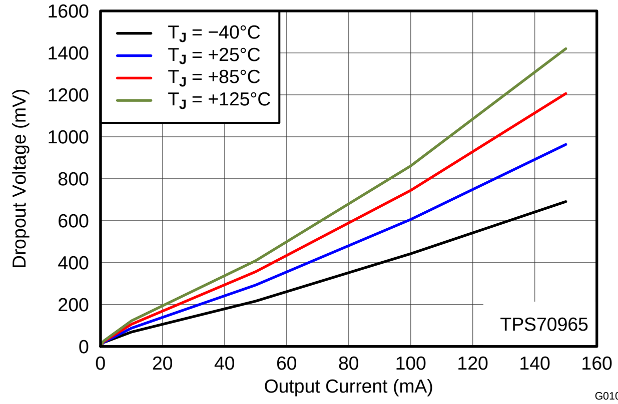


Figure 10. DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE

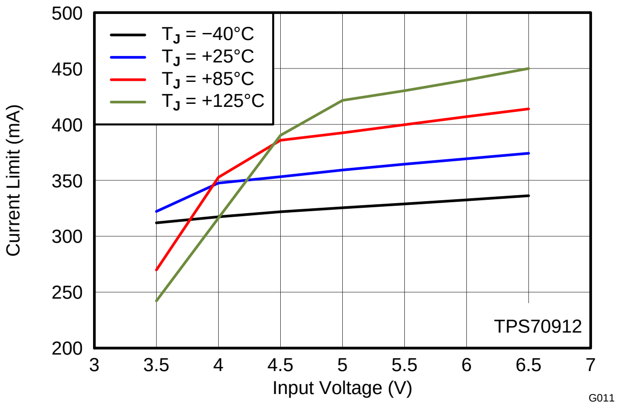


Figure 11. 1.2-V CURRENT LIMIT vs V_{IN} AND TEMPERATURE

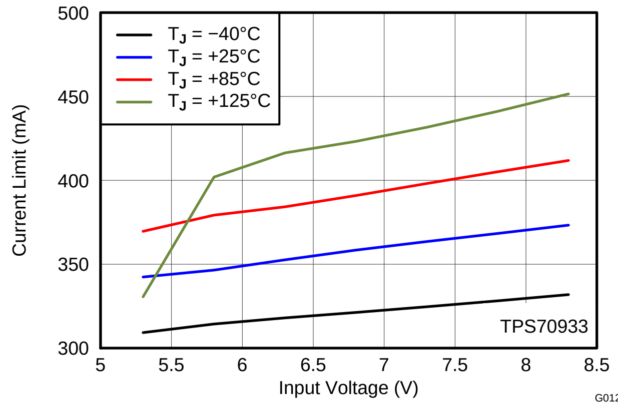


Figure 12. 3.3-V CURRENT LIMIT vs V_{IN} AND TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 μF, and V_{IN} = $V_{OUT(TYP)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = +25°C.

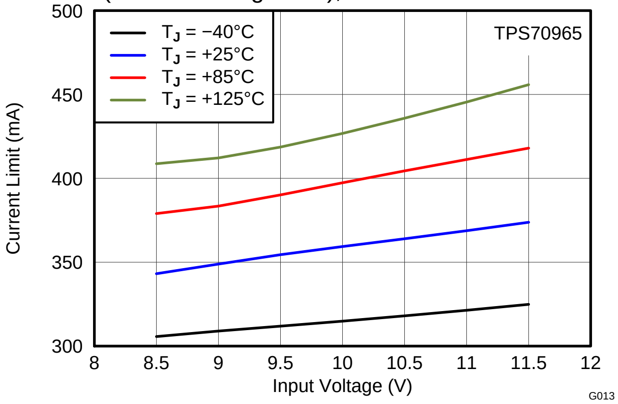


Figure 13. 6.5-V CURRENT LIMIT vs V_{IN} AND TEMPERATURE

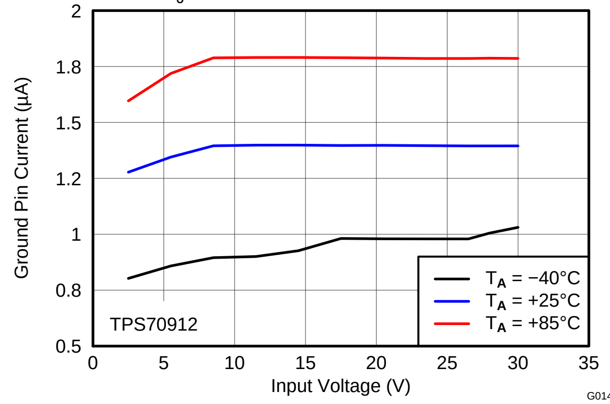


Figure 14. GND CURRENT vs V_{IN} AND TEMPERATURE

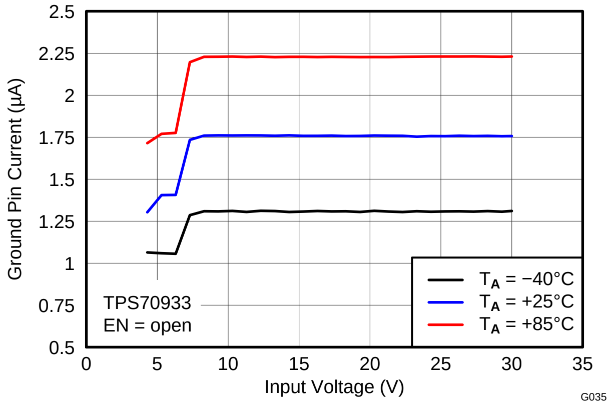


Figure 15. GND CURRENT vs V_{IN} AND TEMPERATURE

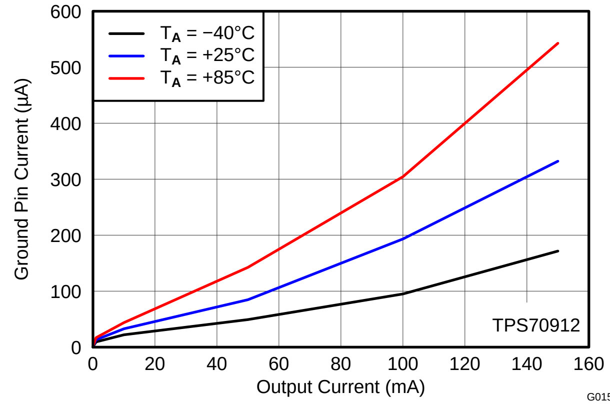


Figure 16. GND CURRENT vs I_{OUT} AND TEMPERATURE

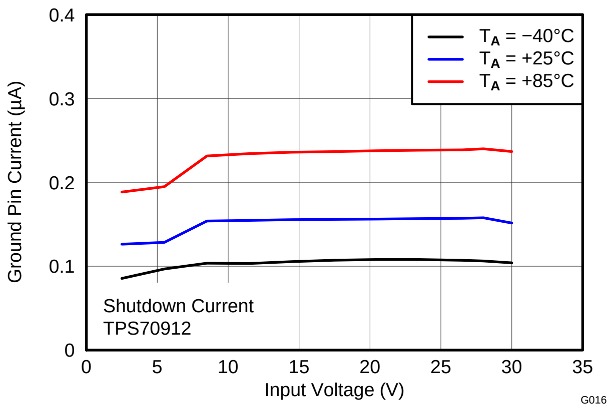


Figure 17. SHUTDOWN CURRENT vs V_{IN} AND TEMPERATURE

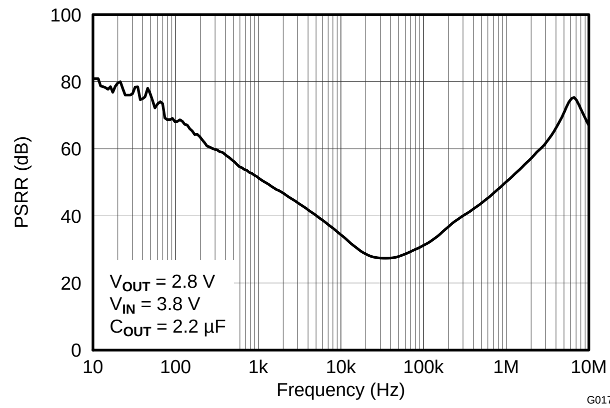


Figure 18. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(TYP)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = +25°C.

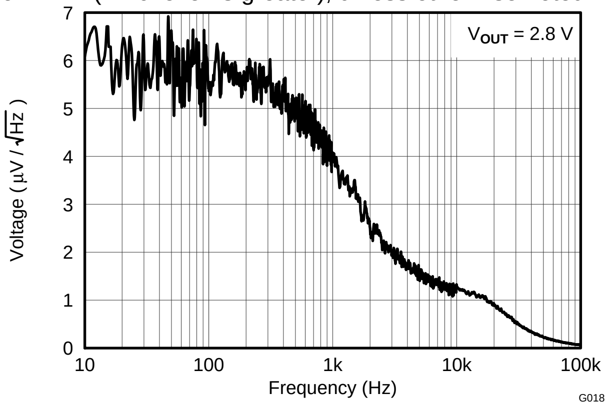


Figure 19. NOISE

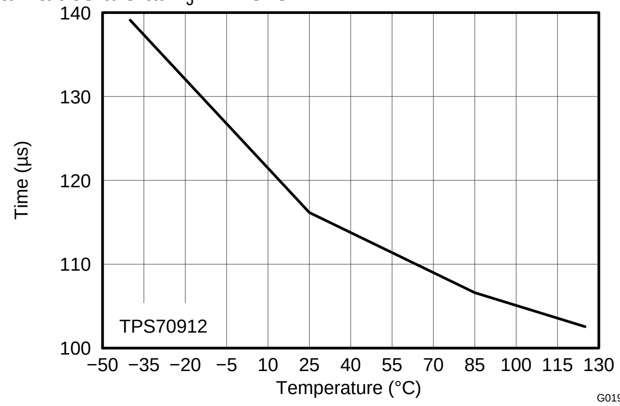


Figure 20. START-UP TIME vs TEMPERATURE

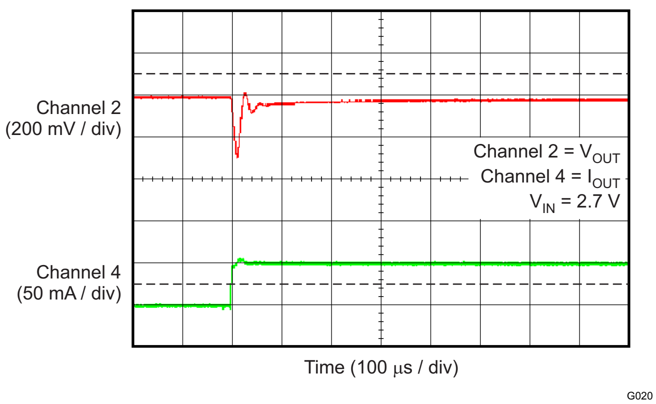


Figure 21. TPS70912 LOAD TRANSIENT (0 mA to 50 mA)

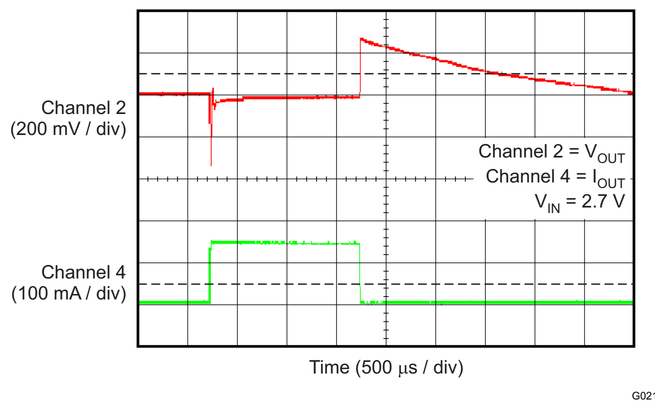


Figure 22. TPS70912 LOAD TRANSIENT (1 mA to 150 mA)

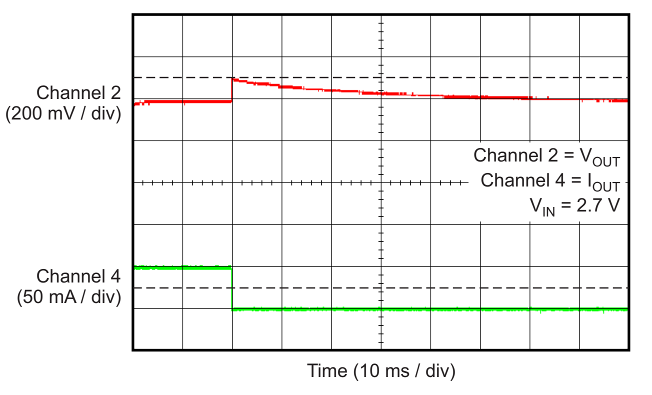


Figure 23. TPS70912 LOAD TRANSIENT (50 mA to 0 mA)

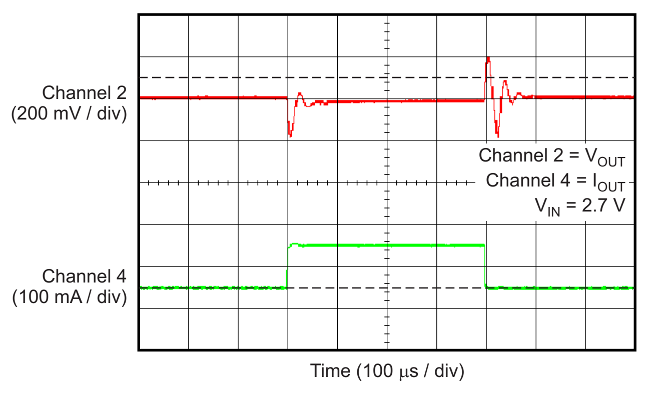


Figure 24. TPS70912 LOAD TRANSIENT (50 mA to 150 mA)

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(TYP)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = +25°C.

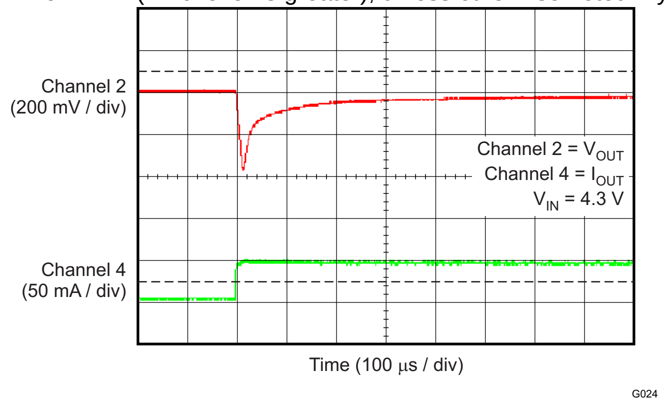


Figure 25. TPS70933 LOAD TRANSIENT (0 mA to 50 mA)

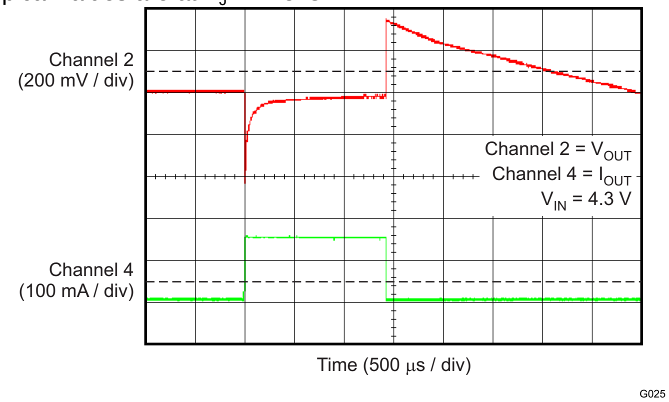


Figure 26. TPS70933 LOAD TRANSIENT (1 mA to 150 mA)

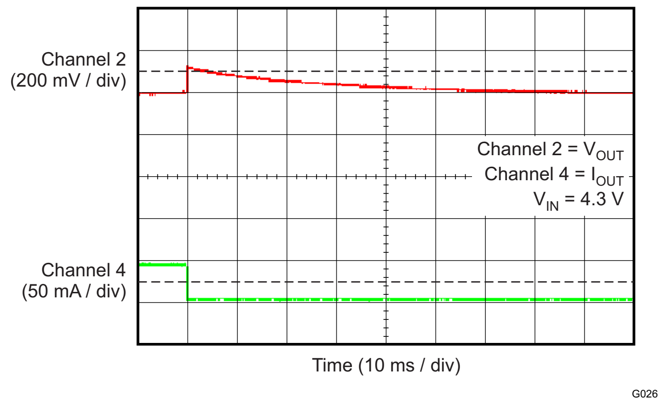


Figure 27. TPS70933 LOAD TRANSIENT (50 mA to 0 mA)

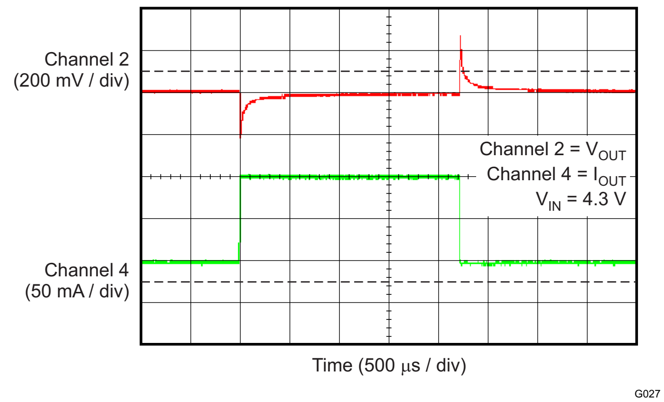


Figure 28. TPS70933 LOAD TRANSIENT (50 mA to 150 mA)

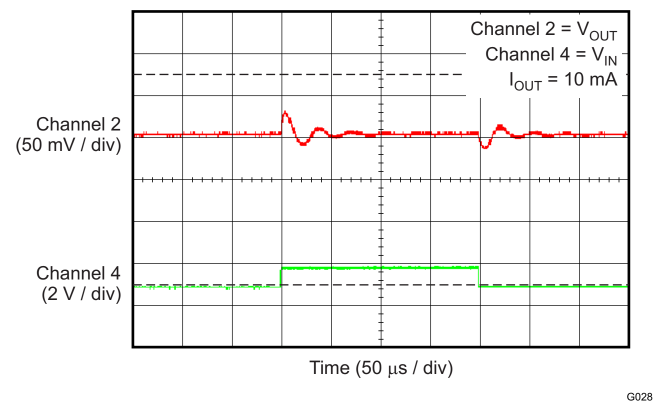


Figure 29. TPS70912 LINE TRANSIENT (2.7 V to 3.7 V)

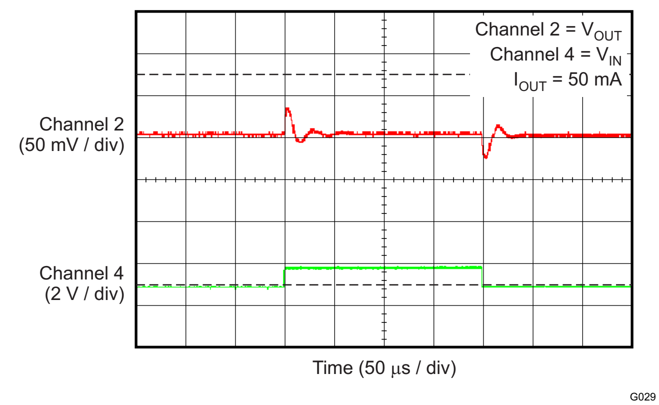


Figure 30. TPS70912 LINE TRANSIENT (2.7 V to 3.7 V)

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), I_{OUT} = 10 mA, V_{EN} = 2 V, C_{OUT} = 2.2 µF, and V_{IN} = $V_{OUT(TYP)}$ + 1 V or 2.7 V (whichever is greater), unless otherwise noted. Typical values are at T_J = +25°C.

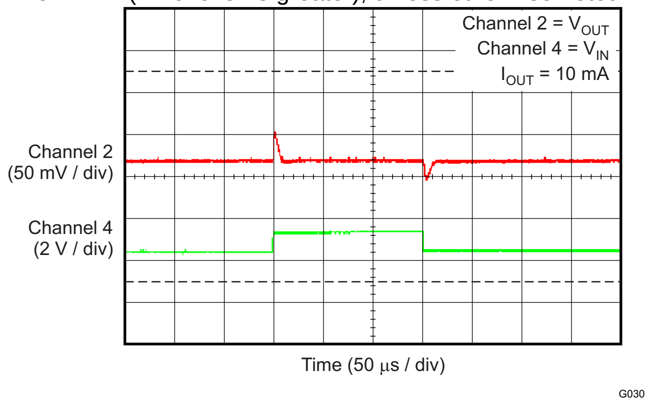


Figure 31. TPS70933 LINE TRANSIENT (4.3 V to 5.3 V)

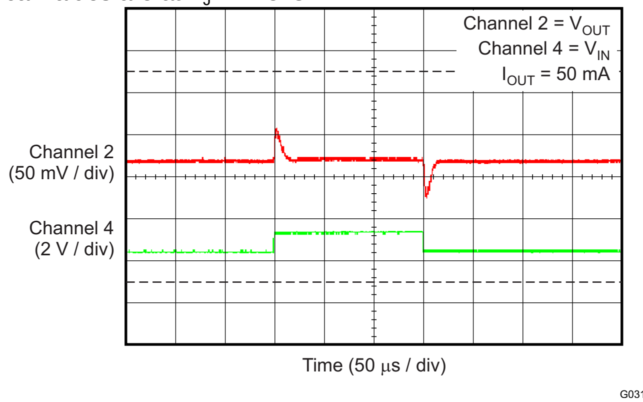


Figure 32. TPS70933 LINE TRANSIENT (4.3 V to 5.3 V)

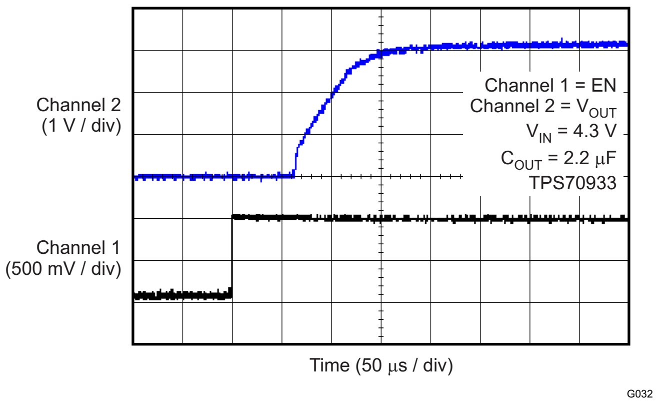


Figure 33. POWER-UP WITH ENABLE

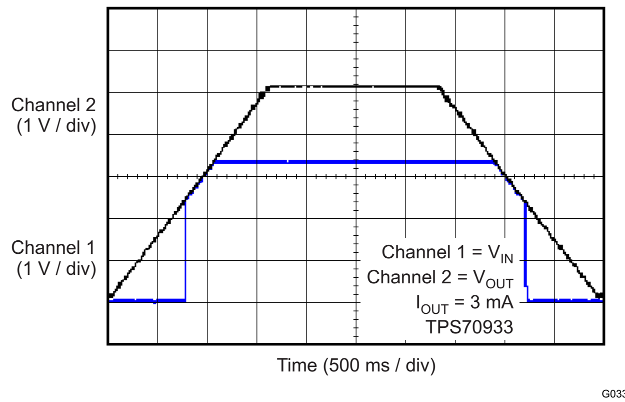


Figure 34. POWER-UP AND POWER-DOWN RESPONSE

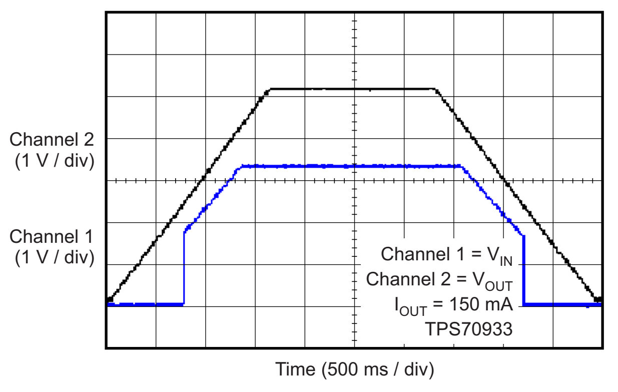


Figure 35. POWER-UP AND POWER-DOWN RESPONSE

APPLICATION INFORMATION

The TPS709xx are a series of devices that belong to a new family of next-generation voltage regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, makes these devices ideal for RF portable applications, current limit, and thermal protection. The TPS709xx are specified from –40°C to +125°C.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the device GND pin.

INTERNAL CURRENT LIMIT

The TPS709xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as ($V_{OUT} = I_{LIMIT} \times R_{LOAD}$). The PMOS pass transistor dissipates [(V_{IN} – V_{OUT}) × I_{LIMIT}] until a thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Information* section for more details.

The TPS709xx are characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 200 mA of output current. The TPS709xx continue to operate for output currents between 150 mA and 200 mA but some data sheet parameters may not be met.

DROPOUT VOLTAGE

The TPS709xx use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with the output current because the PMOS device behaves like a resistor in dropout.

The ground pin current of many linear voltage regulators increases substantially when the device is operated in dropout. This increase in ground pin current while operating in dropout can be several orders of magnitude larger than when the device is not in dropout. The TPS709xx employ a special control loop that limits the increase in ground pin current while operating in dropout. This functionality allows for the most efficient operation while in dropout conditions tht can greatly increase battery run times.

INPUT AND OUTPUT CAPACITOR

The TPS709xx are stable with output capacitors with an effective capacitance of 2.0 µF or greater for output voltages below 1.5 V. For output voltages equal or greater than 1.5 V, the minimum effective capacitance for stability is 1.5 µF. The maximum capacitance for stability is 47 µF. The equivalent series resistance (ESR) of the output capacitor should be between 0 Ω and 0.2 Ω for stability.

The effective capacitance is the minimum capacitance value of a capacitor after taking into account variations resulting from tolerances, temperature, and dc bias effects. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and ESR over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 2.2-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is necessary if line transients greater than 10 V in magnitude are anticipated.

TRANSIENT RESPONSE

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS709xx use an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

REVERSE CURRENT PROTECTION

The TPS709xx have integrated reverse current protection. Reverse current protection prevents current from flowing from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse current protection circuitry places the power path in high impedance when it detects that the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to 10 nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 1.8 V. Reverse current can flow if the output voltage is less than 1.8 V and if input voltage is less than the output voltage.

If voltage is applied to the input pin, then the maximum voltage that can be applied to the OUT pin is the lower of three times the nominal output voltage or 6.5 V. For example, if the 1.2-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 3.6 V. If the 5.0-V output voltage version is used, then the maximum reverse bias voltage that can be applied to the OUT pin is 6.5 V.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The TPS709xx internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS709xx into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, which presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the Thermal Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (October 2013) to Revision E	Page
• Changed DRV (SON-6) package status from Preview to Production Data	1
• Deleted SON-6 package from footnote 1 in *Features* section	1
• Deleted DRV package from pin out diagram note	1
• Deleted DRV from pin out note in the *Pin Configurations* section	4

Changes from Revision C (June 2013) to Revision D	Page
• Changed device status from Production Data to Mixed Status	1
• Changed last Features bullet: added footnote and changed device order	1
• Added note to pin out diagrams	1
• Added product preview footnote to pin configurations	4

Changes from Revision B (November 2012) to Revision C	Page
• Changed title	1
• Added DCY (SOT-223) and DRV (SON) packages to data sheet	1
• Changed I_Q feature bullet value from 1.35 µA to 1 µA	1
• Added typical application circuit	1
• Changed quiescent current value in first paragraph of *Description* section from 1.35 µA to 1 µA	1
• Changed text in second paragraph of *Description* section from "leakage" to "shutdown."	1
• Added DRV and DCY packages to Thermal Information table	2
• Changed ground pin current typical values for I_{OUT} = 0-mA test conditions	3
• Added DCY and DRV packages to *Pin Configuration* section	4
• Added DCY and DRV packages to Pin Descriptions table	4

Changes from Revision A (October 2012) to Revision B	Page
• Changed *Line regulation* and *Load regulation* parameters in Electrical Characteristics table	3
• Changed I_{GND} parameter test conditions in Electrical Characteristics table	3
• Changed $I_{SHUTDOWN}$ parameter test conditions in Electrical Characteristics table	3
• Changed footnote 4 in Electrical Characteristics table	3
• Added Pin Configuration section	4
• Changed second paragraph of *Dropout Voltage* section	12

Changes from Original (March 2012) to Revision A	Page
• Changed device status from Product Preview to Production Data	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70912DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCX	Samples
TPS70912DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCX	Samples
TPS70912DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SCX	
TPS70912DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		SCX	
TPS70912DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCX	Samples
TPS70912DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCX	Samples
TPS709135DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCY	Samples
TPS709135DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCY	Samples
TPS70915DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIM	Samples
TPS70915DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIM	Samples
TPS70916DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCZ	Samples
TPS70916DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SCZ	Samples
TPS70918DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDA	Samples
TPS70918DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDA	Samples
TPS70919DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDB	Samples
TPS70919DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDB	Samples
TPS70925DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70925DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDC	Samples
TPS70925DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDC	
TPS70925DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDC	
TPS70925DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDC	Samples
TPS70925DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDC	Samples
TPS70927DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDD	Samples
TPS70927DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDD	Samples
TPS70928DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDE	Samples
TPS70928DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDE	Samples
TPS70930DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDF	Samples
TPS70930DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDF	Samples
TPS70930DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SDF	
TPS70930DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SDF	
TPS70930DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDF	Samples
TPS70930DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDF	Samples
TPS70933DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDG	Samples
TPS70933DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDG	Samples
TPS70933DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SDG	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS70933DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SDG	
TPS70933DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDG	Samples
TPS70933DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDG	Samples
TPS70936DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SEJ	Samples
TPS70936DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SEJ	Samples
TPS70936DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SEJ	
TPS70936DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SEJ	
TPS70938DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIC	Samples
TPS70938DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIC	Samples
TPS70939DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SID	Samples
TPS70939DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SID	Samples
TPS70950DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDH	Samples
TPS70950DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SDH	Samples
TPS70950DCYR	PREVIEW	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SDH	
TPS70950DCYT	PREVIEW	SOT-223	DCY	4	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 85	SDH	
TPS70950DRVR	PREVIEW	SON	DRV	6	3000	TBD	Call TI	Call TI	-40 to 85	SDH	
TPS70950DRVT	PREVIEW	SON	DRV	6	250	TBD	Call TI	Call TI	-40 to 85	SDH	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS70912, TPS70918, TPS70925, TPS70928, TPS70930, TPS70933, TPS70936, TPS70950 :

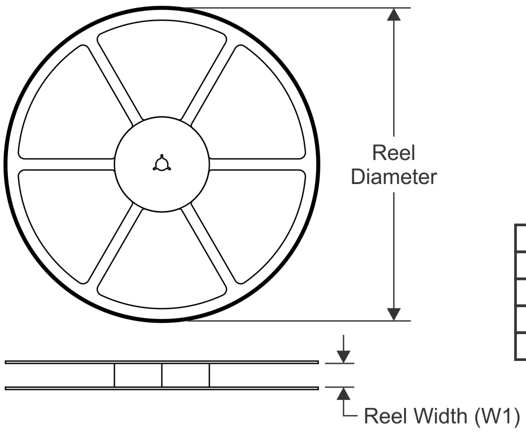
- Automotive: TPS70912-Q1, TPS70918-Q1, TPS70925-Q1, TPS70928-Q1, TPS70930-Q1, TPS70933-Q1, TPS70936-Q1, TPS70950-Q1

NOTE: Qualified Version Definitions:

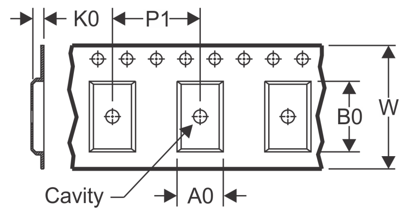
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

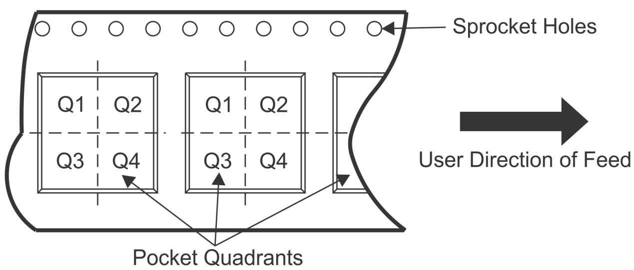


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

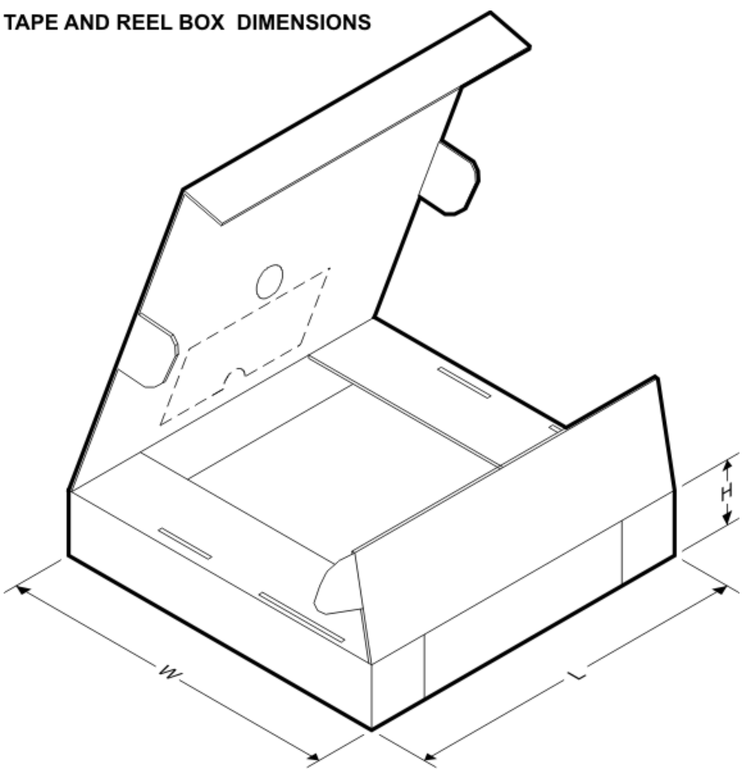


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70912DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70912DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70912DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70912DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS709135DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS709135DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70915DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70916DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70916DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70918DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70919DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70919DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70925DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70925DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70925DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS70927DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70927DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70928DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70930DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70930DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70933DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70933DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70933DRVR	SON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70933DRVT	SON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS70936DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS70936DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70938DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70938DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70939DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70939DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS70950DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

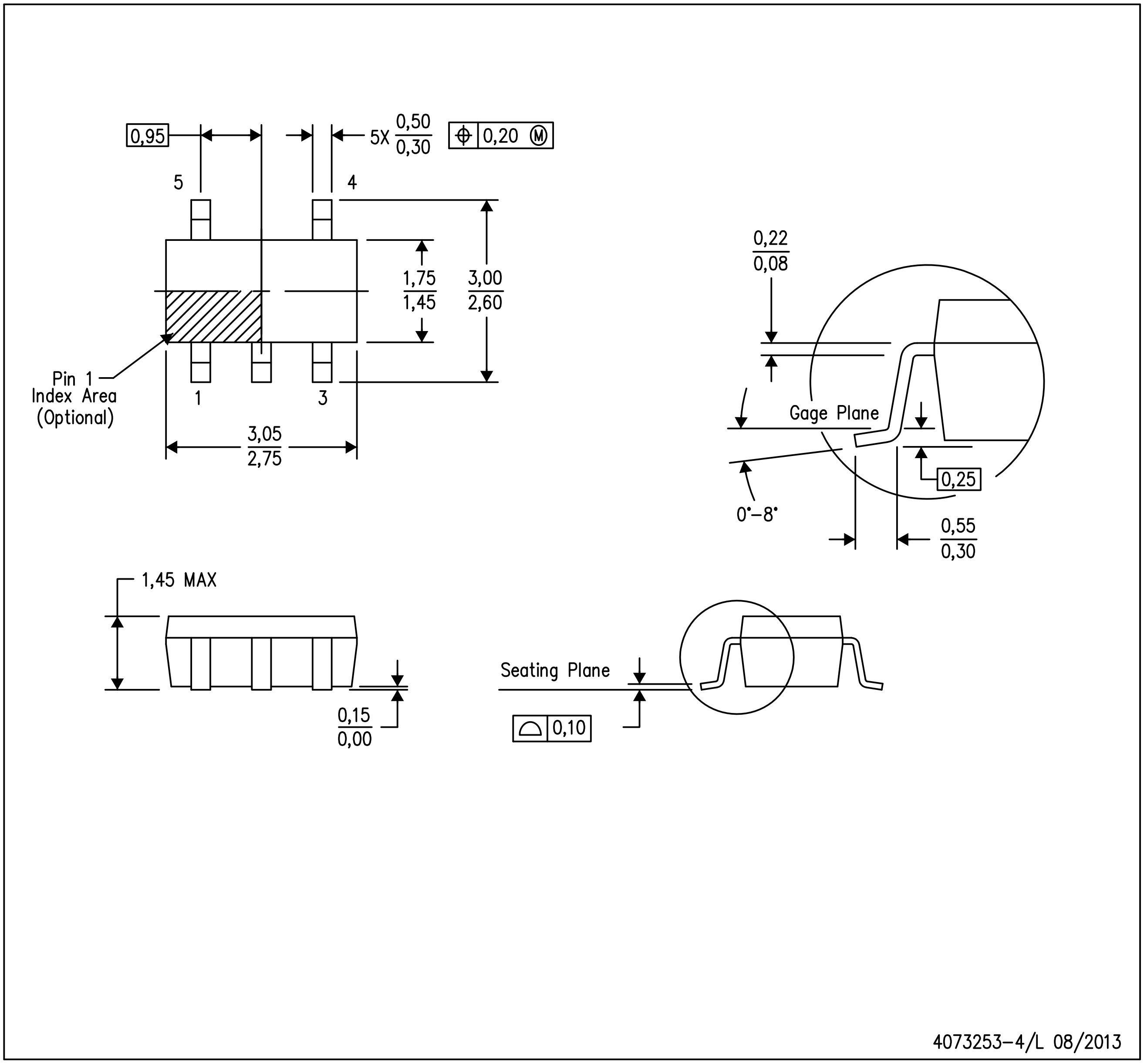
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

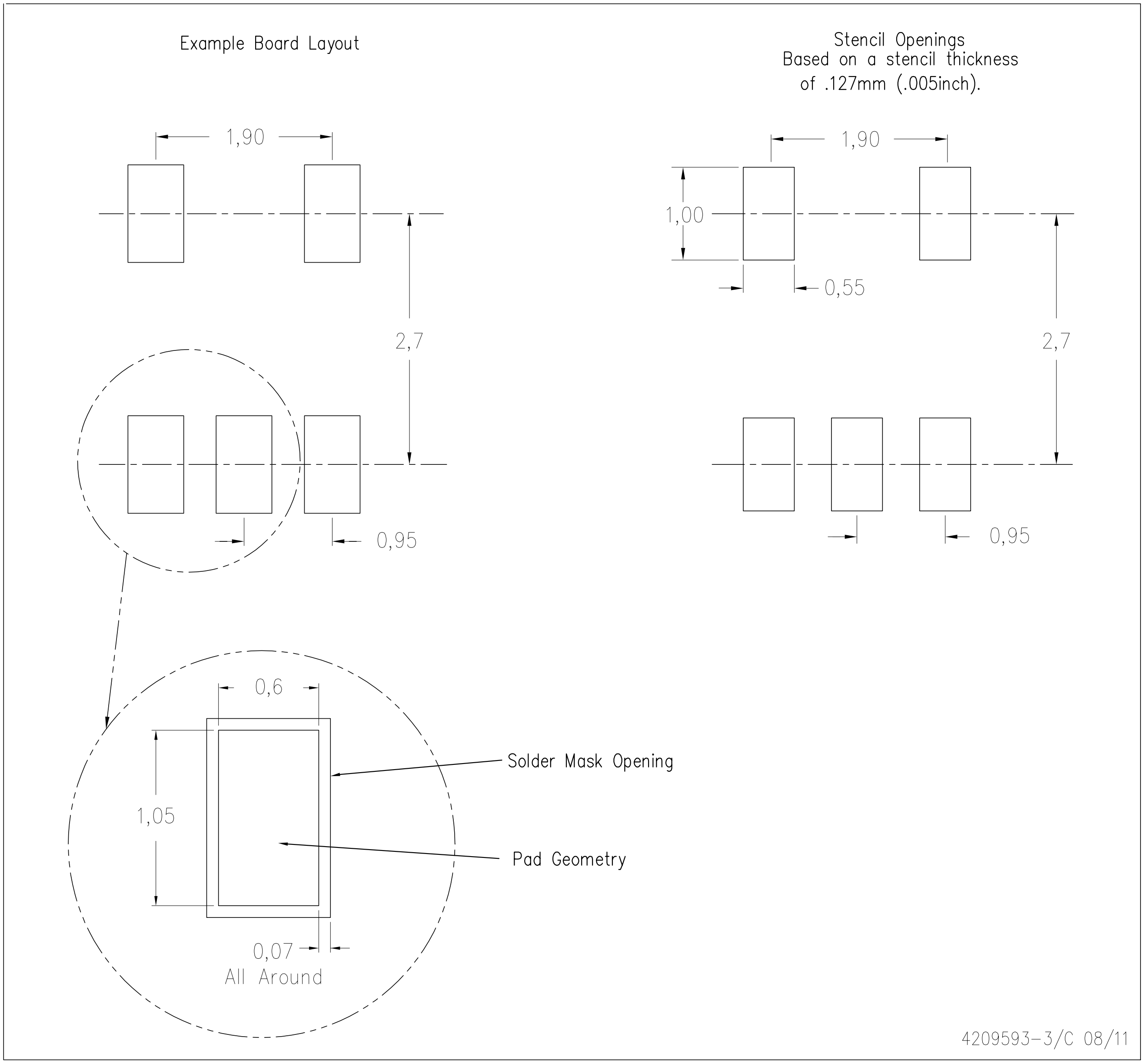
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS70912DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70912DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70912DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS70912DRVT	SON	DRV	6	250	210.0	185.0	35.0
TPS709135DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS709135DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70915DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70915DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70916DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70916DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70918DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70918DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70919DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70919DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70925DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70925DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70925DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS70925DRVT	SON	DRV	6	250	210.0	185.0	35.0
TPS70927DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70927DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70928DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70928DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70930DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70930DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70930DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS70930DRVT	SON	DRV	6	250	210.0	185.0	35.0
TPS70933DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70933DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70933DRVR	SON	DRV	6	3000	210.0	185.0	35.0
TPS70933DRVT	SON	DRV	6	250	210.0	185.0	35.0
TPS70936DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70936DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70938DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70938DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70939DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70939DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS70950DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS70950DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



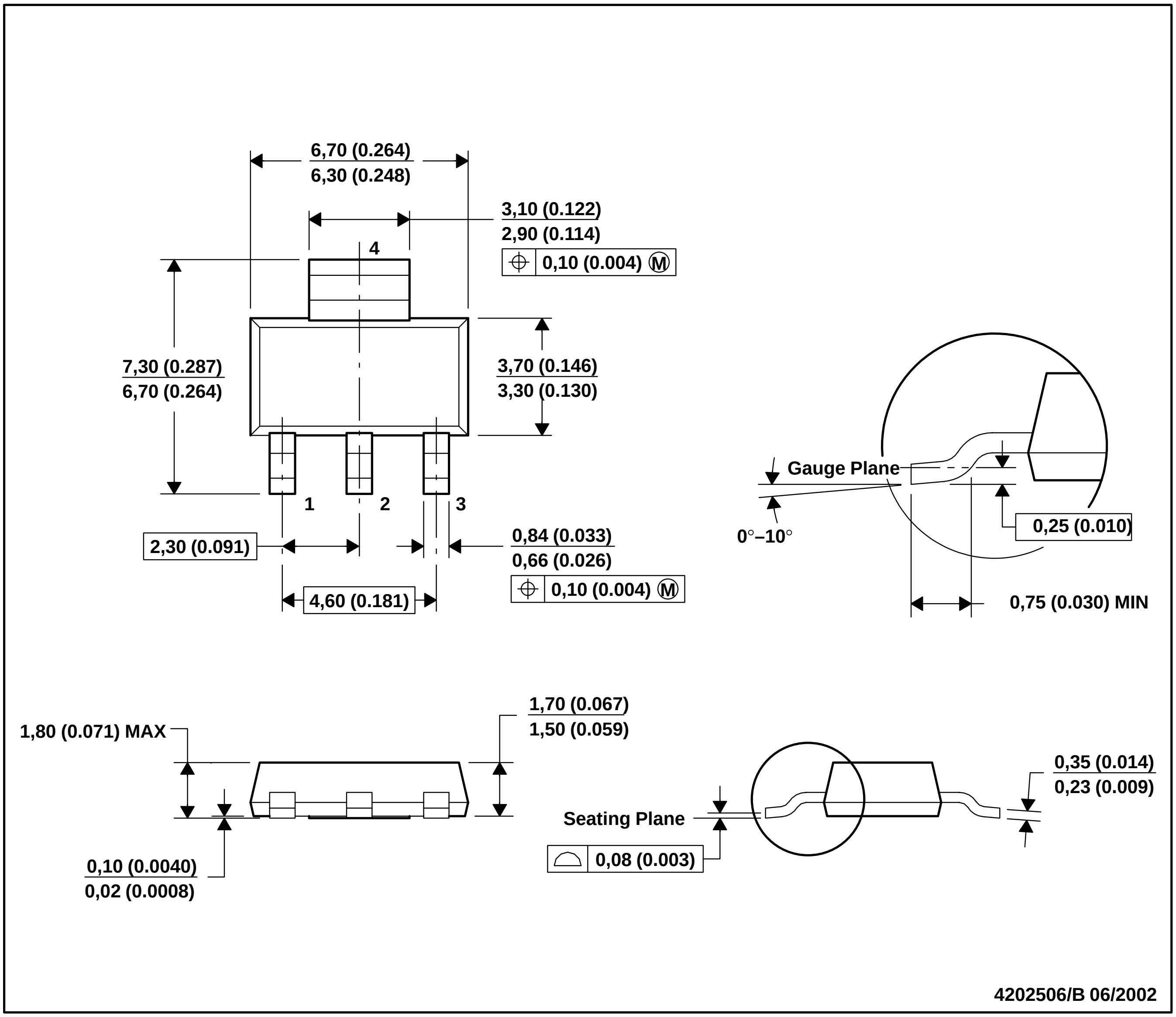
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



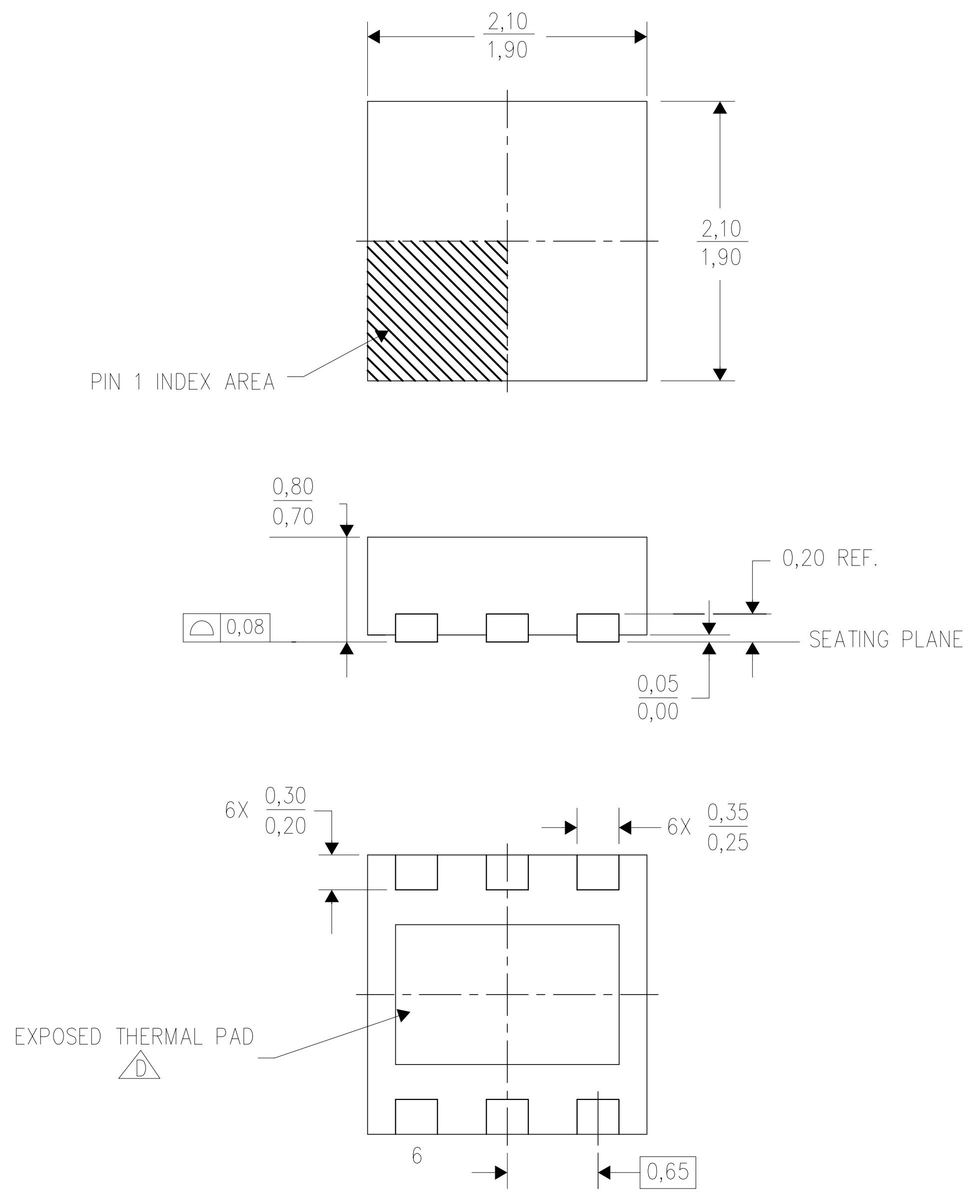
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

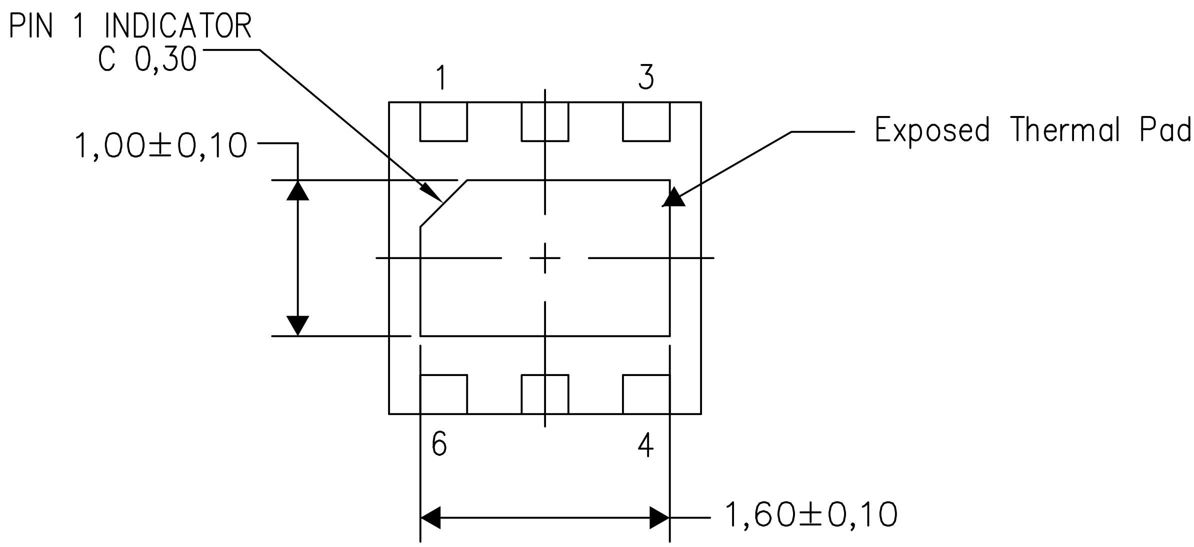
DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



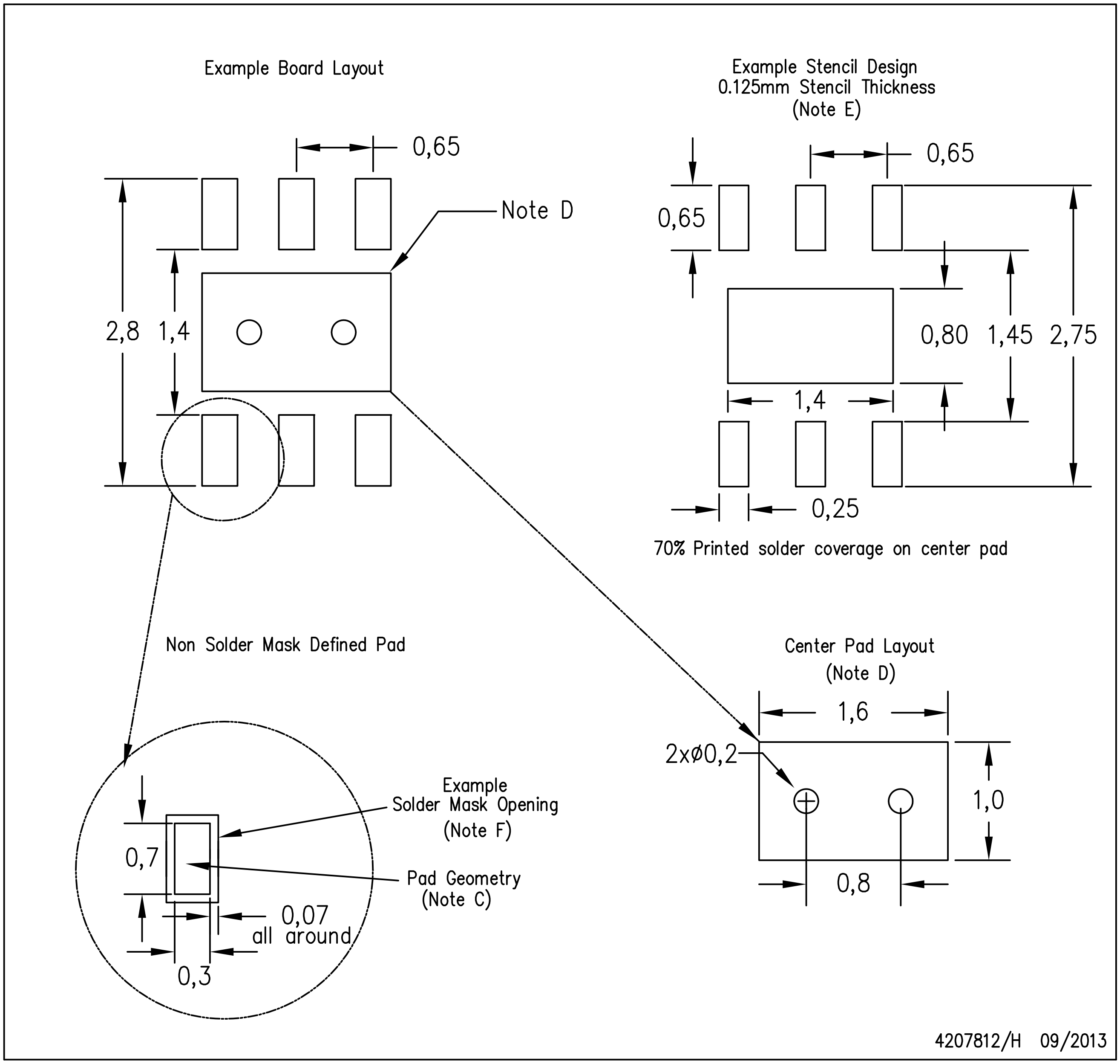
Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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