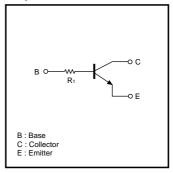
Digital transistors (built-in resistor)

DTC114TM / DTC114TE / DTC114TUA / DTC114TKA / DTC114TSA

●Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making device design easy.

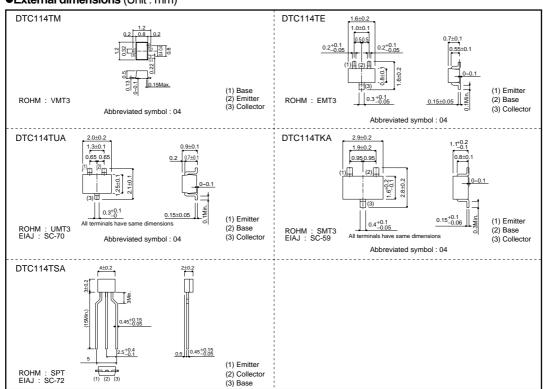
●Equivalent circuit



Structure

NPN digital transistor (With single built in resistor)

●External dimensions (Unit:mm)



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol		Unit				
- Farameter		М	Е	UA	KA	SA	Offic
Collector-base voltage	Vсво		V				
Collector-emitter voltage	VCEO		V				
Emitter-base voltage	Vево		V				
Collector current	Ic		mA				
Collector power dissipation	Pc	15	50	200		300	mW
Junction temperature	Tj	150					°C
Storage temperature	Tstg	−55 to +150					°C

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Collector-base breakdown voltage	ВУсво	50	_	-	V	Ic=50μA
Collector-emitter breakdown voltage	BVCEO	50	-	-	V	Ic=1mA
Emitter-base breakdown voltage	ВУЕВО	5	-	-	V	Iε=50μA
Collector cutoff current	Ісво	_	_	0.5	μА	Vcb=50V
Emitter cutoff current	ІЕВО	_	-	0.5	μА	V _{EB} =4V
Collector-emitter saturation voltage	VCE(sat)	_	_	0.3	V	Ic/Iв=10mA/1mA
DC current transfer ratio	hFE	100	250	600	-	VcE=5V, Ic=1mA
Input resistance	R ₁	7	10	13	kΩ	-
Transition frequency	fτ	-	250	-	MHz	Vce=10V, Ie=-5mA, f=100MHz *

^{*} Transition frequency of the device

Packaging specifications

	Package	VMT3	EMT3	UMT3	SMT3	SPT			
	Package type	Taping	Taping	Taping	Taping	Taping			
	Code	T2L	TL	T106	T146	TP			
Туре	Basic ordering unit (pieces)	8000	3000	3000	3000	5000			
DTC114TM		0	-	-		_			
DTC114TE		-	0	-	-	-			
DTC114TU/	4			0		-			
DTC114TKA	4	-	-	-	0	-			
DTC114TSA	4	-	-	-	-	0			

•Electrical characteristic curves

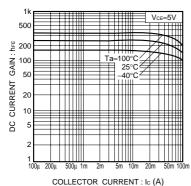


Fig.1 DC current gain vs. collector current

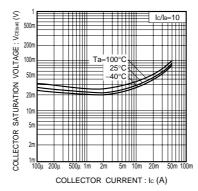


Fig.2 Collector-emitter saturation voltage vs. collector current

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