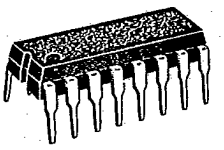
MN4042B / MN4042BS

Quad D Latches

■ Description

The MN4042B/S are quad D latches which have a common clock line and different data input terminals.
When the input (El) is "H" level, the output (O) shows the input (D) while input (E_0) is on the positive going edge; when the input (E_0) is on the negative going edge, output (O) maintains the input (D).
When the input (E_0) is on the negative going edge, the output (D) does not change even if input (D) changes.
When input (E_1) is at the "L" level, input (D) appears on the output (O) while input (E_0) is at the "L" level, and while input (E_0) is at the "H" level, Latch operates.
The MN4042B/S are equivalent to MOTOROLA MC14042B and RCA CD4042B.

P- 3



16-Pin • Plastic DIL Package

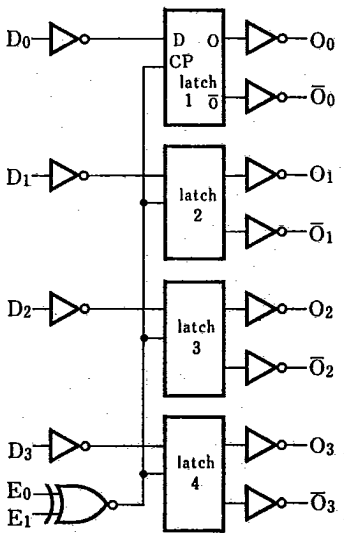
P- 4

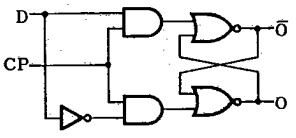
16-Pin • Panaflat Package (SO-16D)

■ Tructh Table

Input		Output
E_0	E_1	O
L	L	D
L	H	latch
H	L	latch
H	H	D

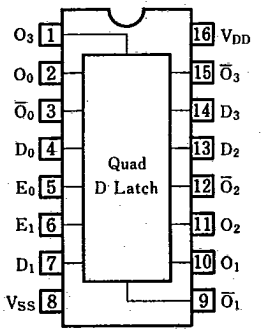
■ Logic Diagram





(One latch)

Pin Configuration



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

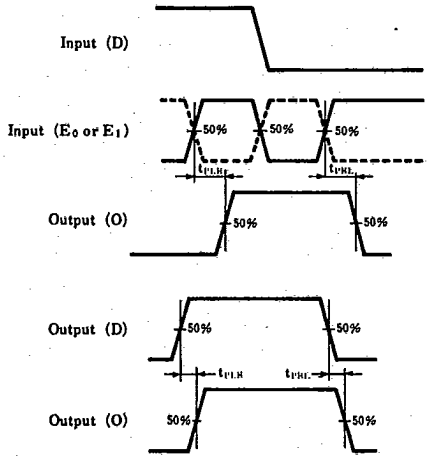
■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	V_I=V_{SS} or V_{DD}		—	4	—	4	—	30	μA
	10				—	8	—	8	—	60	
	15				—	16	—	16	—	120	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD}		—	0.05	—	0.05	—	0.05	V
	10		$\|I_O\|$<1μA		—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD}		4.95	—	4.95	—	4.95	—	V
	10		$\|I_O\|$<1μA		9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\|I_O\|$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA

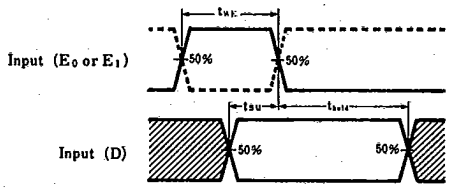
■ **Switching Characteristics** ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time D→O, $\overline{O}$ (H→L)	5	t_{PHL}	—	95	285	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time D→O, $\overline{O}$ (L→H)	5	t_{PLH}	—	85	255	ns
	10		—	40	120	
	15		—	30	90	
Propagation Delay Time E→O, $\overline{O}$ (H→L)	5	t_{PHL}	—	130	390	ns
	10		—	50	150	
	15		—	35	105	
Propagation Delay Time E→O, $\overline{O}$ (L→H)	5	t_{PLH}	—	120	360	ns
	10		—	50	150	
	15		—	35	105	
Minimum Enable Pulse Width	5	t_{WE}	—	45	135	ns
	10		—	20	60	
	15		—	15	45	
Set-up Time D→E	5	t_{su}	—	10	30	ns
	10		—	5	20	
	15		—	5	20	
Hold Time D→E	5	t_{hold}	—	−5	15	ns
	10		—	0	15	
	15		—	0	15	
Input Capacitance		C_I	—	—	7.5	pF

• Dynamic Signal Waveforms



Waveforms showing propagation delays for D to O, with latch enabled



Waveforms showing minimum enable pulse width, set-up time and hold time for E and D
Set-up and hold-times are shown as positive values but may be specified as negative values.