

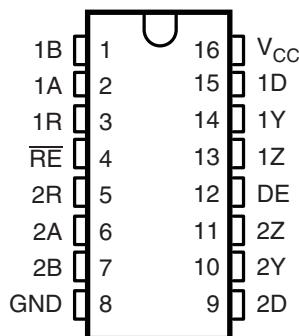
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

Check for Samples: [SN7534050](#), [SN7534051](#)

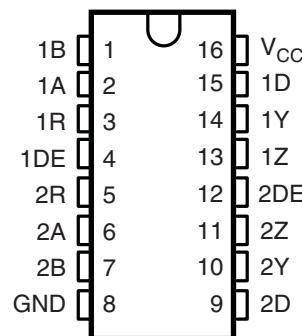
FEATURES

- Meet or Exceed Standards TIA/EIA-422-B and ITU Recommendation V.11
- Operate From Single 5-V Power Supply
- Driver Positive and Negative Current Limiting
- Receiver Input Sensitivity: $\pm 200\text{mV}$
- Receiver Input Impedance: $12\text{ k}\Omega$ Min
- Driver 3-State Outputs
- Receiver 3-State Outputs (SN7534050 Only)

**SN7534050...N OR NS PACKAGE
(TOP VIEW)**



**SN7534051...N OR NS PACKAGE
(TOP VIEW)**



DESCRIPTION

The SN7534050 and SN7534051 dual differential drivers and receivers are monolithic integrated circuits designed to meet the requirements of ANSI standards TIA/EIA-422-B and ITU Recommendations V.11.

The driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on transmission bus line.

The SN7534050 combines dual 3-state differential drivers and dual 3-state differential input receivers. The drivers and receivers have active-high and active-low enables, respectively which can be externally connected together to function as direction control. SN7534051 drivers each have an individual active-high enable.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾ (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-20°C to 85°C	PDIP – N	Tube of 25	SN7534050N	SN7534050N
	SOP – NS	Tube of 50	SN7534050NS	SN7534050
		Reel of 2000	SN7534050NSR	SN7534050
	PDIP – N	Tube of 25	SN7534051N	SN7534051N
	SOP – NS	Tube of 50	SN7534051NS	SN7534051
		Reel of 2000	SN7534051NSR	SN7534051

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLES

**Table 1. SN7534050,
SN7534051
Each Driver⁽¹⁾**

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level,
X = irrelevant, Z = high impedance
(off)

**Table 2. SN7534050
Each Receiver⁽¹⁾**

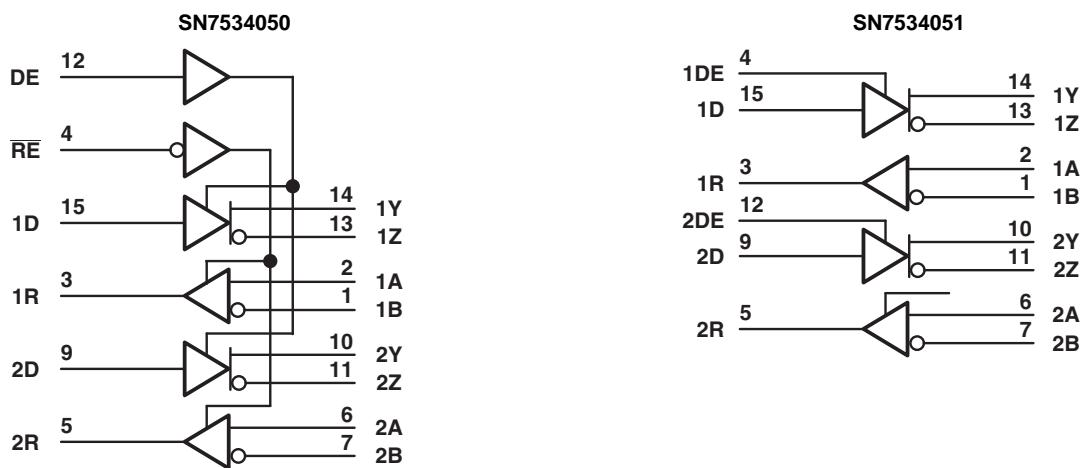
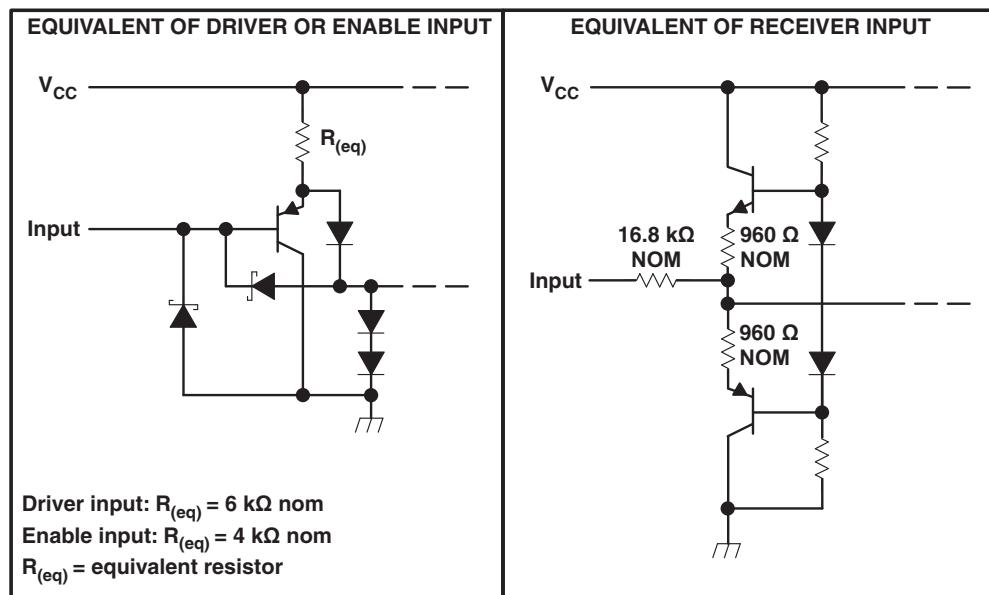
DIFFERENTIAL INPUTS, A–B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	L	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant,
Z = high impedance (off)

**Table 3. SN7534051
Each Receiver⁽¹⁾**

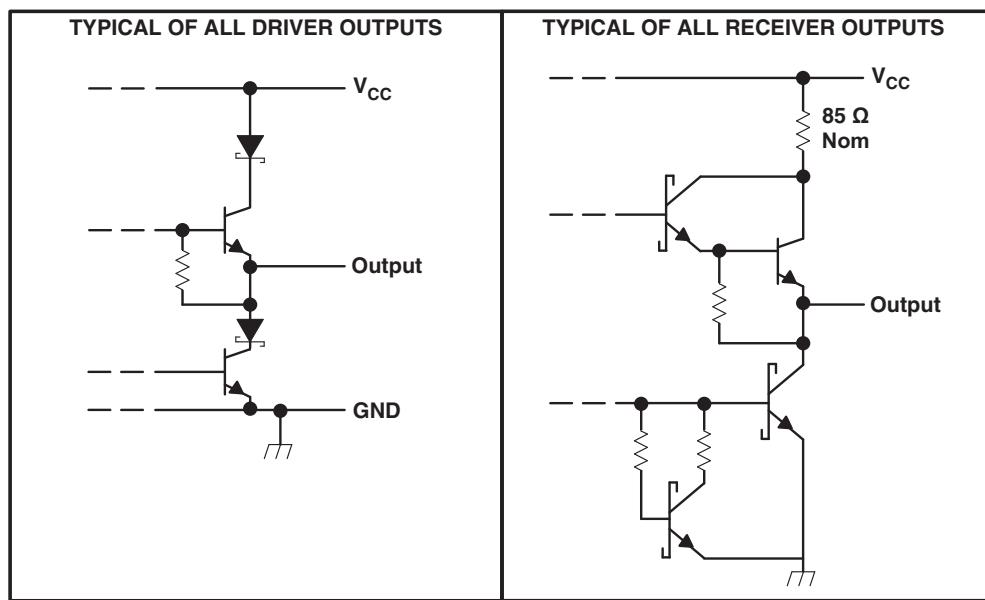
DIFFERENTIAL INPUTS, A–B	OUTPUT R
$V_{ID} \geq 0.2 \text{ V}$	H
$-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$?
$V_{ID} \leq -0.2 \text{ V}$	L

(1) H = high level, L = low level,
? = indeterminate

LOGIC DIAGRAMS

SCHEMATIC OF INPUTS


All resistor values are nominal.

SCHEMATIC OF OUTPUTS



All resistor values are nominal.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾		7	V
V_I	Input voltage	DE, \overline{RE} , D inputs	7	V
V_i	Receiver input voltage	A or B inputs	± 25	V
V_{ID}	Receiver differential output voltage ⁽³⁾		± 25	V
V_O	Driver output voltage range	-10	15	V
I_{OL}	Receiver low-level output current		50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	N package	66	°C/W
		NS package	68	
Operating free-air temperature range		-20	85	°C
T_{stg}	Storage temperature range	-65	150	°C
Lead temperature, 1.6 mm (1/16 in) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages, except differential input voltage, are with respect to the network GND.

(3) Differential input voltage is measured at the noninverting terminal, with respect to the inverting terminal.

(4) The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	DE, \overline{RE} , D	2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Common-mode input voltage ⁽¹⁾	Receiver			± 7	V
V_{ID}	Differential input voltage	Receiver			± 12	V
I_{OH}	High-level output current	Driver			40	mA
		Receiver			-400	μA
I_{OL}	Low-level output current	Driver			-40	mA
		Receiver			16	
T_A	Operating free-air temperature		-20		85	$^{\circ}C$

(1) Refer to TIA/EIA-422-B for exact conditions.

DRIVER SECTION

Electrical Characteristics

over recommended supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -20$ mA		3.7		V
V_{OL}	$V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OL} = 20$ mA		1.1		V
V_{OD1}	$I_O = 0$ mA		1.5	6	V
V_{OD2}	$R_L = 100 \Omega$, See Figure 1		2		V
ΔV_{OD}	$R_L = 100 \Omega$, See Figure 1			± 0.4	V
V_{OC}	$R_L = 100 \Omega$, See Figure 1			± 3	V
ΔV_{OC}	$R_L = 100 \Omega$, See Figure 1			± 0.4	V
I_{off}	$V_{CC} = 0$ V	$V_O = 6$ V		100	μA
		$V_O = -0.25$ V		-100	
I_{OZ}	$V_O = -0.25$ V to 6 V			± 100	μA
I_{IH}	$V_I = 2.7$ V			20	μA
I_{IL}	$V_I = 0.4$ V			-100	μA
I_{os}	$V_O = V_{CC}$ or GND		-30	-150	mA
I_{cc}	No load	Output enabled		80	mA
		Output disabled		50	

(1) All typical values are at $V_{CC} = 5$ V and $T_A = 25^{\circ}C$.

(2) Refer to TIA-EIA-422-B for exact conditions.

(3) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

Switching Characteristics

$V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential output delay time	$R_L = 100 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3	20	25	ns	
$t_{t(OD)}$ Differential output transition time	$R_L = 100 \Omega$, $C_L = 50 \text{ pF}$, See Figure 3	27	35	ns	
t_{PLH} Propagation delay time, low- to high-level output	$R_L = 27 \Omega$, See Figure 4	20	25	ns	
t_{PHL} Propagation delay time, high- to low-level output	$R_L = 27 \Omega$, See Figure 4	20	25	ns	
t_{PZH} Output enable time to high level	$R_L = 110 \Omega$, See Figure 5	80	120	ns	
t_{PZL} Output enable time to low level	$R_L = 110 \Omega$, See Figure 6	40	60	ns	
t_{PHZ} Output disable time from high level	$R_L = 110 \Omega$, See Figure 5	90	120	ns	
t_{PLZ} Output disable time from low level	$R_L = 110 \Omega$, See Figure 6	30	45	ns	

RECEIVER SECTION

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IT+} Positive-going input threshold voltage, differential input			0.2		V
V_{IT-} Negative-going input threshold voltage, differential input		-0.2 ⁽²⁾			V
V_{hys} Input hysteresis ($V_{IT+} - V_{IT-}$)		50			mV
V_{IK} Input clamp voltage, \overline{RE}	SN7534050	$I_I = -18 \text{ mA}$		-1.5	V
V_{OH} High-level output voltage		$V_{ID} = 200 \text{ mV}$, $I_{OH} = -400 \mu\text{A}$,	See Figure 2	2.7	V
V_{OL} Low-level output voltage		$V_{ID} = -200 \text{ mV}$, See Figure 2	$I_{OL} = 8 \text{ mA}$	0.45	V
			$I_{OL} = 16 \text{ mA}$	0.5	
I_{OZ} High-impedance-state output current	SN7534050	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$		± 20	μA
I_I Line input current		Other input at 0 V	$V_I = 10 \text{ V}$	1.5	mA
			$V_I = -10 \text{ V}$	-2.5	
I_{IH} High-level enable input current, \overline{RE}	SN7534050	$V_{IH} = 2.7 \text{ V}$		20	μA
I_{IL} Low-level enable input current, \overline{RE}	SN7534050	$V_{IL} = 0.4 \text{ V}$		-100	μA
r_i Input resistance			12		$\text{k}\Omega$
I_{OS} Short circuit output current			-15	-85	mA
I_{CC} Supply current (total package)		No load, enabled	80	110	mA

(1) All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

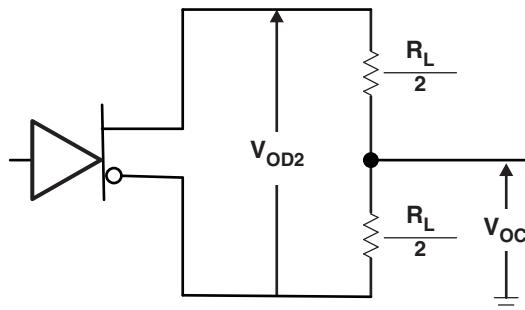
(2) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels.

Switching Characteristics

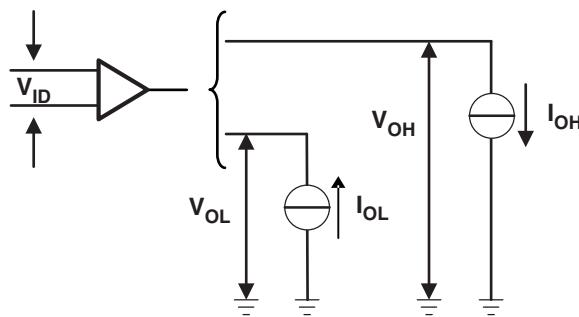
over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = 1.5 \text{ V}$, $C_L = 15 \text{ pF}$, See Figure 7	20	35	ns	
t_{PHL} Propagation delay time, high- to low-level output	$V_{ID} = 1.5 \text{ V}$, $C_L = 15 \text{ pF}$, See Figure 7	22	35	ns	
t_{PZH} Output enable time to high level	SN7534050	$C_L = 15 \text{ pF}$, see Figure 8	17	25	ns
t_{PZL} Output enable time to low level	SN7534050	$C_L = 15 \text{ pF}$, See Figure 8	20	27	ns
t_{PHZ} Output disable time from high level	SN7534050	$C_L = 15 \text{ pF}$, See Figure 8	25	40	ns
t_{PLZ} Output disable time from low level	SN7534050	$C_L = 15 \text{ pF}$, See Figure 8	30	40	ns

PARAMETER MEASUREMENT INFORMATION

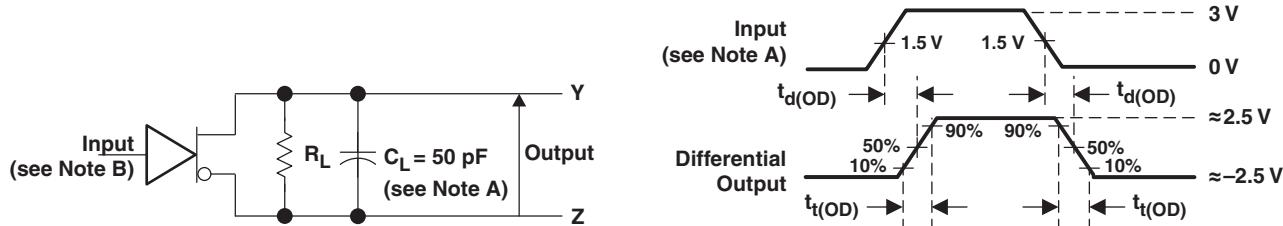


**Figure 1. Driver Test Circuit,
 V_{OD2} and V_{OC}**



**Figure 2. Receiver Test Circuit,
 V_{OH} and V_{OL}**

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

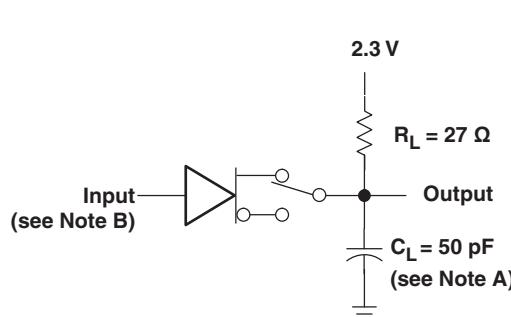


TEST CIRCUIT

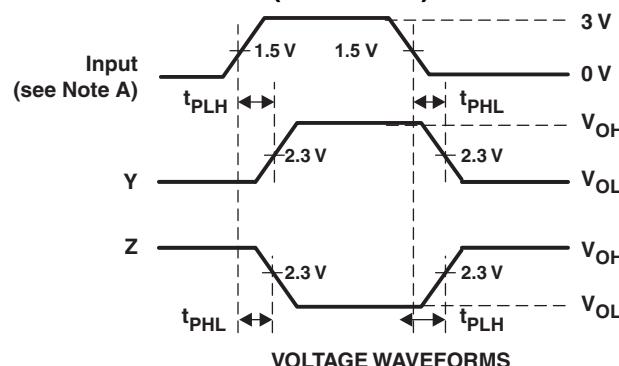
**Figure 3. Driver Test Circuit and Voltage Waveforms,
 $t_{d(OD)}$ and $t_{t(OD)}$**

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

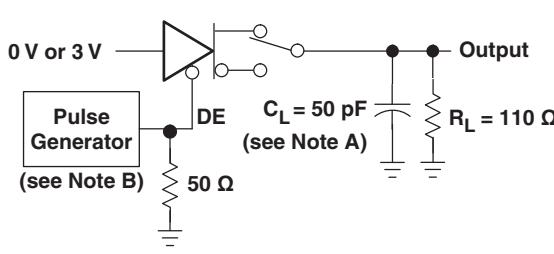
PARAMETER MEASUREMENT INFORMATION (continued)



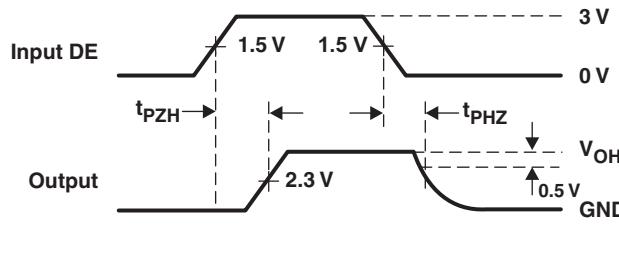
TEST CIRCUIT

Figure 4. Driver Test Circuit and Voltage Waveforms,
 t_{PLH} and t_{PHL}

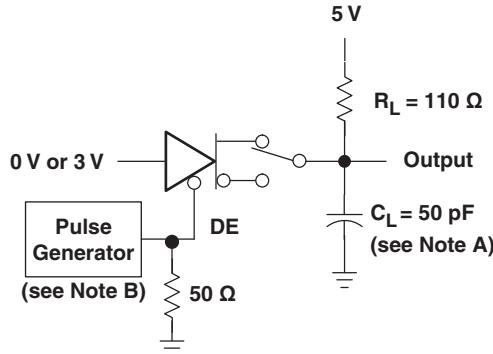
A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.



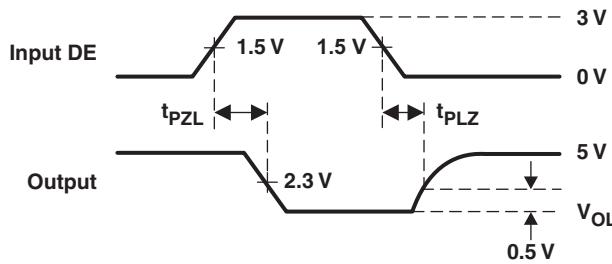
TEST CIRCUIT

Figure 5. Driver Test Circuit and Voltage Waveforms,
 t_{PZH} and t_{PHZ}

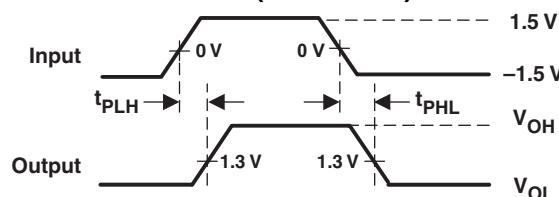
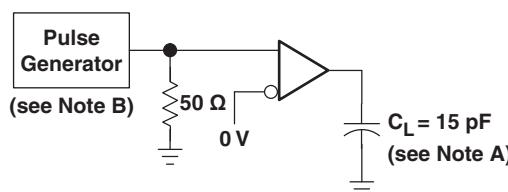
A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.



TEST CIRCUIT

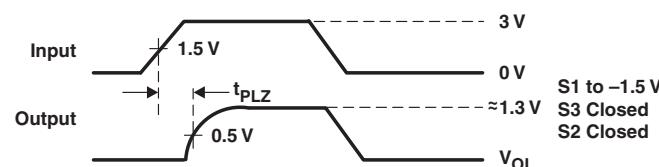
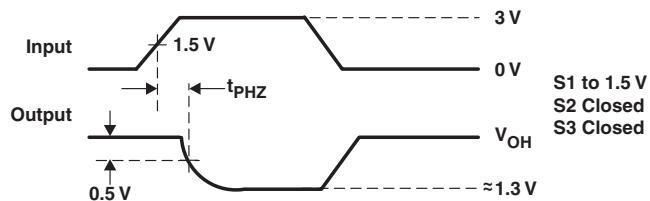
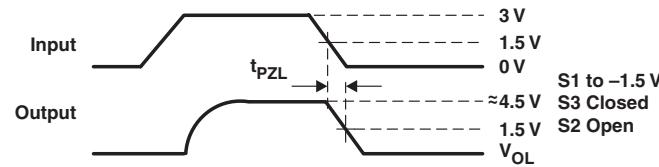
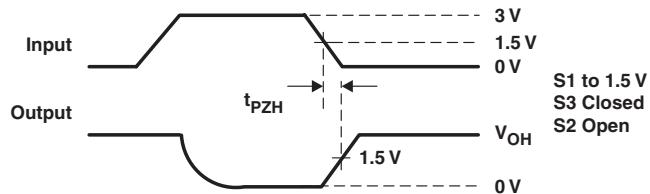
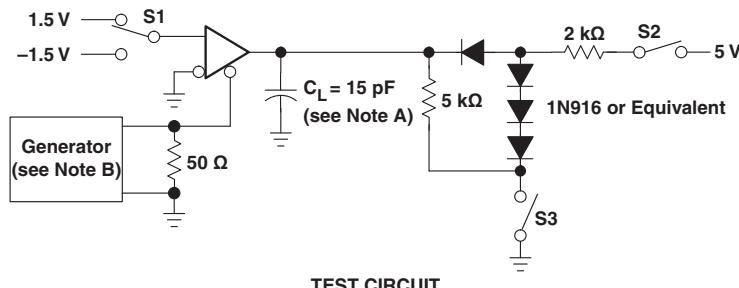
Figure 6. Driver Test Circuit and Voltage Waveforms,
 t_{PZL} and t_{PLZ}

A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.

PARAMETER MEASUREMENT INFORMATION (continued)


**Figure 7. Receiver Test Circuit and Voltage Waveforms,
 t_{PLH} and t_{PHL}**

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR \leq 1 MHz, duty cycle = 50%, $t_r = t_f \leq 6$ ns.



**Figure 8. Receiver Test Circuit and Voltage Waveforms,
 t_{PZH} , t_{PZL} , t_{PHZ} , t_{PLZ} (SN7534050)**

REVISION HISTORY

Changes from Original (May 2007) to Revision A	Page
• Updated document format from QS to DocZone.	1
• Updated ORDERING INFORMATION table.	1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN7534050N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN7534050N
SN7534050N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN7534050N
SN7534050NS	Active	Production	SOP (NS) 16	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	SN7534050
SN7534050NS.A	Active	Production	SOP (NS) 16	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	SN7534050
SN7534050NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN7534050
SN7534050NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN7534050
SN7534051N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN7534051N
SN7534051N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN7534051N
SN7534051NS	Active	Production	SOP (NS) 16	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN7534051
SN7534051NS.A	Active	Production	SOP (NS) 16	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 85	SN7534051
SN7534051NSR	Obsolete	Production	SOP (NS) 16	-	-	Call TI	Call TI	-20 to 85	SN7534051

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

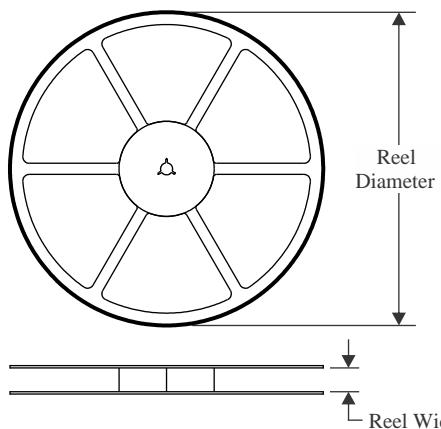
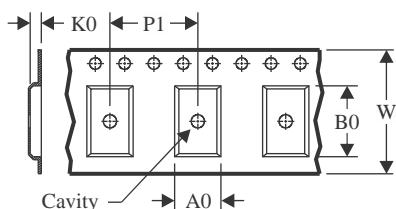
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

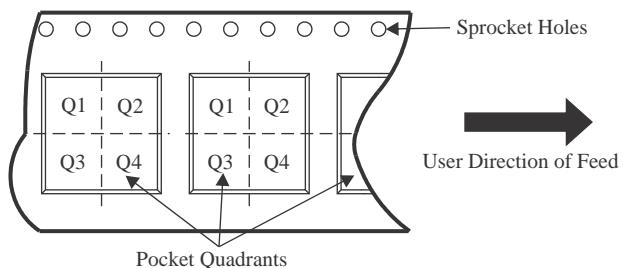
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN7534050NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN7534050NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE

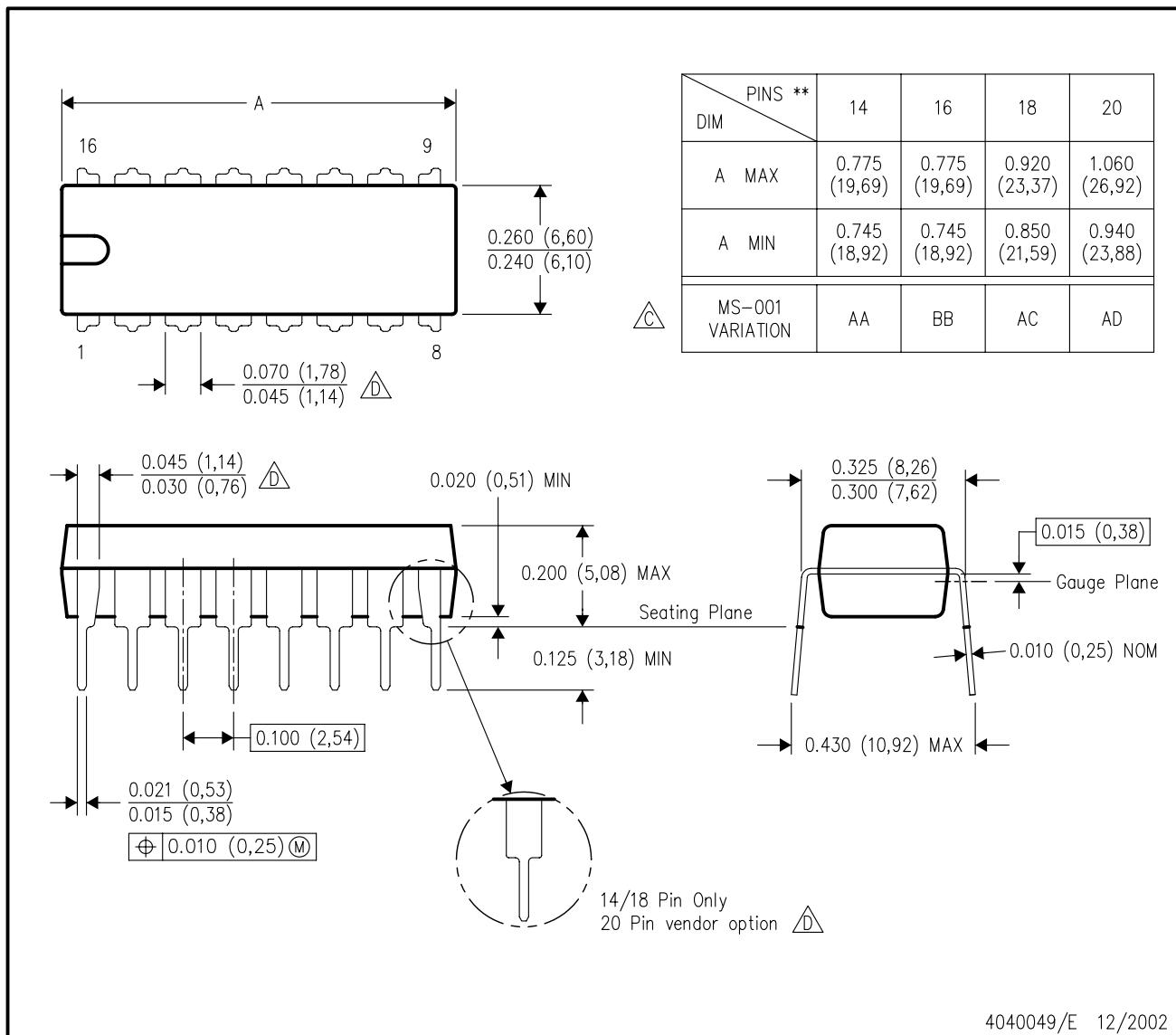

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN7534050N	N	PDIP	16	25	506	13.97	11230	4.32
SN7534050N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN7534050NS	NS	SOP	16	50	530	10.5	4000	4.1
SN7534050NS.A	NS	SOP	16	50	530	10.5	4000	4.1
SN7534051N	N	PDIP	16	25	506	13.97	11230	4.32
SN7534051N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN7534051NS	NS	SOP	16	50	530	10.5	4000	4.1
SN7534051NS.A	NS	SOP	16	50	530	10.5	4000	4.1

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

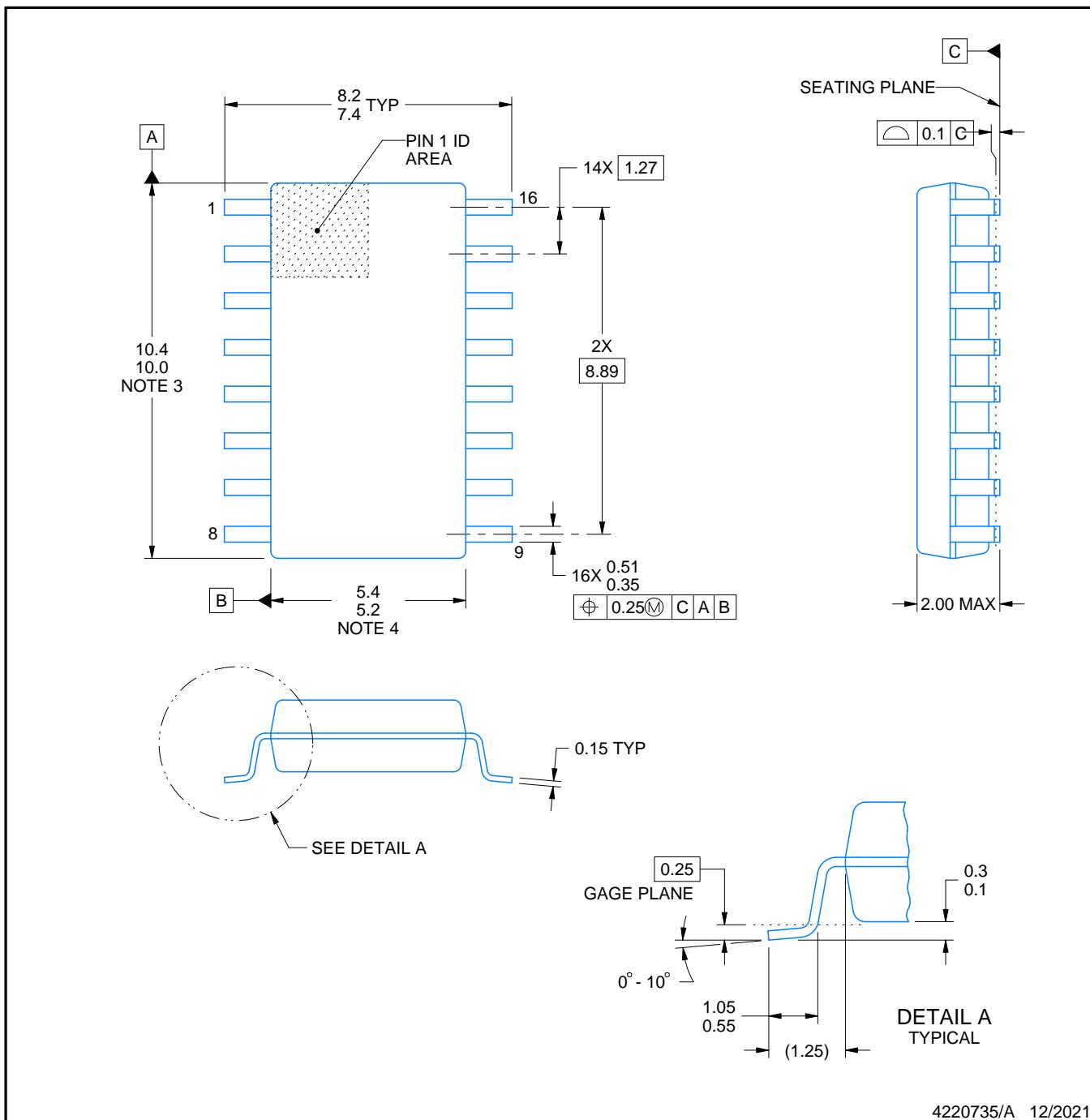
△ The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



NOTES:

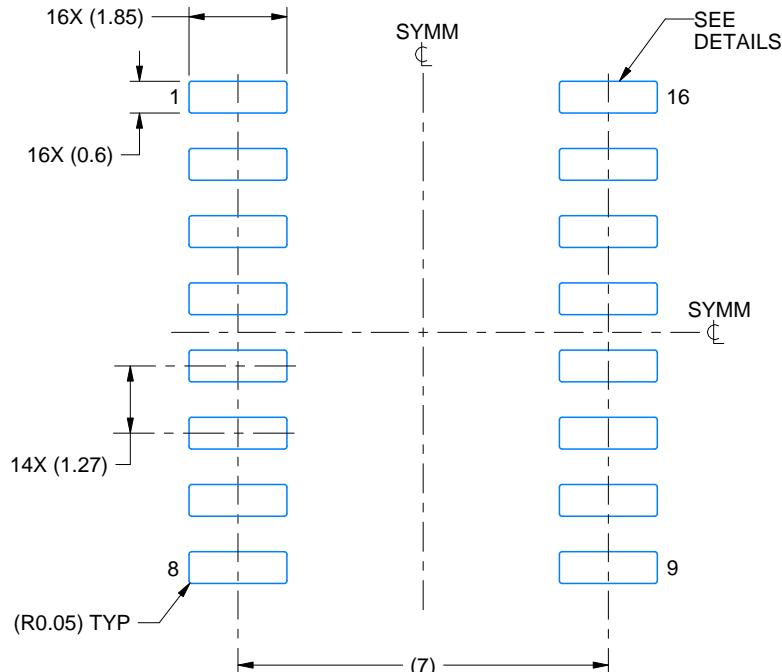
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

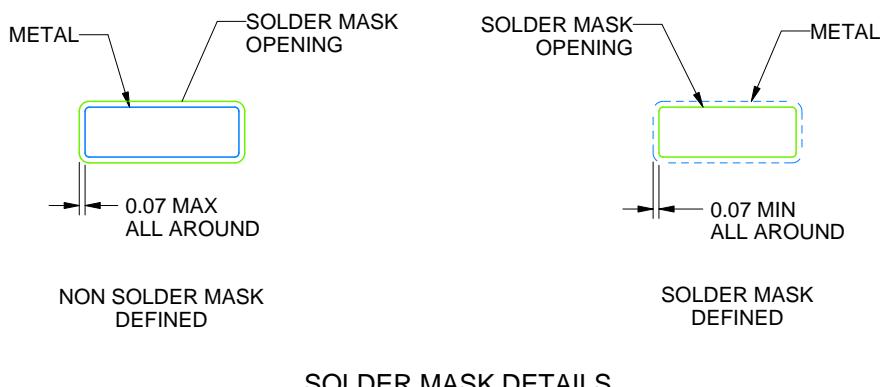
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

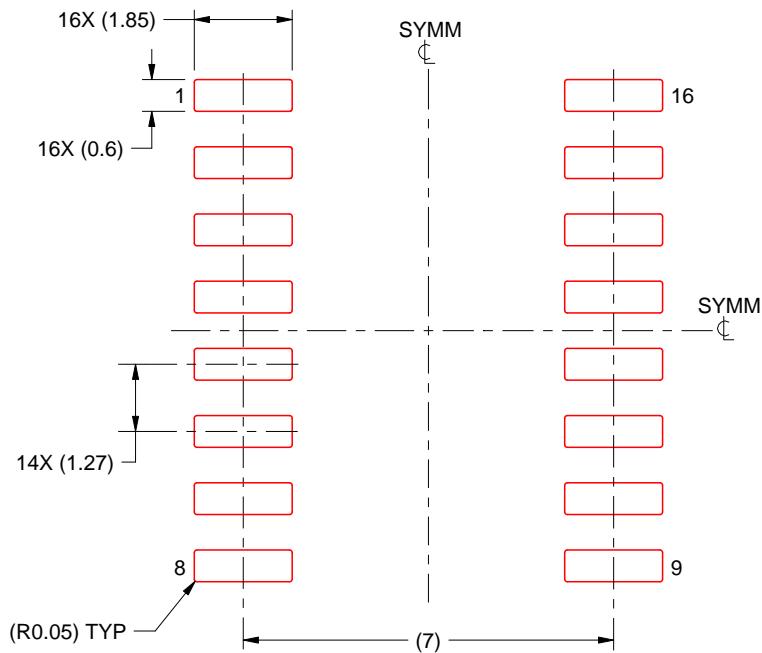
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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